

N-channel 40 V, 5.8 mΩ typ., 80 A STripFET™ VI DeepGATE™ Power MOSFET in a IPAK package

Datasheet - production data

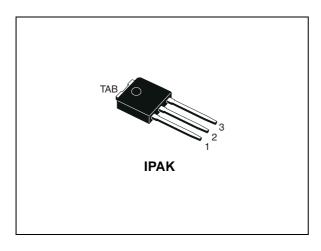
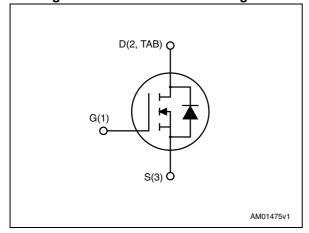


Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	R _{DS(on)} max	Ι _D
STU80N4F6	40 V	$6.3~\mathrm{m}\Omega$	80 A

- · Low gate charge
- Very low on-resistance
- · High avalanche ruggedness

Applications

· Switching applications

Description

This device is an N-channel Power MOSFET developed using the 6^{th} generation of STripFETTM DeepGATETM technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order code	Marking	Package	Packaging
STU80N4F6	80N4F6	IPAK	Tube

Contents STU80N4F6

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STU80N4F6 Electrical ratings

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	40	V
V _{GS}	Gate-source voltage	± 20	V
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25 °C	80	Α
I _D ⁽¹⁾	Drain current (continuous) at T _C = 100 °C	56	Α
I _{DM} ⁽²⁾	Drain current (pulsed) 320		Α
P _{TOT}	Total dissipation at T _C = 25 °C 70		W
I _{AV}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _{Jmax})	e 40	
E _{AS}	Single pulse avalanche energy (starting $T_j = 25$ °C, $I_D = I_{AV}$, $V_{DD} = 25$ V)	149	
	Derating factor 0.47		W/°C
T _{stg}	Storage temperature	-55 to 175	°C
T _j	Max. operating junction temperature	-55 to 175	

^{1.} Current limited by package.

Table 3. Thermal data

	Symbol	Parameter	Value	Unit
Ī	R _{thj-case}	Thermal resistance junction-case max	2.14	°C/W
Ī	R _{thj-amb}	Thermal resistance junction-ambient max	100	°C/W

^{2.} Pulse width limited by safe operating area

Electrical characteristics STU80N4F6

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0$	40			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 40 V V _{DS} = 40 V, T _C =125 °C			1 100	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 20 V			± 100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	2		4	٧
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 40 A		5.8	6.3	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		-	2150	-	pF
C _{oss}	Output capacitance	V _{DS} = 25 V, f = 1 MHz,	-	335	-	pF
C _{rss}	Reverse transfer capacitance	V _{GS} = 0	-	160	-	pF
Qg	Total gate charge	V _{DD} = 20 V, I _D = 80 A,	-	36	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 10 V	-	11	-	nC
Q _{gd}	Gate-drain charge	(see Figure 14)	-	9	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
t _{d(on)}	Turn-on delay time	$V_{DD} = 20 \text{ V}, I_{D} = 40 \text{ A},$ $R_{G} = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (see Figure 15)	-	10.5	-	ns
t _r	Rise time		-	7.6	-	ns
t _d (off)	Turn-off delay time		-	46.1	-	ns
t _f	Fall time		-	11.9	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		80	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		320	Α
V _{SD} (2)	Forward on voltage	I _{SD} = 40 A, V _{GS} = 0	-		1.3	٧
t _{rr}	Reverse recovery time		-	41.1		ns
Q _{rr}	Reverse recovery charge	$I_{SD} = 80 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s}$ $V_{DD} = 32 \text{ V (see Figure 17)}$	-	43.6		nC
I _{RRM}	Reverse recovery current	TOD = SE T (SSS Figure 77)	-	2.1		Α

^{1.} Pulse width limited by safe operating area.

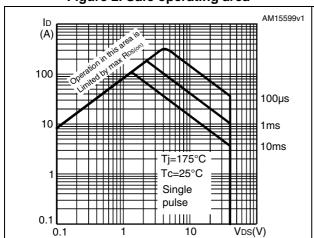
^{2.} Pulsed: pulse duration = 300 μ s, duty cycle 1.5%

Electrical characteristics STU80N4F6

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

Figure 3. Thermal impedance



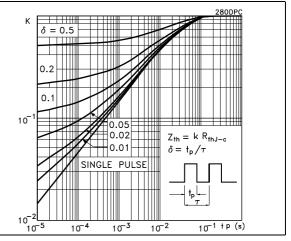
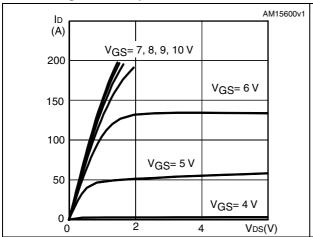


Figure 4. Output characteristics

Figure 5. Transfer characteristics



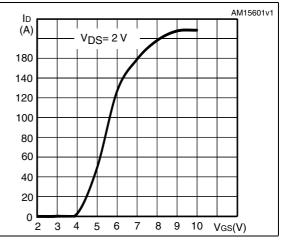
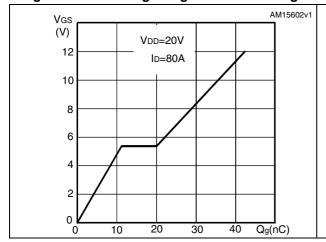
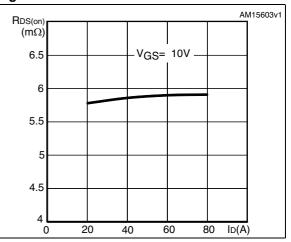


Figure 6. Gate charge vs gate-source voltage

Figure 7. Static drain-source on-resistance

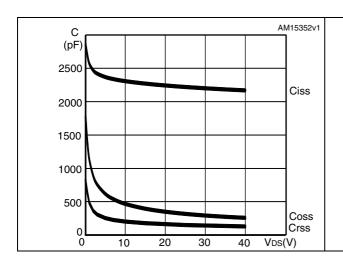




STU80N4F6 Electrical characteristics

Figure 8. Capacitance variations

Figure 9. Drain-source diode forward characteristics



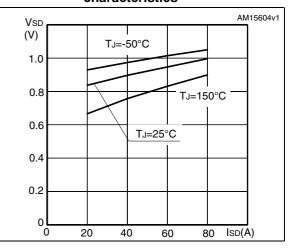
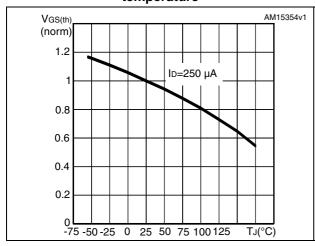


Figure 10. Normalized gate threshold voltage vs temperature

Figure 11. Normalized on-resistance vs temperature



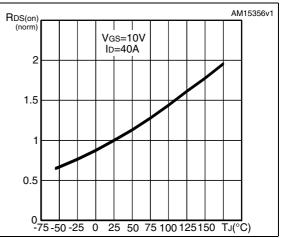
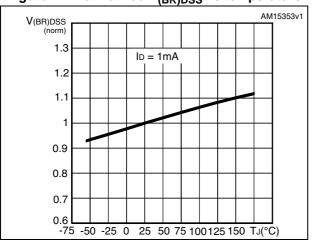


Figure 12. Normalized V_{(BR)DSS} vs temperature



Test circuits STU80N4F6

3 Test circuits

Figure 13. Switching times test circuit for resistive load

Figure 14. Gate charge test circuit

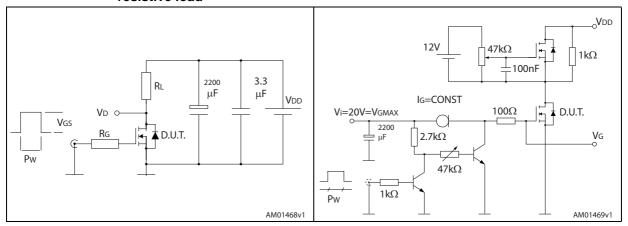


Figure 15. Test circuit for inductive load switching and diode recovery times

Figure 16. Unclamped inductive load test circuit

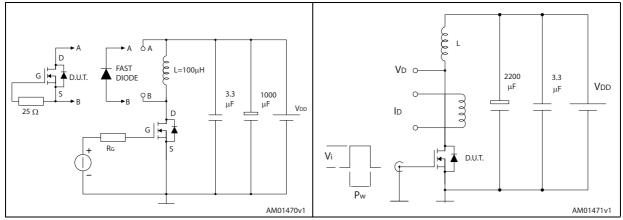
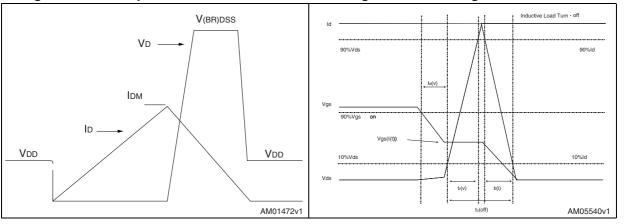


Figure 17. Unclamped inductive waveform

Figure 18. Switching time waveform



4 Package mechanical data

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Eb4 L2 D L1 *b2 (3x)* Н b (3x) V1 -*B5* -e1— 0068771_K

Figure 19. IPAK (TO-251) drawing

Table 8. IPAK (TO-251) mechanical data

DIM		mm.	
DIW	min.	typ.	max.
А	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
С	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
Е	6.40		6.60
е		2.28	
e1	4.40		4.60
Н		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

Revision history STU80N4F6

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
26-Oct-2012	1	Initial release.
01-Mar-2013	2	 Added: IPAK package The part number STI80N4F6 has been moved to a separate datasheet Added: Figure 2, 3, 4, 5, 6, 7 and 9
05-Mar-2013	3	Minor text changesModified: Table 3
28-Feb-2014	4	- The part number STD80N4F6 has been moved to a separate datasheet - Minor text changes

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