50V, 500mA, Low-I_Q 40µA Low-Dropout Linear Regulator with Enable, Reset, Watchdog Functions

DESCRIPTION

The TQL850CSV50 is a high-performance low dropout linear regulator for 5V with input range of 3V to 50V and low quiescent 40µA. TQL850CSV50 provides 2% output voltage accuracy and 500mA maximum driving current and is suitable for automotive or other supply systems. TQL850CSV50 just requires one small ceramic capacitor of 1µF to exhibit fast regulation and good stability. And it shows very low dropout voltage with typical 60mV in 100mA-load and 150mV in 250mA-load. The start operating voltage is 3V which is suitable to cranking condition of automotive system.

The device has an enable function to switch ON and OFF for power dissipation. And other protection functions such as thermal-shutdown and current-limit are against immediate damage.

FEATURES

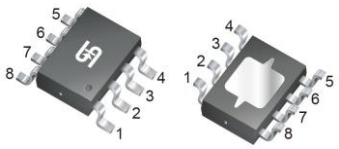
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: -40°C to 125°C
  - Device HBM ESD classification level H2
  - Device CDM ESD classification level C3
- 3V to 50V Input Voltage Range
- 5V Fixed Output Voltage
- Typical 60mV @100mA Low Dropout Voltage
- 500mA Output Current
- Typical 40µA Low Quiescent Current
- Typical ±2% Output Voltage Accuracy
- 1µF Ceramic Output Stable Capacitor
- Output Current Limit
- Over Temperature Protection
- RoHS Compliant
- Halogen-Free according to IEC 61249-2-21

APPLICATION

- Automotive Power Supply Systems
- General Power Supply applications

Pb-Free RoHS COMPLIANT HALOGEN FREE

SOP-8EP

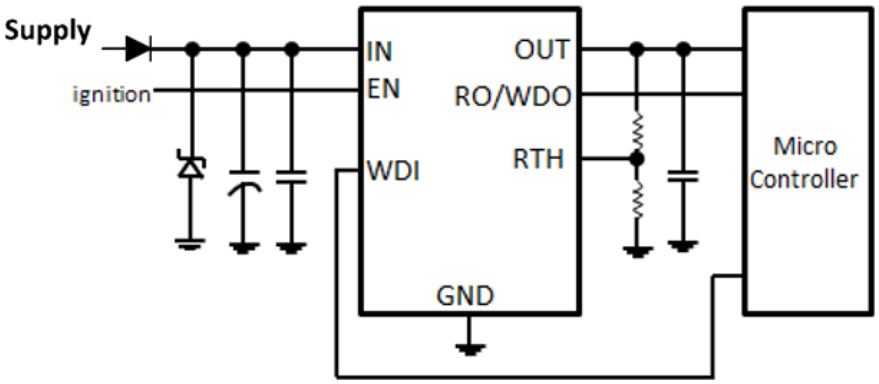


Pin Definition:

1.IN	5. RTH
2.EN	6. WDI
3.RO/WDO	7. NC
4.GND	8. OUT

Notes: MSL 3 (Moisture Sensitivity Level) per J-STD-020

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified) (Note 1)			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Power Supply Pin	V_{IN}	55	V
EN Voltage to GND	V_{EN}	-0.3 to 55	V
OUT/RO/WDO Voltage to GND	$V_{OUT}/V_{RO/WDO}$	-0.3 to 7	V
WDI/RTH Voltage to GND	V_{WDI}/V_{RTH}	-0.3 to 7	V
Junction Temperature Range	T_J	-40 to +150	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C
ESD Rating (Human Body Model) (Note 2)	HBM	±2	kV
ESD Rating (Charged Device Model)	CDM	±1	kV

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**TYP**	**UNIT**
Junction to Case Thermal Resistance	$R_{\Theta JC}$	11	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	43	°C/W

Notes: The thermal data is based on the PCB JESD 51-3 at natural convection on 1s0p board with 1 copper layer (1 x 70μm Cu) and with 300mm^2 heatsink area on PCB

RECOMMENDED OPERATING CONDITIONS (Note 3)			
PARAMETER	**SYMBOL**	**CONDITIONS**	**UNIT**
Power Supply Pin	V_{IN}	$V_{OUT}+V_{dr}$ to 50	V
Extended Power Supply Pin	$V_{IN,ext}$	3 to 50	V
EN Voltage to GND	V_{EN}	0 to 50	V
Output Stable Capacitor	C_{OUT}	≧1	μF
ESR of Output Capacitor	ESR	≦100	Ω
Operating Junction Temperature Range	T_J	-40 to +150	°C
Operating Ambient Temperature Range	T_{OPA}	-40 to +125	°C

ELECTRICAL SPECIFICATIONS (V_{IN} = 13.5V, T_J = -40 to 150°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Supply Voltage						
Output Voltage	0.05mA < I_{OUT} < 500mA 5.95V < V_{IN} < 28V	V_{OUT}	4.9	5	5.1	V
Output Voltage	0.05mA < I_{OUT} < 200mA 5.44V < V_{IN} < 40V	V_{OUT}	4.9	5	5.1	V
Start-up Slew-rate	V_{IN} > 18V/ms C_{OUT} = 1μF 0.5V < V_{OUT} < 4.5V	dV_{OUT}/dt	--	35	--	V/ms
Current Limit	0V < V_{OUT} < 4.8V	I_{lim}	501	650	1100	mA
Load Regulation	I_{OUT} = 0.05 to 500mA V_{IN} = 6V	$\Delta V_{OUT,lo}$	-20	-1.5	+15	mV

ELECTRICAL SPECIFICATIONS (V_{IN} = 13.5V, T_J = -40 to 150°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Supply Voltage						
Line Regulation	V_{IN} = 8 to 32V I_{OUT} = 5mA	$\Delta V_{OUT,li}$	-20	0	20	mV
Dropout Voltage (V_{dr}=V_{IN}-V_{OUT})	I_{OUT} = 250mA	V_{dr}	--	150	425	mV
Dropout Voltage (V_{dr}=V_{IN}-V_{OUT})	I_{OUT} = 100mA	V_{dr}	--	60	170	mV
Power Supply Ripple Rejection	f = 100Hz V = 0.5Vpp	PSRR	--	59	--	dB
Thermal Shutdown Threshold	Note 4	T_{th}	151	--	200	°C
Thermal Shutdown Hysteresis	Note 4	T_{hy}	--	30	--	°C
Current Consumption (PI1=PI2=WDI=GND)						
Standby Current (I_O=I_{IN})	V_{EN} = 0V; T_J≦105°C	$I_{O,st}$	--	1.3	5	μA
Standby Current (I_O=I_{IN})	V_{EN} = 0.4V; T_J≦125°C	$I_{O,st}$	--	--	8	μA
Quiescent Current (I_O=I_{IN}-I_{OUT})	I_{OUT} = 0.05mA, T_J=25°C	I_O	--	40	52	μA
Quiescent Current (I_O=I_{IN}-I_{OUT})	I_{OUT} = 0.05mA, T_J≦125°C	I_O	--	62	77	μA
Enable						
High Level Input Voltage		V_{ENH}	2	--	--	V
Low Level Input Voltage	V_{OUT}≦0.1V	V_{ENL}	--	--	0.8	V
Threshold Hysteresis		V_{ENHy}	100	--	--	mV
EN Input Current	V_{EN} = 3.3V	I_{EN}	--	--	3.5	μA
EN Input Current	V_{EN}≦18V	I_{EN}	--	--	22	μA
EN Pull-down Resistor		R_{EN}	0.95	1.5	2.6	MΩ
Reset						
UVLO Reset Upper Threshold	V_{OUT} increasing	V_{RTH}	4.6	4.7	4.8	V
UVLO Reset Lower Threshold	V_{OUT} decreasing RTH = GND	V_{RTL}	4.5	4.6	4.7	V
UVLO Reset Threshold Hysteresis	RTH = GND	V_{RTHy}	60	100	--	mV
UVLO Reset Headroom (V_{OUT}-V_{RTL})	RTH = GND	V_{RH}	200	400	--	mV
UVLO Adjustment Threshold		V_{RTTH}	1.15	1.2	1.25	V
UVLO Adjustment Range		V_{RTRG}	2.5	--	4.4	V
Reset/Watchdog Output Low Voltage	1V≦V_{OUT}≦V_{RTL} $R_{RO/WDO}$≧5.1kΩ	$V_{RO/WDOL}$	--	0.2	0.4	V
Internal Pull-up Resistor	Connected to OUT	$R_{RO/WDO,int}$	13	20	36	kΩ
External Pull-up Resistor to OUT	1V≦V_{OUT}≦V_{RTL} V_{RO}≦0.4V	$R_{RO/WDO,ext}$	5.1	--	--	kΩ
Reset Delay Time		t_{RD}	6.8	8.5	10.2	ms
Reset Blanking Time	Note 4	t_{RB}	--	7	--	μs

ELECTRICAL SPECIFICATIONS (V_{IN} = 13.5V, T_J = -40 to 150°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Reset						
Internal Reset Reaction Time	Note 4	t_{RR}	--	10	33	μs
Watchdog						
Watchdog Ignore Time		$t_{WDI,i}$	12.8	16	19.2	ms
Watchdog Trigger Time		$t_{WDI,tr}$	38.4	48	57.6	ms
Watchdog Low Time		t_{WDOL}	6.4	8	9.6	ms
WDI High Signal Valid		V_{WDIH}	2.0	--	--	V
WDI Low Signal Valid		V_{WDIL}	--	--	0.8	V
WDI High Pulse Length (Note 4)	$V_{WDI} \geqq V_{WDIH}$	$t_{WDI,ph}$	1	--	--	μs
WDI Low Pulse Length (Note 4)	$V_{WDI} \leqq V_{WDIL}$	$t_{WDI,pl}$	1	--	--	μs
WDI Signal Slew Rate (Note 4)	$V_{WDIL} \leqq V_{WDI} \leqq V_{WDIH}$	dV_{WDI}/dt	1	--	--	V/μs
WDI Input Current	V_{WDI} = 3.3V	I_{WDI}	--	--	3.5	μA
WDI Pull Down Resistor		R_{WDI}	0.9	1.5	2.6	MΩ
WDI Disable Threshold	V_{IN} > 5.95V	$V_{WD,dis}$	1.15	--	1.4	V
Minimum Filter Time By WDI	Note 4	$t_{FWDI,min}$	100	--	--	μs
Maximum Filter Time By WDI	Note 4	$t_{FWDI,max}$	--	--	500	μs

Note:

1. Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.
2. Devices are ESD sensitive. Handing precaution recommended.
3. The device is not guaranteed to function outside its operating conditions.
4. Guaranteed by design.

ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TQL850CSV50 RLG	SOP-8EP	2,500pcs / 13” Reel

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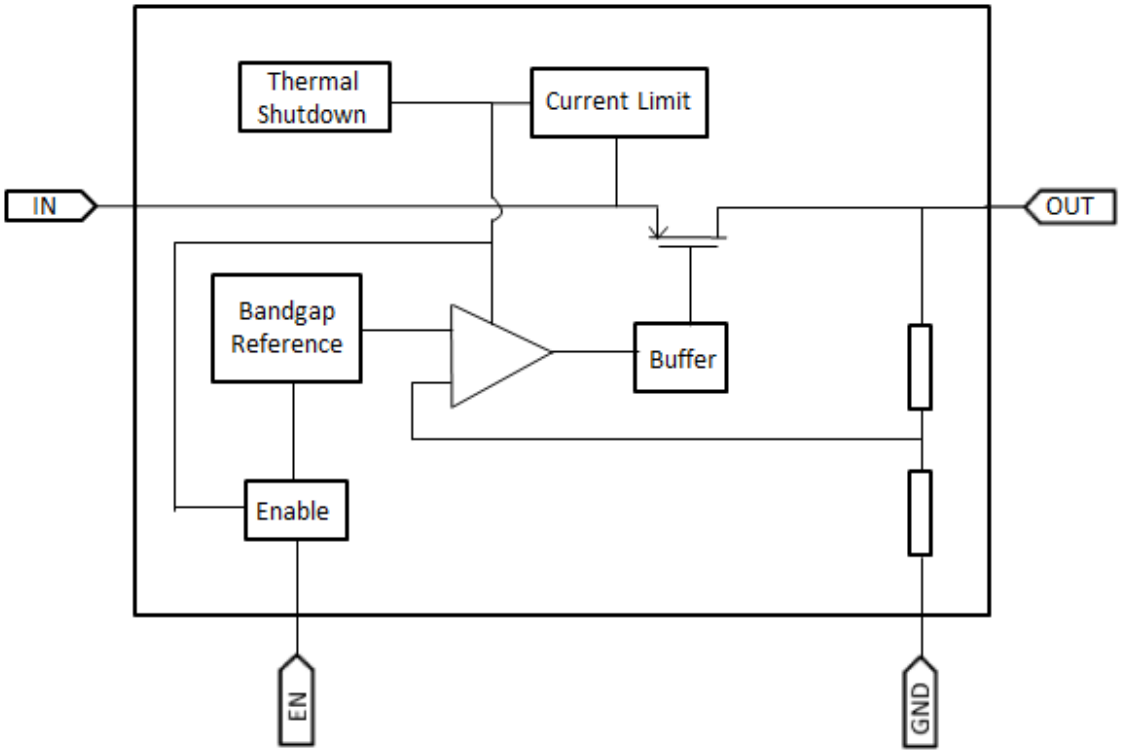
BLOCK DIAGRAM



PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	IN	Power supply pin for system
2	EN	Enable system function
3	RO/WDO	Reset and watchdog output
4	GND	Ground
5	RTH	Reset threshold adjustment
6	WDI	Watchdog monitor input
7	NC	No connect
8	OUT	Output supply voltage
Pad	--	Connect to GND

APPLICATION INFORMATION

TQL850CSV50 is a high-performance low dropout voltage regulator. The device operates with a wide input voltage from 3V to 50V and up to 500mA of output current. It also provides a high accuracy output voltage for ±2% in all the load and line regulation.

Reset

The TQL850CSV50 is monitored by Reset system including Power-ON Delayed Reset, Under-Voltage Reset, and Reset Threshold Adjustment. When reset is activated, the RO/WDO pin is low.

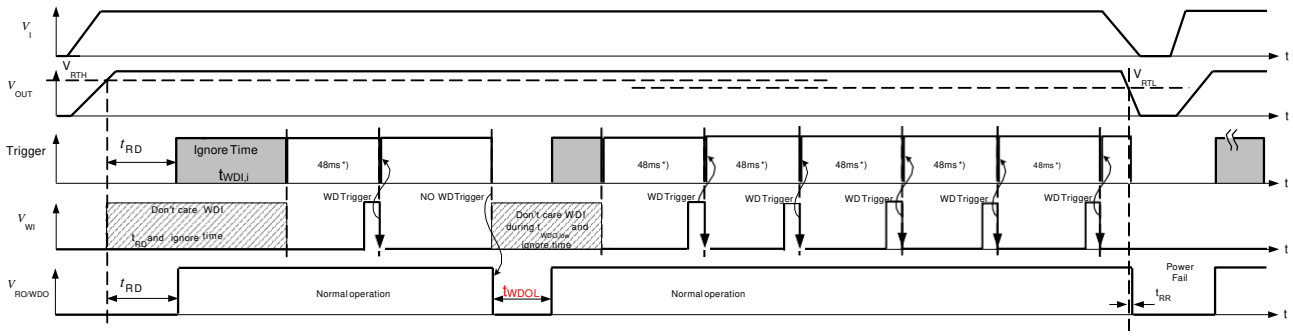
- Power-ON Delayed Reset
  When device starts up, the RO/WDO pin delays to become “High” in Power-ON Delayed Time (t_{RD}) without reset issue.
- Under-Voltage Reset
  When the output supply voltage drops below UVLO Reset Lower Threshold (V_{RTL}), the RO/WDO switches from “High” to “Low”. The RO/WDO pin is an open collector output with an internal pull-up resistor.
- Reset Threshold Adjustment
  The UVLO Reset Lower Threshold can be adjusted. If the RTH pin connects to GND, the threshold voltage is default value (V_{RTL}). We can take two resistors (R_{th1}, R_{th2}) to adjust under-voltage threshold. The R_{th1} is connected between OUT pin and RTH pin and R_{th2} is connected between RTH and GND. The reminder is taking proper resistance for current sourcing. The new threshold voltage is calculated as follows:

$$V_{RTL,new} = V_{RTTH} \times (R_{th1} + R_{th2}) / R_{th2}$$

- **$V_{RTL,new}$:** Desired switching threshold
- **R_{th1}, R_{th2} :** External divider resistors
- **V_{RTTH} :** Reset adjust switching threshold

Watchdog

The TQL850CSV50 has the watchdog function with fixed watchdog timing to monitor microcontroller process. The device monitors the period clock-pulse provided by Microcontroller at WDI pin in a certain timing (Watchdog Trigger Time, $t_{WDI,tr}$). If there is no signal in Watchdog Trigger Time, the RO/WDO pin becomes “Low” in a certain time (Watchdog Low Time, t_{WDOL}). After that, the RO/WDO pin returns to “High” and keep watching the WDI signal repeatedly. The RO/WDO pin is an open collector output with an internal pull-up resistor.
The Watchdog function is inactivated by WDI pin. While the WDI voltage is in 1.15V to 1.4V, the Watchdog function is disable.



Typical Watchdog Timing Diagram, Watchdog and Reset Modes

APPLICATION INFORMATION (CONTINUE)

Enable

The EN pin is high voltage tolerant pin. High input enables the device ON and low is disable which can be connected to microcontroller or digital control system. It can be connected to input power pin directly.

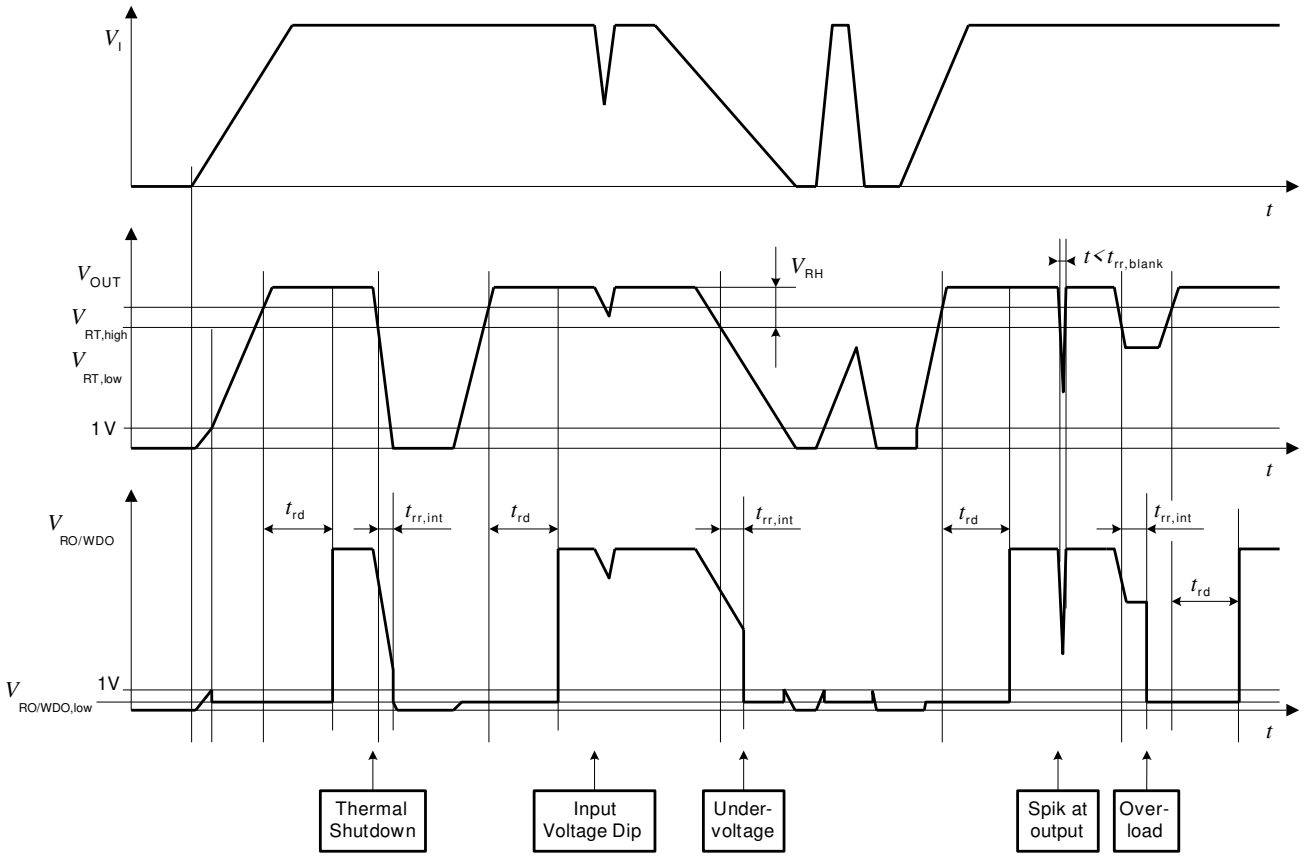
Thermal Shutdown (TSD)

Internal 160°C comparator will trigger temperature protection (TSD). TSD will shut down system, until internal temperature back to 130°C.

Current Limit

The TQL850CSV50 features Current Limit function to protect device from damage by excessive power dissipation such as OUT shorted to GND. It limits output current to maintain power dissipation in the safe region.

Typical Timing Diagram Reset



TYPICAL OPERATING CHARACTERISTICS

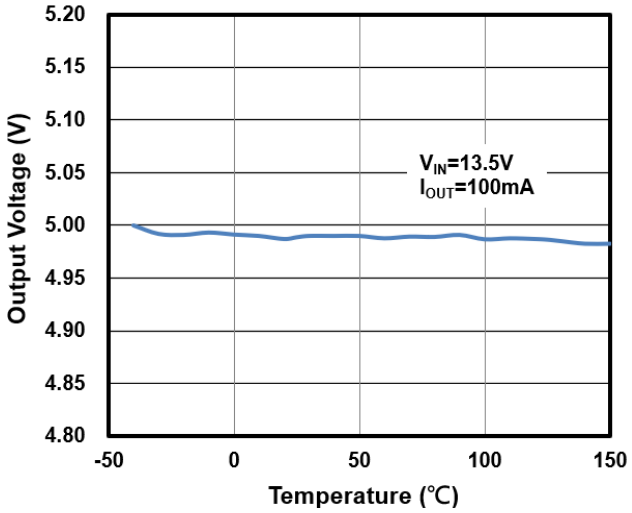


Figure 1. Output Voltage vs. Junction Temperature

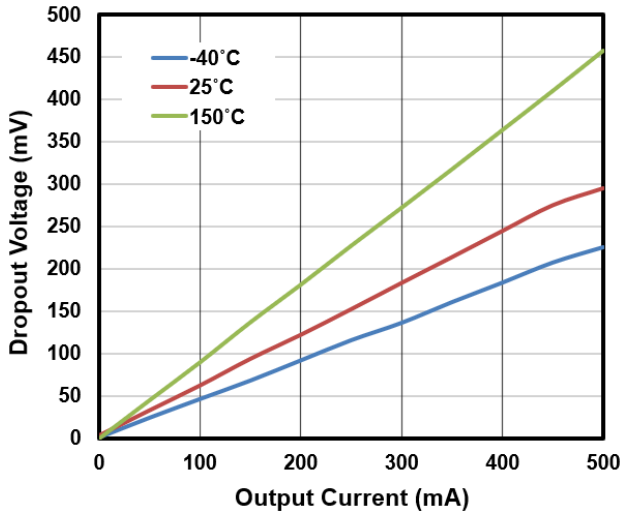


Figure 2. Dropout Voltage vs. Output Current

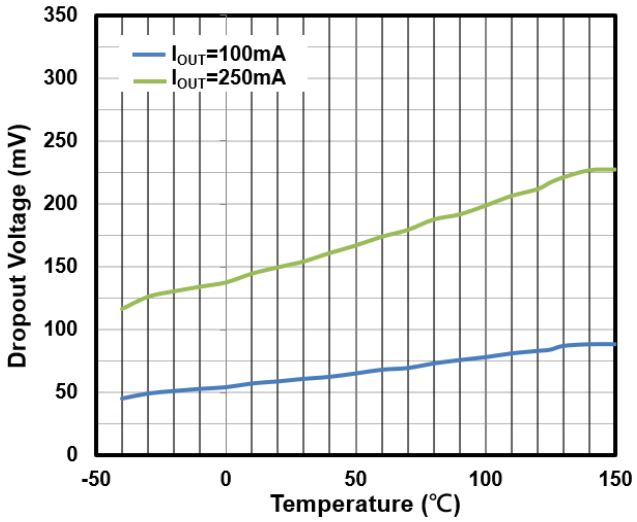


Figure 3. Dropout Voltage vs. Junction Temperature

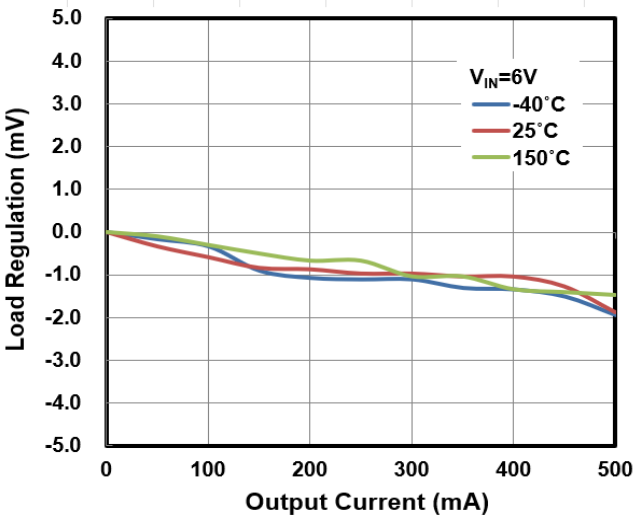


Figure 4. Load Regulation vs. Output Current

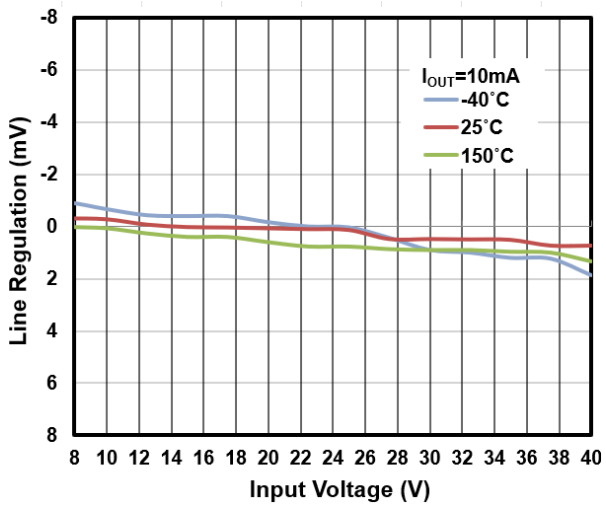


Figure 5. Line Regulation vs. Input Voltage

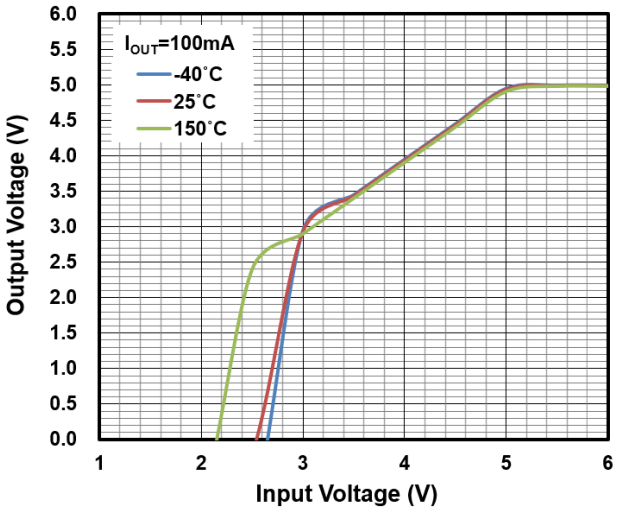


Figure 6. Output Voltage vs. Input Voltage

TYPICAL OPERATING CHARACTERISTICS (CONTINUE)

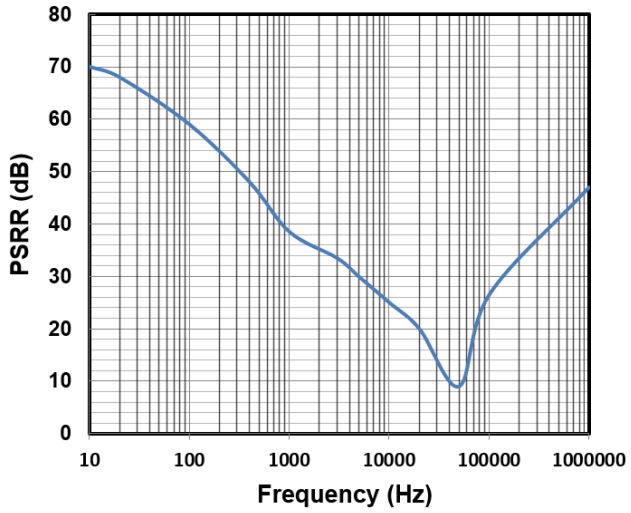


Figure 7. Ripple Rejection vs. Frequency

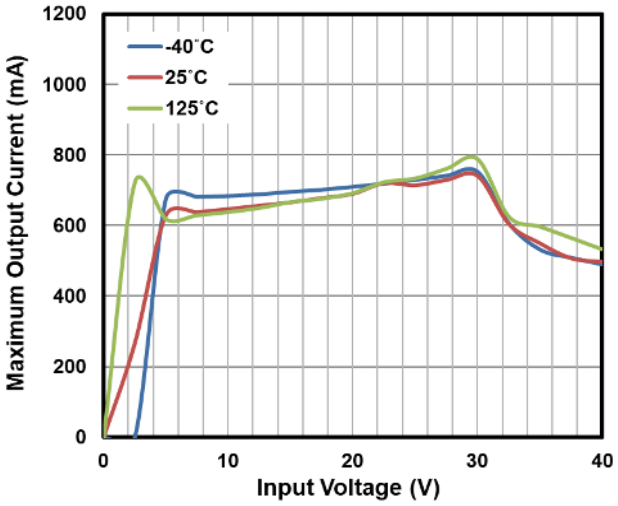


Figure 8. Output Current vs. Input Voltage

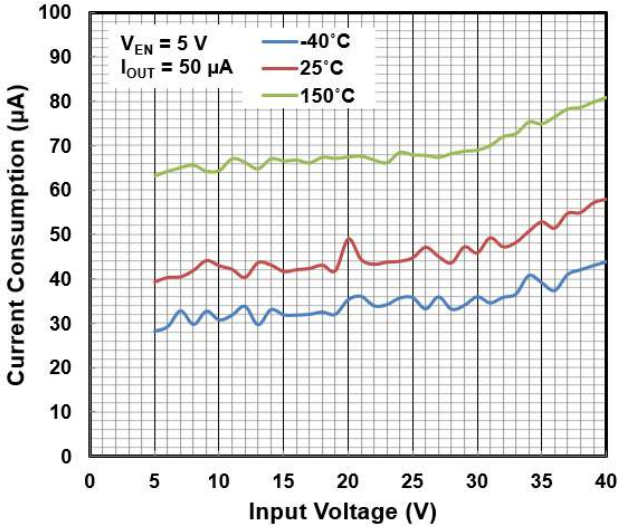


Figure 9. Current Consumption vs. Input Voltage

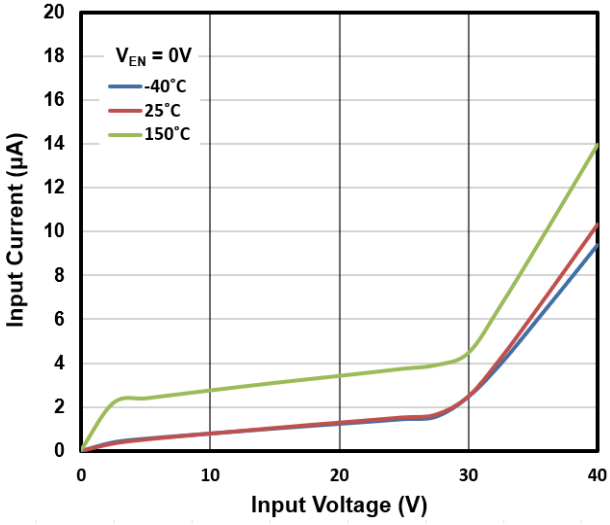


Figure 10. Input Current vs. Input Voltage

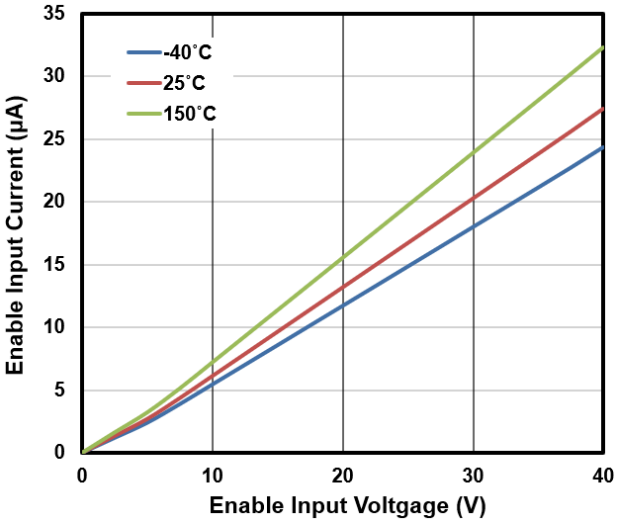


Figure 11. Enabled Input Current vs. Enabled Input Voltage

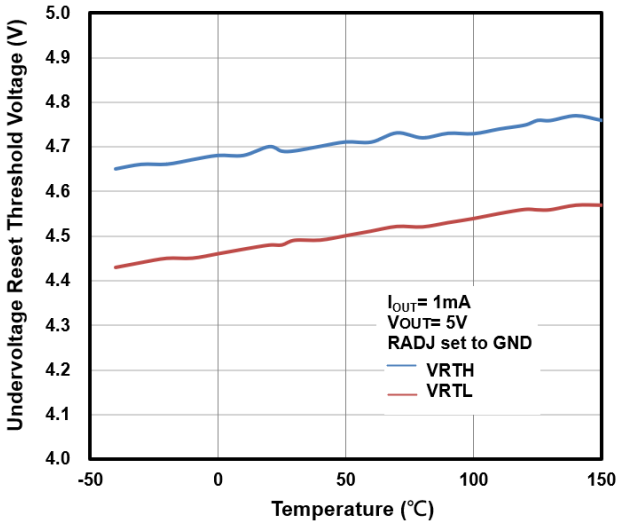


Figure 12. Undervoltage Reset Threshold vs. Junction Temperature

TYPICAL OPERATING CHARACTERISTICS (CONTINUE)

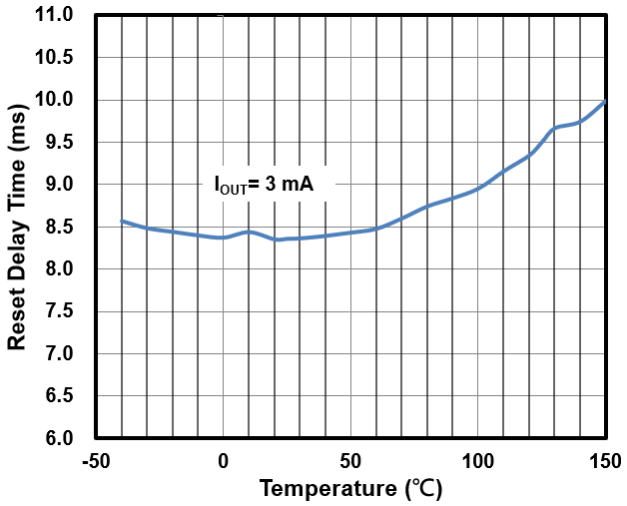


Figure 13. Power On Reset Delay Time vs. Junction Temperature

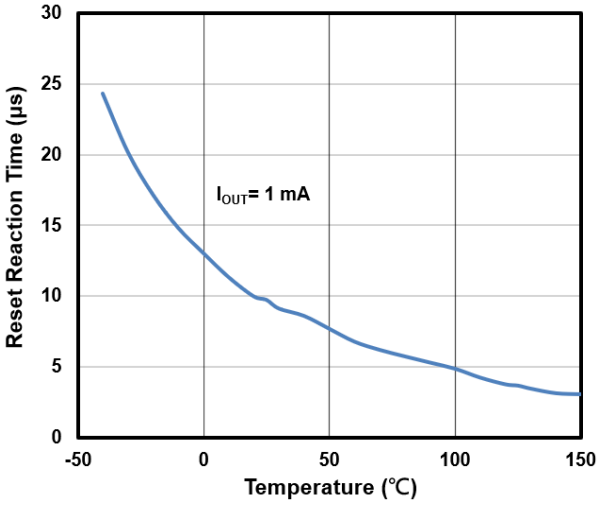


Figure 14. Internal Reset Reaction Time vs. Junction Temperature

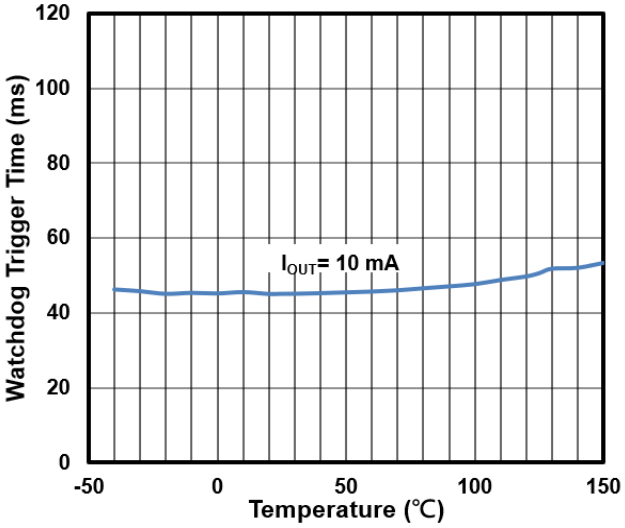


Figure 15. Watchdog Trigger Time vs. Junction Temperature

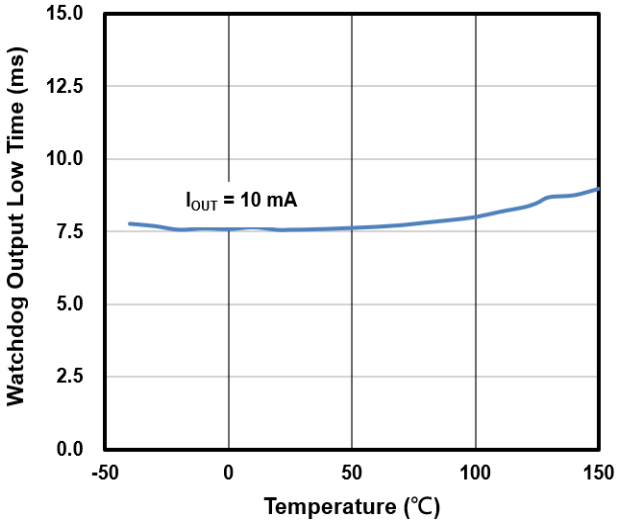


Figure 16. Watchdog Output Low Time vs. Junction Temperature

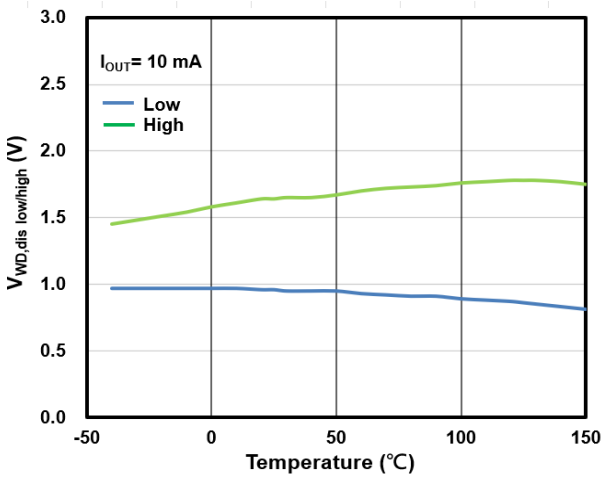


Figure 15. Watchdog Disable Threshold vs. Junction Temperature

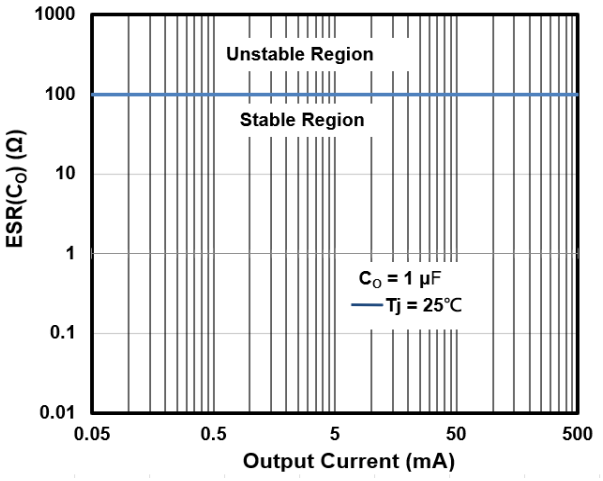


Figure 16. Output Capacitor Series Resistor ESR(C_O) vs. Output Current

TYPICAL OPERATING CHARACTERISTICS (CONTINUE)

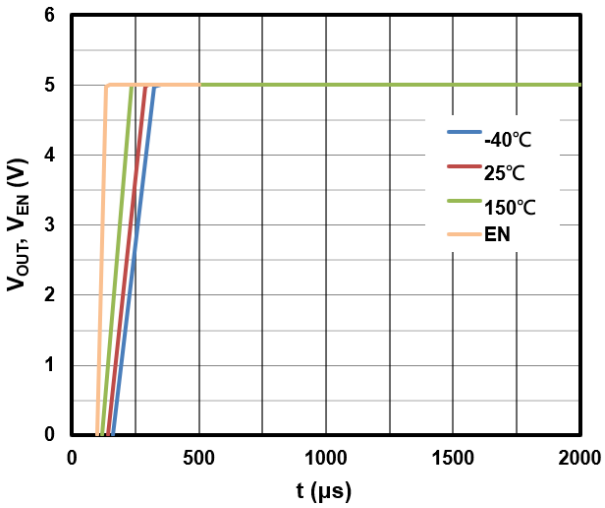
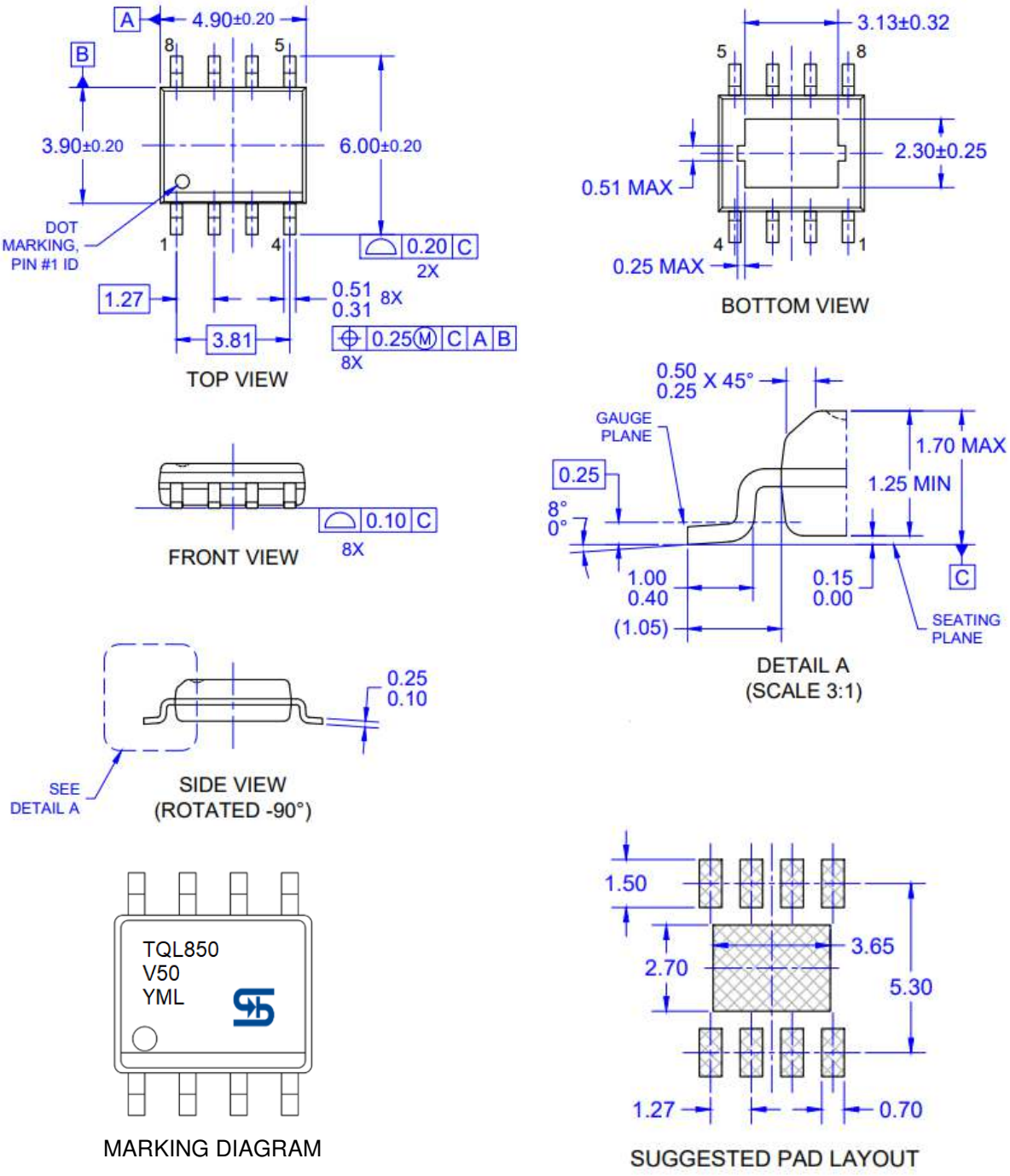


Figure 17. Output Voltage vs. time (EN switched ON)

PACKAGE OUTLINE DIMENSIONS

SOP-8EP



Y = Year Code

M = Month Code for Halogen Free Product

O	=Jan	**P**	=Feb	**Q**	=Mar	**R**	=Apr
S	=May	**T**	=Jun	**U**	=Jul	**V**	=Aug
W	=Sep	**X**	=Oct	**Y**	=Nov	**Z**	=Dec

L = Lot Code (1~9, A~Z)

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEDEC MS-012, ISSUE G, VARIATION BA.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO REF: HQ2SD07-030 REV A.

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