General Description

The ICS83PN161i is LVPECL output synthesizer designed for converting forward-error correction (FEC) clock frequencies in 10 GB Ethernet LAN/WAN transport applications. The device is optimized for an input frequency of 156.25MHz and supports four FEC rate conversions: 33/32, 255/237, 255/238 and 235/236. The conversion rate is pin-selectable and one of four rates are supported at a time. In the default configuration, an input clock of 156.25MHz is converted to an output clock of 168.8294492MHz (255/236).

The device uses IDT's fourth Generation of FemtoClock® NG technology to deliver low phase noise clocks combined with a low power consumption. The RMS phase jitter at 168.8294492MHz output frequency is 0.533ps (12kHz-20MHz integration range).

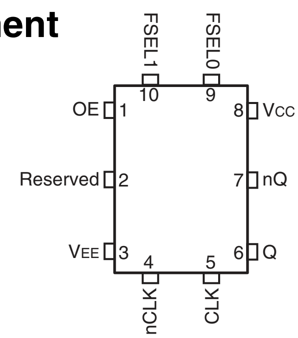
Features

- Fourth Generation FemtoClock® Next Generation (NG) technology
- Footprint compatible with 5mm x 7mm differential oscillators
- 10 Gb Ethernet LAN/WAN FEC clock converter
- Supports 33/32, 255/237, 255/238, 255/236 rate conversions
- Optimized for an input clock frequency of 156.25MHz
- One differential LVPECL output pair
- CLK, nCLK input pair can accept the following levels: HCSL, LVDS, LVPECL, LVHSTL and SSTL
- Output frequency range: 161.1328125MHz – 168.8294492MHz
- VCO range: 2.0GHz – 2.5GHz
- Cycle-to-cycle jitter: 18ps (typical)
- RMS phase jitter, 12kHz – 20MHz: 0.533ps (typical)
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Frequency Select Table

FSEL[1:0]	Input	Output Frequency (MHz)	FEC Rate
0 0	156.25	161.1328125	33/32
0 1	156.25	168.1170886	255/237
1 0	156.25	167.4107143	255/238
1 1 (default)	156.25	168.8294492	255/236

Pin Assignment



ICS83PN161I

10-Lead VFQFN
5mm x 7mm x 1mm package body
K Package
Top View

Block Diagram

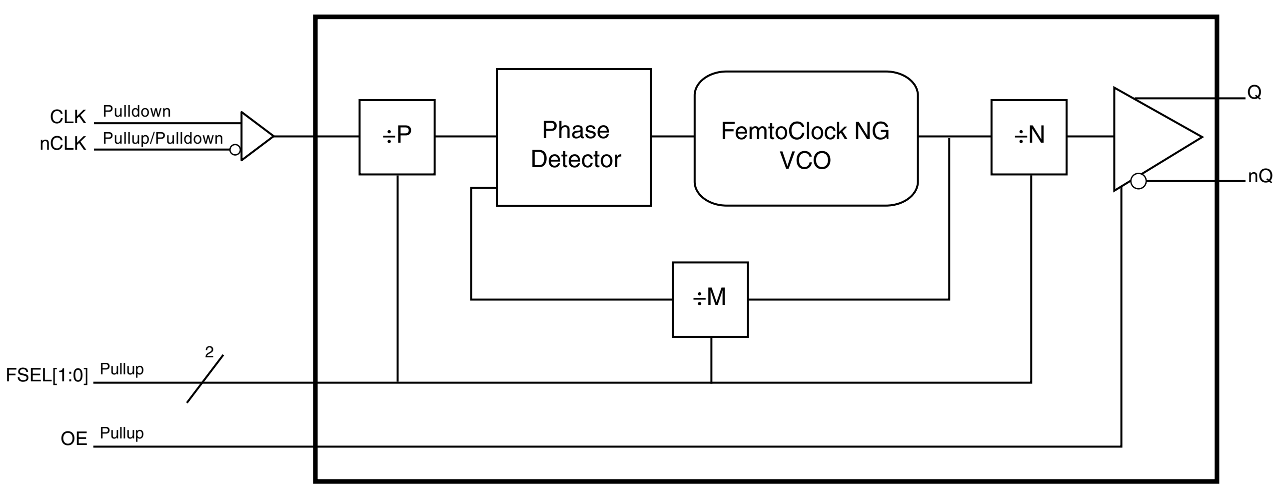


Table 1. Pin Descriptions

Number	Name	Type		Description
1	OE	Input	Pullup	Output enable. External pullup required for normal operation. LVCMOS/LVTTL interface levels.
2	Reserved	Reserve		Reserved pin. Do not connect.
3	V_{EE}	Power		Negative supply pin.
4	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating
5	CLK	Input	Pulldown	Non-inverting differential clock input.
6, 7	Q, nQ	Output		Differential output pair. LVPECL interface levels.
8	V_{CC}	Power		Power supply pin.
9	FSEL0	Input	Pullup	Feedback control inputs. Sets the output divider value to one of four values. LVCMOS/LVTTL interface levels. See *Frequency Select Table* on page 1.
10	FSEL1	Input	Pullup	Feedback control inputs. Sets the output divider value to one of four values. LVCMOS/LVTTL interface levels. See *Frequency Select Table* on page 1.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			3.5		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Table

Table 3. P, M, N Divider Function Table

FSEL[1:0]	P Divider	M Divider	N Divider	Input Frequency (MHz)	Output Frequency (MHz)
0 0	÷2	÷28.87500000	÷14	156.25	161.1328125
0 1	÷2	÷30.12658228	÷14	156.25	168.1170886
1 0	÷2	÷25.71428571	÷12	156.25	167.4107143
1 1 (default)	÷2	÷25.93220339	÷12	156.25	168.8294492

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	3.63V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	39.2°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				189	mA

Table 4B. Power Supply DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				182	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.465V	2		V_{CC} + 0.3	V
			V_{CC} = 2.625V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.465V	-0.3		0.8	V
			V_{CC} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	FSEL[1:0]	V_{CC} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	FSEL[1:0]	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

Table 4D. Differential DC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

<table>
<tr><th>Symbol</th><th colspan="2">Parameter</th><th>Test Conditions</th><th>Minimum</th><th>Typical</th><th>Maximum</th><th>Units</th></tr>
<tr><td>I_{IH}</td><td>Input High Current</td><td>CLK, nCLK</td><td>V_{CC} = V_{IN} = 3.465V or 2.625V</td><td></td><td></td><td>150</td><td>µA</td></tr>
<tr><td rowspan="2">I_{IL}</td><td rowspan="2">Input Low Current</td><td>CLK</td><td>V_{IN} = 0V,
V_{CC} = 3.465V or 2.625V</td><td>-5</td><td></td><td></td><td>µA</td></tr>
<tr><td>nCLK</td><td>V_{IN} = 0V,
V_{CC} = 3.465V or 2.625V</td><td>-150</td><td></td><td></td><td>µA</td></tr>
<tr><td>V_{PP}</td><td colspan="2">Peak-to-Peak Voltage</td><td></td><td>0.15</td><td></td><td>1.3</td><td>V</td></tr>
<tr><td>V_{CMR}</td><td colspan="2">Common Mode Input Voltage; NOTE 1</td><td></td><td>V_{EE}</td><td></td><td>V_{CC} – 0.85</td><td>V</td></tr>
</table>

NOTE 1: Common mode input voltage is defined as the crossing point.

Table 4E. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.8	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to V_{CC} – 2V.

AC Electrical Characteristics

Table 5A. AC Characteristics, V_{cc} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		161.1328125		168.8294492	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1			18	30	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	161.1328125MHz, Integration Range: 12kHz – 20MHz		0.533	0.69	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	150		450	ps
odc	Output Duty Cycle		49		51	%

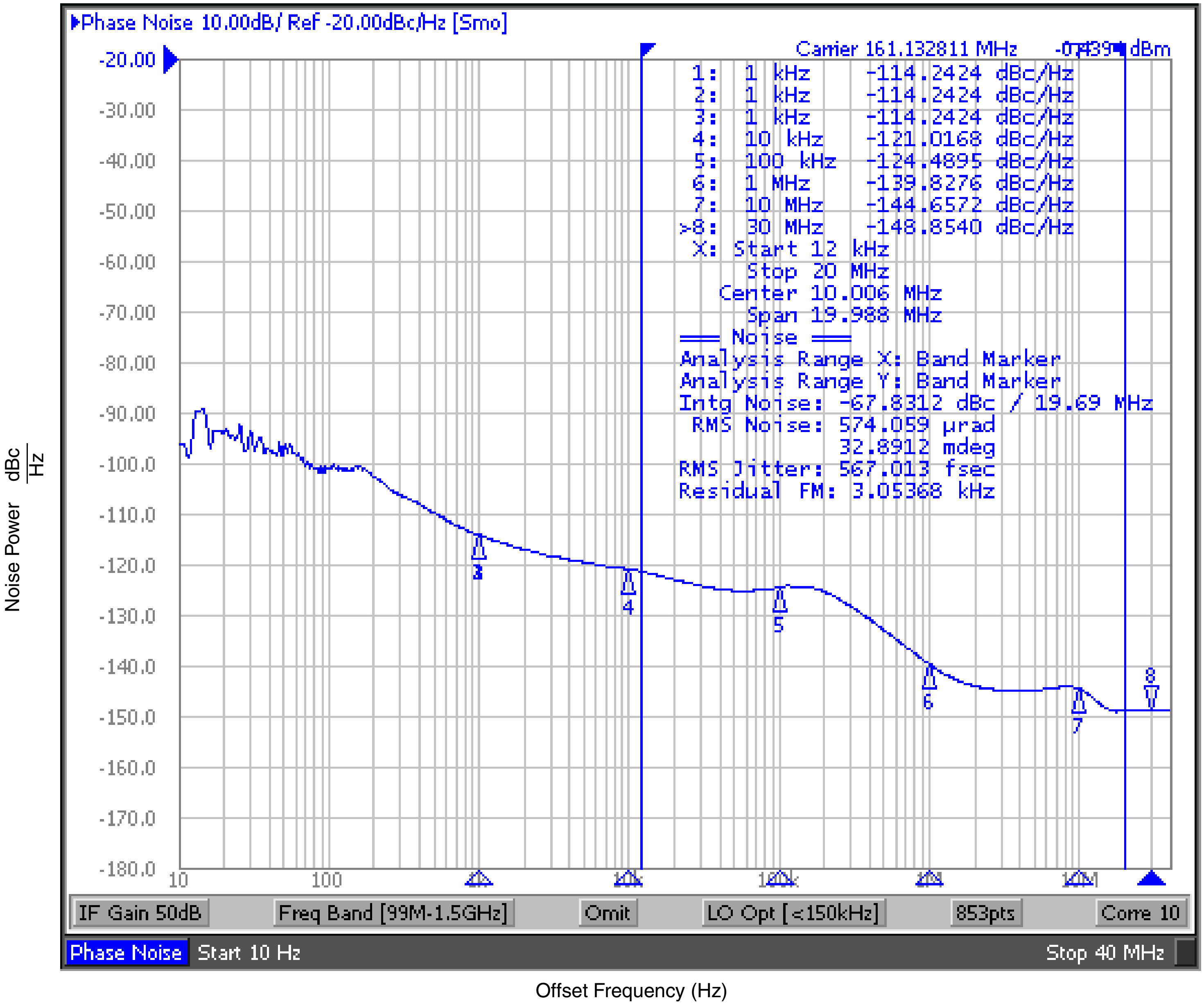
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Refer to the Phase Noise plot.

Table 5B. AC Characteristics, V_{cc} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

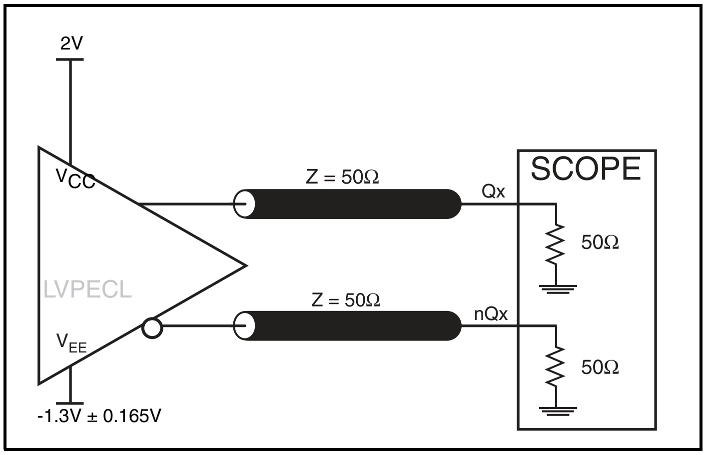
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		161.1328125		168.8294492	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1			18	30	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	161.1328125MHz, Integration Range: 12kHz – 20MHz		0.533	0.69	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		500	ps
odc	Output Duty Cycle		49		51	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Refer to the Phase Noise plot.

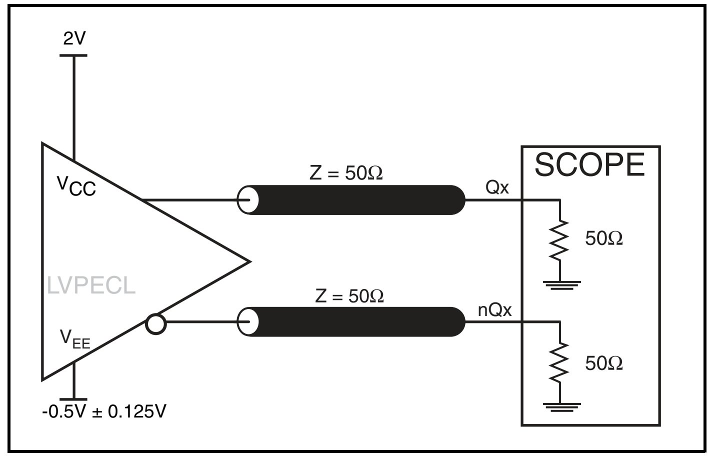
Typical Phase Noise at 161.1328125MHz



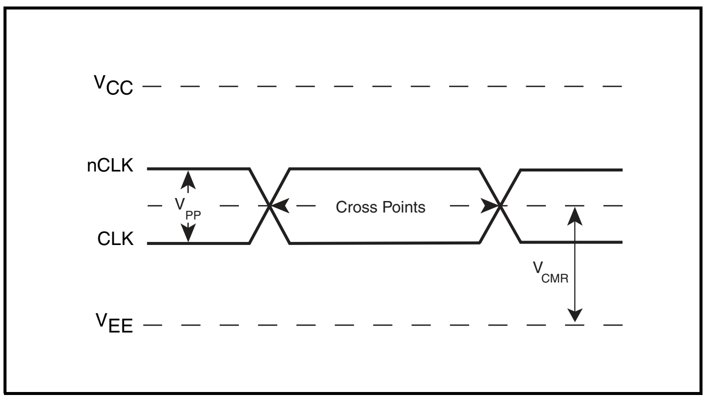
Parameter Measurement Information



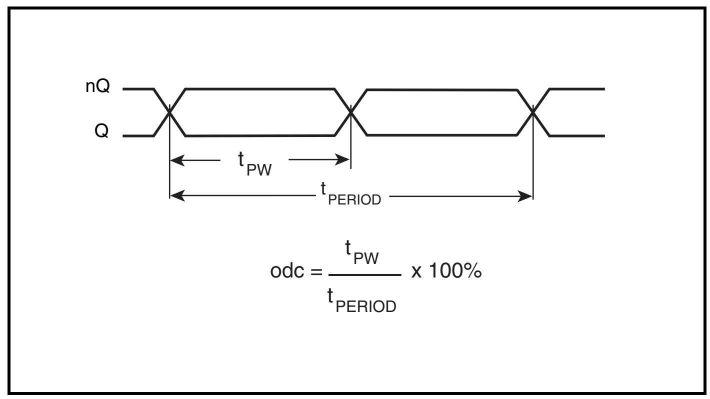
3.3V LVPECL Output Load AC Test Circuit



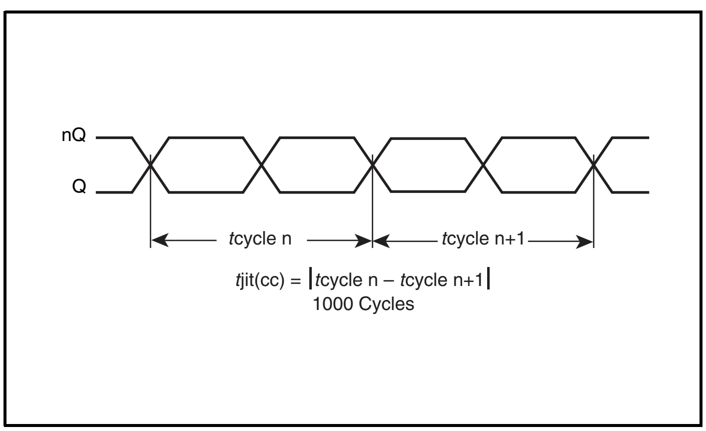
2.5V LVPECL Output Load AC Test Circuit



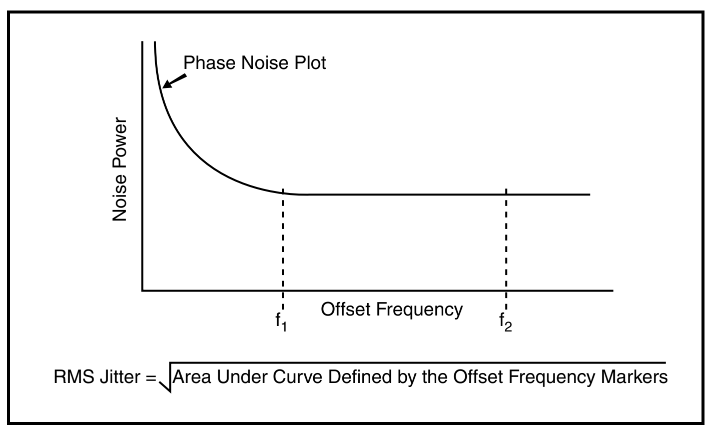
Differential Input Level



Output Duty Cycle/Pulse Width/Period

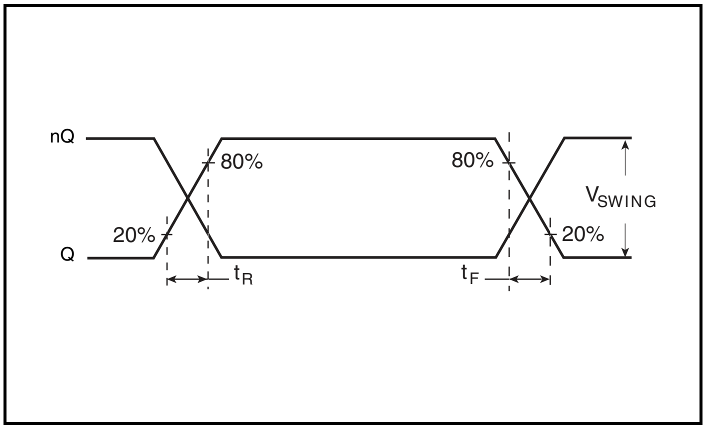


Cycle-to-Cycle Jitter



RMS Phase Jitter

Parameter Measurement Information, continued



Output Rise/Fall Time

Application Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

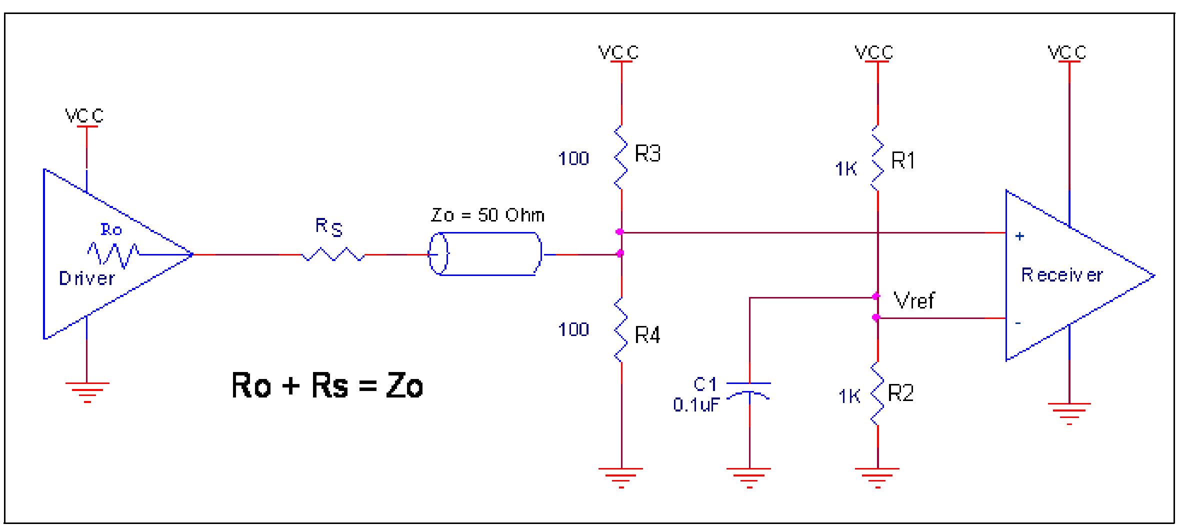


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

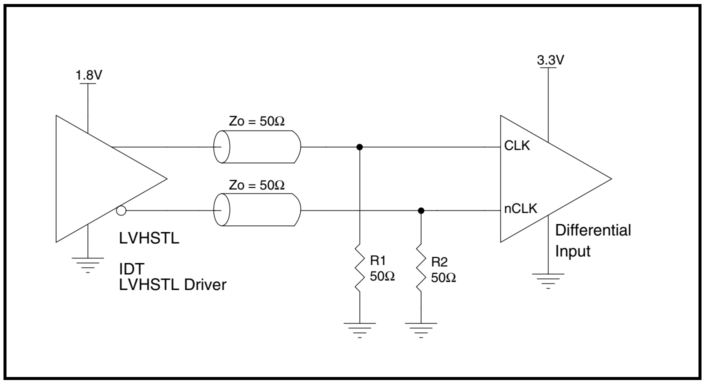


Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

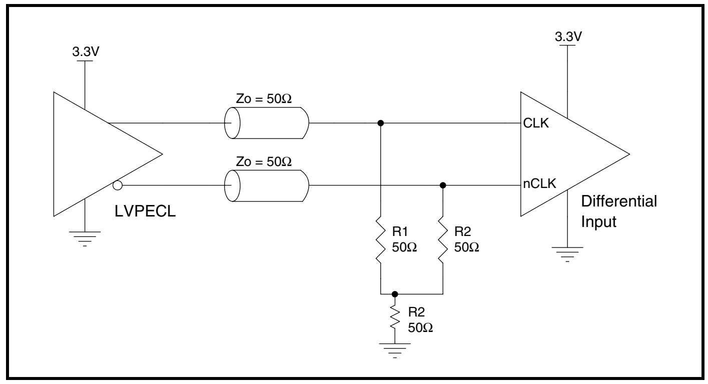


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

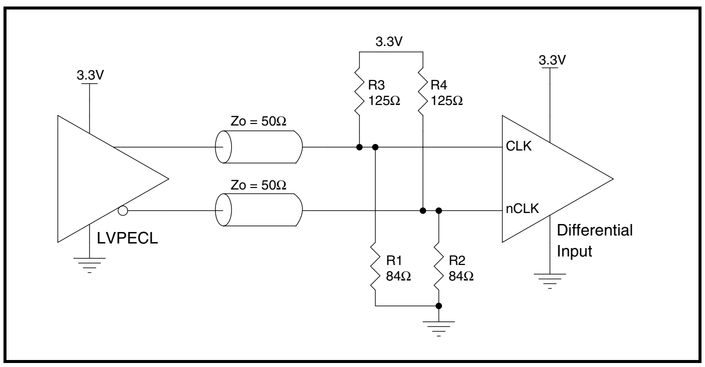


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

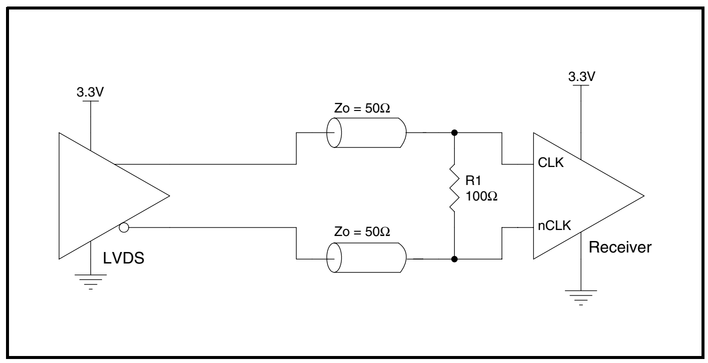


Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

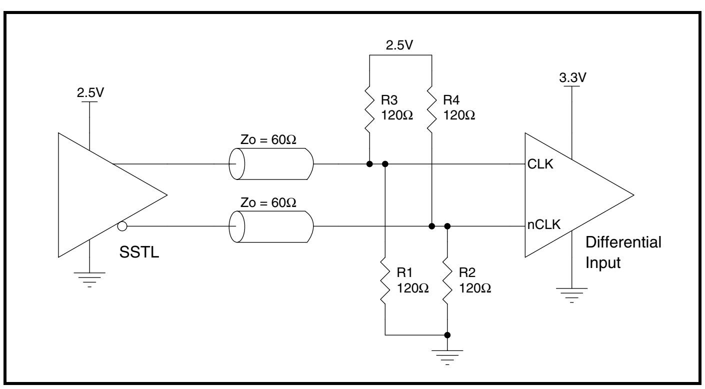


Figure 2E. CLK/nCLK Input Driven by a 2.5V SSTL Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

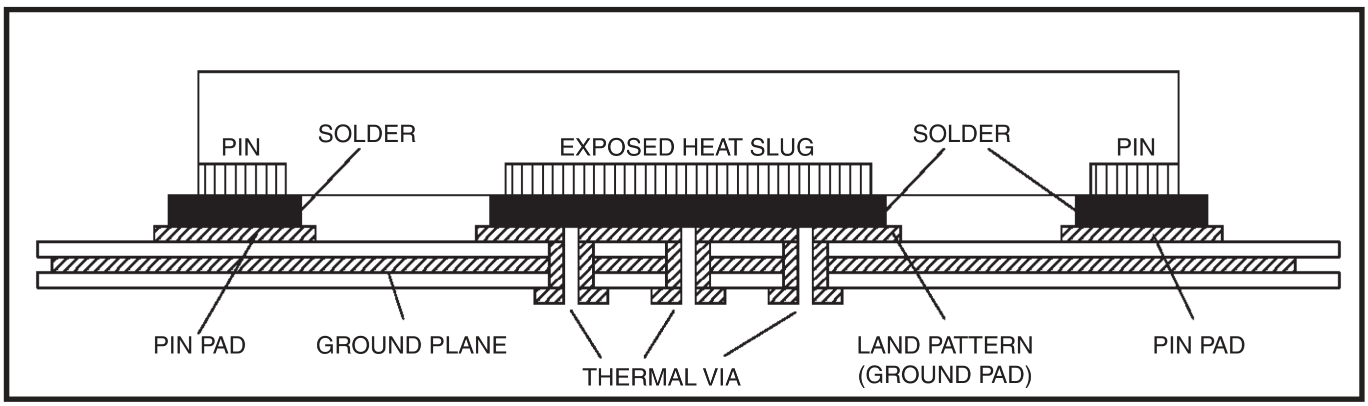


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

For the control pins that have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible signals. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

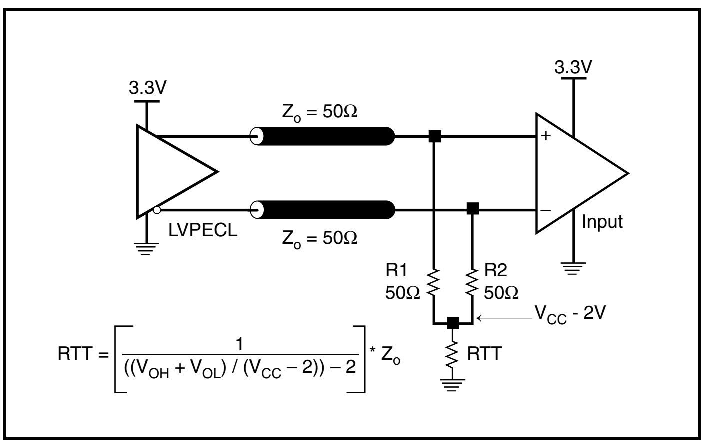


Figure 4A. 3.3V LVPECL Output Termination

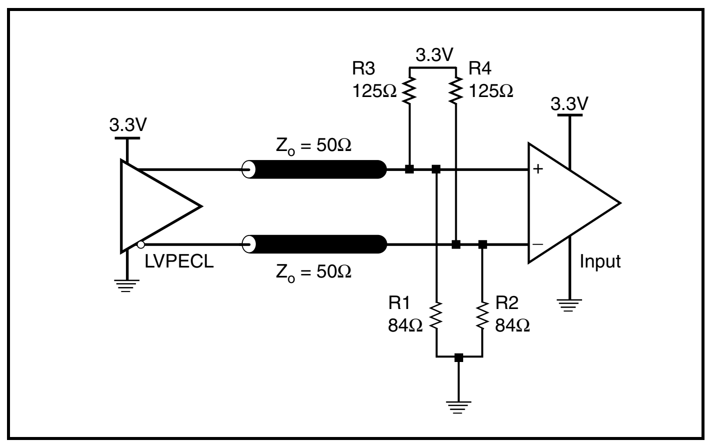


Figure 4B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

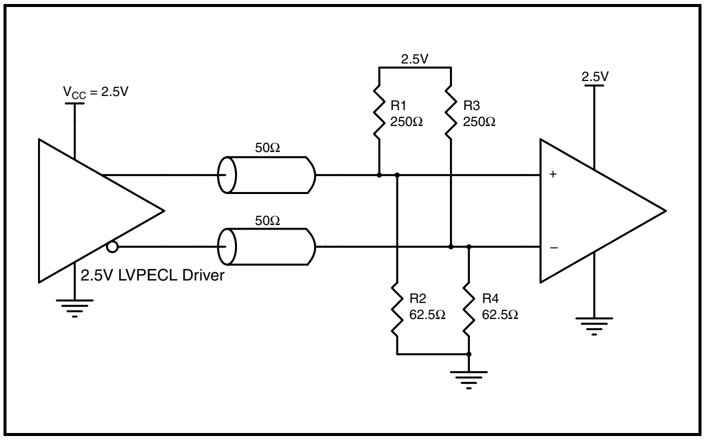


Figure 5A. 2.5V LVPECL Driver Termination Example

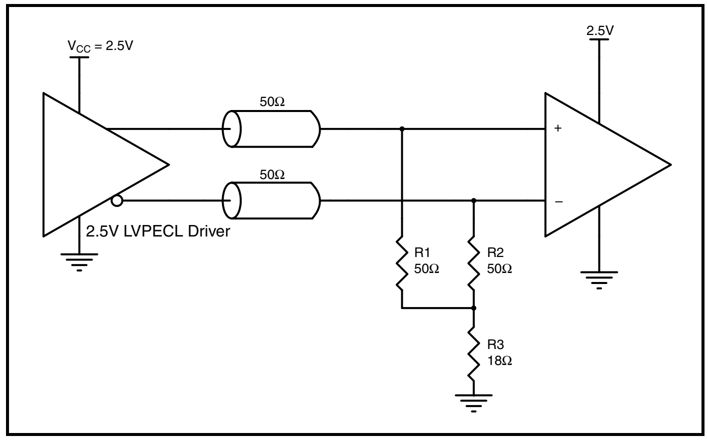


Figure 5B. 2.5V LVPECL Driver Termination Example

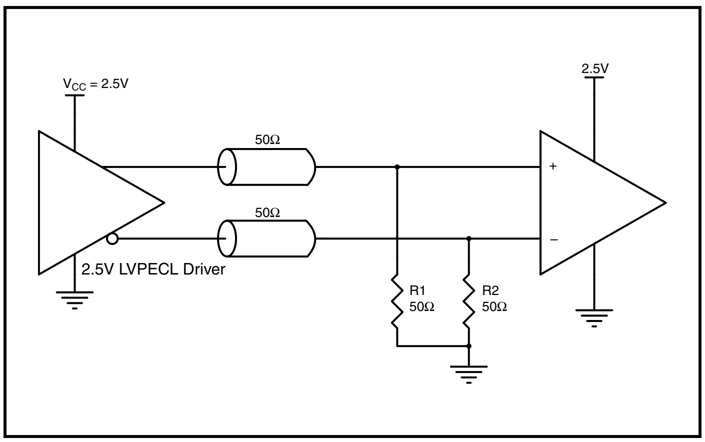


Figure 5C. 2.5V LVPECL Driver Termination Example

Schematic Example

Figure 6 shows an example of ICS83PN161I application schematic. In this example, the device is operated at V_{CC} = 3.3V. The input is driven by either a 3.3V LVPECL or LVDS driver. Two examples of LVPECL termination are shown in this schematic. Additional termination approaches are shown in the *LVPECL Termination Application NOTE.* The decoupling capacitors should be located as close as possible to the power pin.

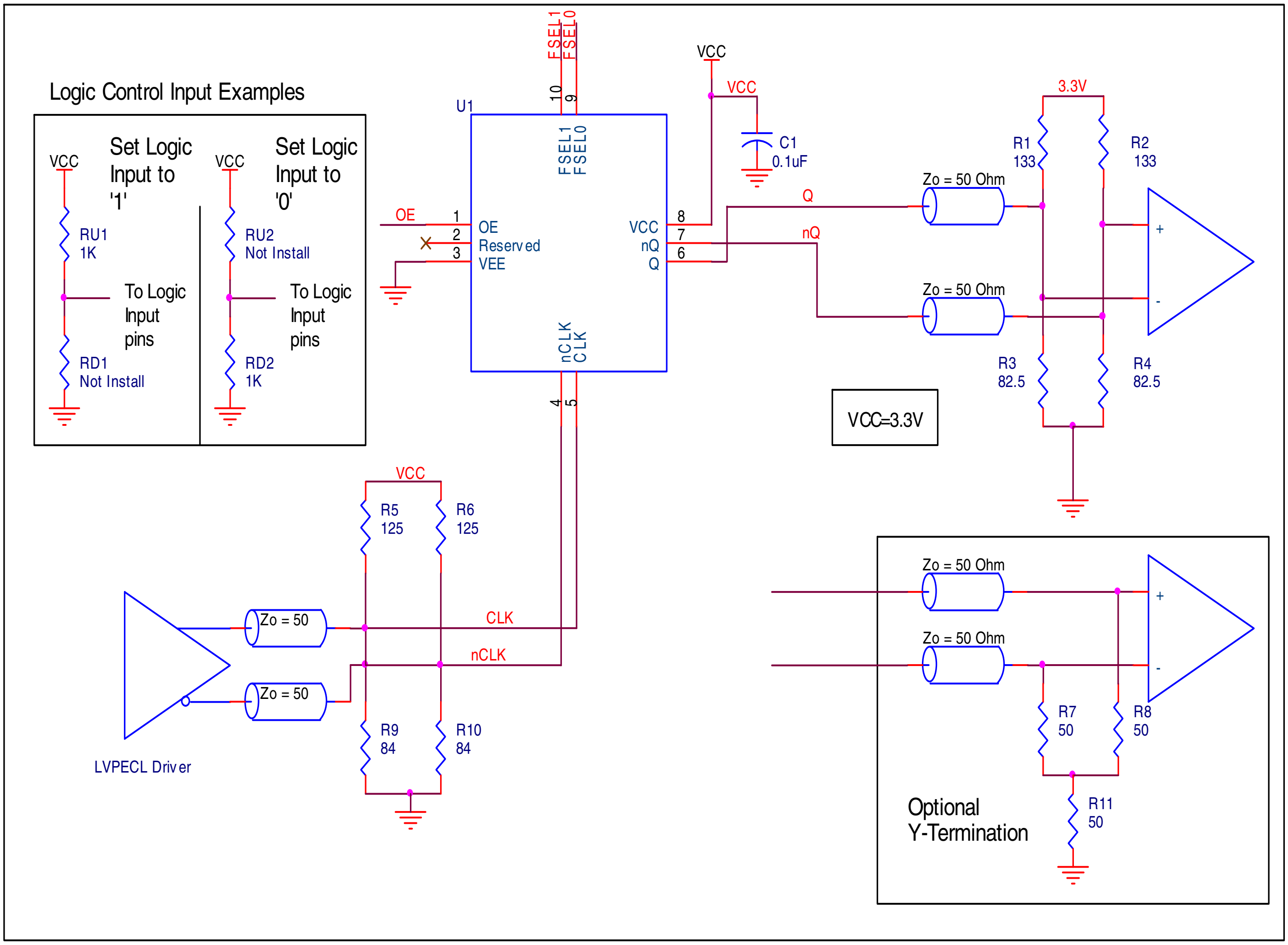


Figure 6. ICS83PN161I Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS83PN161I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS83PN161I is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 189mA = **654.885mW**
- Power (outputs)$_{MAX}$ = **32mW/Loaded Output pair**

Total Power$_{\_MAX}$ (3.3V, with all outputs switching) = 654.885mW + 32mW = **686.68mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 39.2°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.687W * 39.2°C/W = 111.9°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 10 Lead VFQFN, Forced Convection

θ_{JA} by Velocity	
Meters per Second	**0**
Multi-Layer PCB, JEDEC Standard Test Boards	39.2°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

The LVPECL output driver circuit and termination are shown in *Figure 7.*

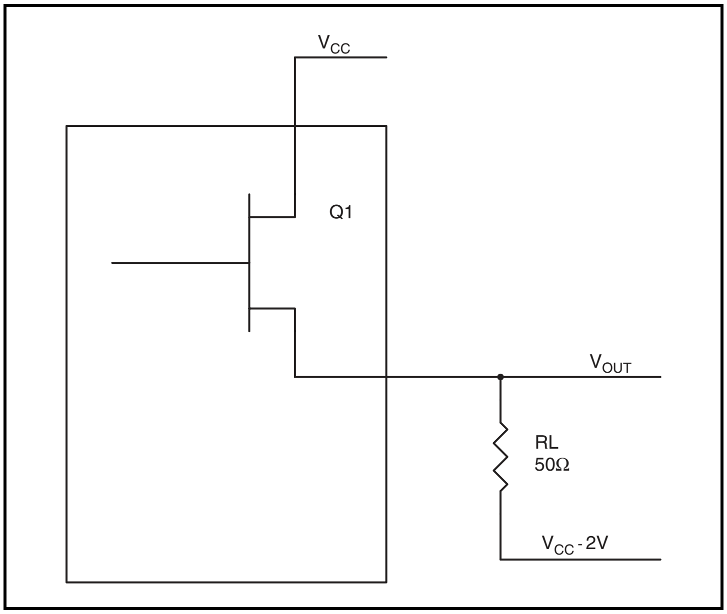


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} – 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.8V}$
  $(V_{CC\_MAX} – V_{OH\_MAX}) = \mathbf{0.8V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.6V}$
  $(V_{CC\_MAX} – V_{OL\_MAX}) = \mathbf{1.6V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – 0.8V)/50\Omega] * 0.8V = \mathbf{19.2mW}$

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – 1.6V)/50\Omega] * 1.6V = \mathbf{12.8mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **32mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 10 Lead VFQFN

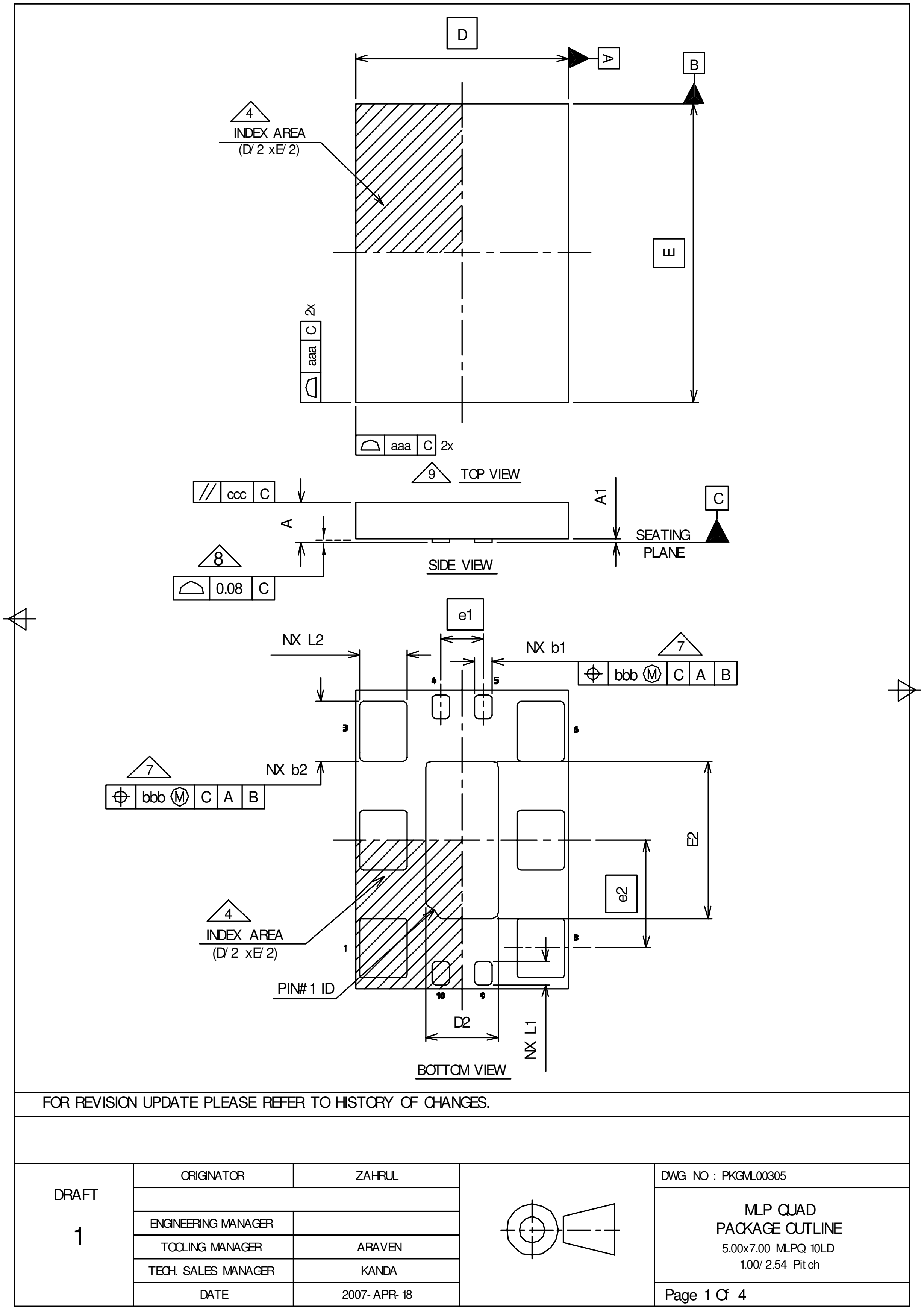
θ_{JA} vs. Air Flow	
Meters per Second	**0**
Multi-Layer PCB, JEDEC Standard Test Boards	39.2°C/W

Transistor Count

The transistor count for ICS83PN161I is: 42,520

Package Outline

Package Outline - K Suffix for 10-Lead VFQFN



Package Outline, continued

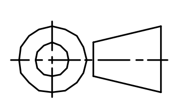
Package Outline - K Suffix for 10-Lead VFQFN

COMMON DIMENSION						
	TOLERANCE OF FORM AND POSITION					
aaa	0.15					
bbb	0.10					
ccc	0.10					

COMMON DIMENSION			
SYMBOL	V : Very thin		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
NOTES	1, 2	1, 2	1, 2

Summary Table				
Lead Pitch (e1 & e2)	Lead Count	Body Size	Very Very Thin Variation	Pin #1 ID
1.00/2.54	10	5.00X7.00	VNJR-1	R0.30

FOR REVISION UPDATE PLEASE REFER TO HISTORY OF CHANGES.

DRAFT 1	ORIGINATOR	ZAHRUL		DWG. NO : PKGML00305
				MLP QUAD PACKAGE OUTLINE 5.00x7.00 MLPQ 10LD 1.00/2.54 Pitch
	ENGINEERING MANAGER			
	TOOLING MANAGER	ARAVEN		
	TECH. SALES MANAGER	KANDA		
	DATE	2007-APR-18		PAGE: 2 of 4

Package Outline, continued

Package Outline - K Suffix for 10-Lead VFQFN

NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.

2. All dimensions are in millimeters, angles are in degrees(°).

3. N is the total number of terminals.

4. The location of the terminal #1 identifier and terminal numbering convention conforms to JEDEC publication 95 SPP-002.

5. ND and NE refer to the number of terminals on each D and E side respectively.

6. NJR refers to NON JEDEC REGISTERED

7. Dimension b applies to metallized terminal and is measured between 0.10mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.

8. Coplanarity applies to the terminals and all other bottom surface metallization.

9. Drawing shown are for illustration only.

FOR REVISION UPDATE PLEASE REFER TO HISTORY OF CHANGES.

DRAFT 1	ORIGINATOR	ZAHRUL	DWG. NO : PKGML00305
			MLP QUAD PACKAGE OUTLINE 5.00x7.00 MLPQ 10LD 1.00/2.54 Pitch
	ENGINEERING MANAGER		
	TOOLING MANAGER	ARAVEN	
	TECH. SALES MANAGER	KANDA	
	DATE	2007-APR-18	PAGE: 3 of 4

Package Outline, continued

Package Outline - K Suffix for 10-Lead VFQFN

Symbol \ Variation		VNJR-1	Note
D BSC		5.00	
E BSC		7.00	
b1	MIN	0.35	
	NOM	0.40	
	MAX	0.45	
b2	MIN	1.35	
	NOM	1.40	
	MAX	1.45	
D2	MIN	1.55	
	NOM	1.70	
	MAX	1.80	
E2	MIN	3.55	
	NOM	3.70	
	MAX	3.80	
L1	MIN	0.45	
	NOM	0.55	
	MAX	0.65	
L2	MIN	1.00	
	NOM	1.10	
	MAX	1.20	
N		10	
ND		2	
NE		3	
NOTES		-	
PAD DESIGN		-	

FOR REVISION UPDATE PLEASE REFER TO HISTORY OF CHANGES.

DRAFT 1	ORIGINATOR	ZAHRUL	DWG. NO : PKGML00305
	ENGINEERING MANAGER		MLP QUAD PACKAGE OUTLINE 5.00x7.00 MLPQ 10LD 1.00/2.54 Pitch
	TOOLING MANAGER	ARAVEN	
	TECH. SALES MANAGER	KANDA	
	DATE	2007-APR-18	PAGE: 4 of 4

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
83PN161AKILF	ICS3PN161AIL	"Lead-Free" 10 Lead VFQFN	Tray	-40°C to 85°C
83PN161AKILFT	ICS3PN161AIL	"Lead-Free" 10Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T4D	4 7 8 13	Differential DC Characteristics Table - changed V_{CMR} min. from V_{EE} + 0.5 to V_{EE}. Updated NOTES. Parameter Measurement Information section - updated *Differential Input Level* diagram. Updated *Wiring the Differential Inputs to Accept Single-ended Levels* section. Added Schematic Layout section.	3/15/10
C	 T3 T5A, T5B	1 2 5	Frequency Select Table - updated Output Frequency Column (extended decimal). Function Table - updated M Divider and Output Frequency Columns (extended decimal). AC Tables - updated Output Frequency rows (extended decimal).	5/17/10
C		3 16-19	Supply Voltage, $V_{CC.}$ Rating changed from 4.5V min. to 3.63V per Errata NEN-11-03. Updated 10-Lead VFQFN package information.	7/6/11

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