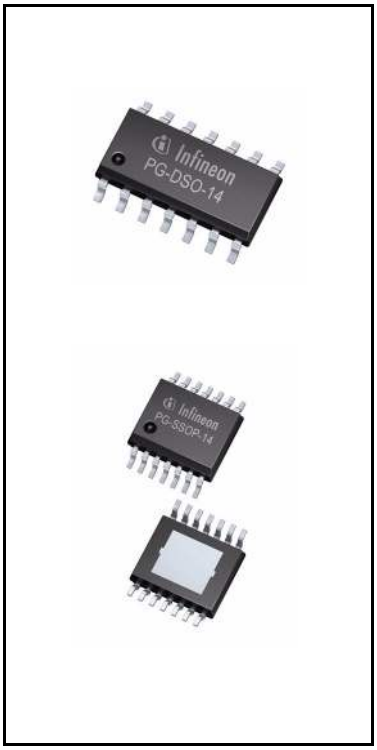
OPTIREG™ Linear TLE4678

Low drop out linear voltage regulator

AEC Qualified RoHS



Features

- Output voltage 5 V ±2%
- Current capability 200 mA
- Ultra low current consumption
- Very low dropout voltage
- Watchdog circuit for monitoring a microprocessor with programmable load-dependent activating threshold
- Reset circuit sensing the output voltage with programmable switching threshold and delay time
- Reset output active low down to V_Q = 1 V
- Separated reset and watchdog output
- Excellent line transient robustness
- Maximum input voltage V_I = -42 V to +45 V
- Reverse polarity protection
- Short circuit protected
- Overtemperature shutdown
- Automotive temperature range T_j = -40°C to +150°C
- Available in a small thermally enhanced PG-SSOP-14 package
- Green Product (RoHS Compliant)

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The OPTIREG™ Linear TLE4678 is a monolithic integrated low dropout fixed output voltage regulator for loads up to 200 mA. An input voltage of up to 45 V is regulated to an output voltage of 5 V. The integrated reset and watchdog function, as well as several protection circuits, combined with a wide operating temperature range offered by the TLE4678GM make it suitable for supplying microprocessor systems in automotive environments.

The watchdog circuitry will be disabled in case the output current drops below a programmable threshold, enabling a microcontroller to switch to stand-by mode. Modifying the reset threshold is possible by an optional resistor divider.

The TLE4678GM is available in a PG-DSO-14 package which makes it pin-compatible to the TLE4278, as well as in a small thermally enhanced PG-SSOP-14 exposed pad package.

Type	Package	Marking
TLE4678GM	PG-DSO-14	TLE4678GM
TLE4678EL	PG-SSOP-14	TLE4678

Table of contents

1 Block Diagram

For details on the circuit blocks see the respective section in this datasheet.

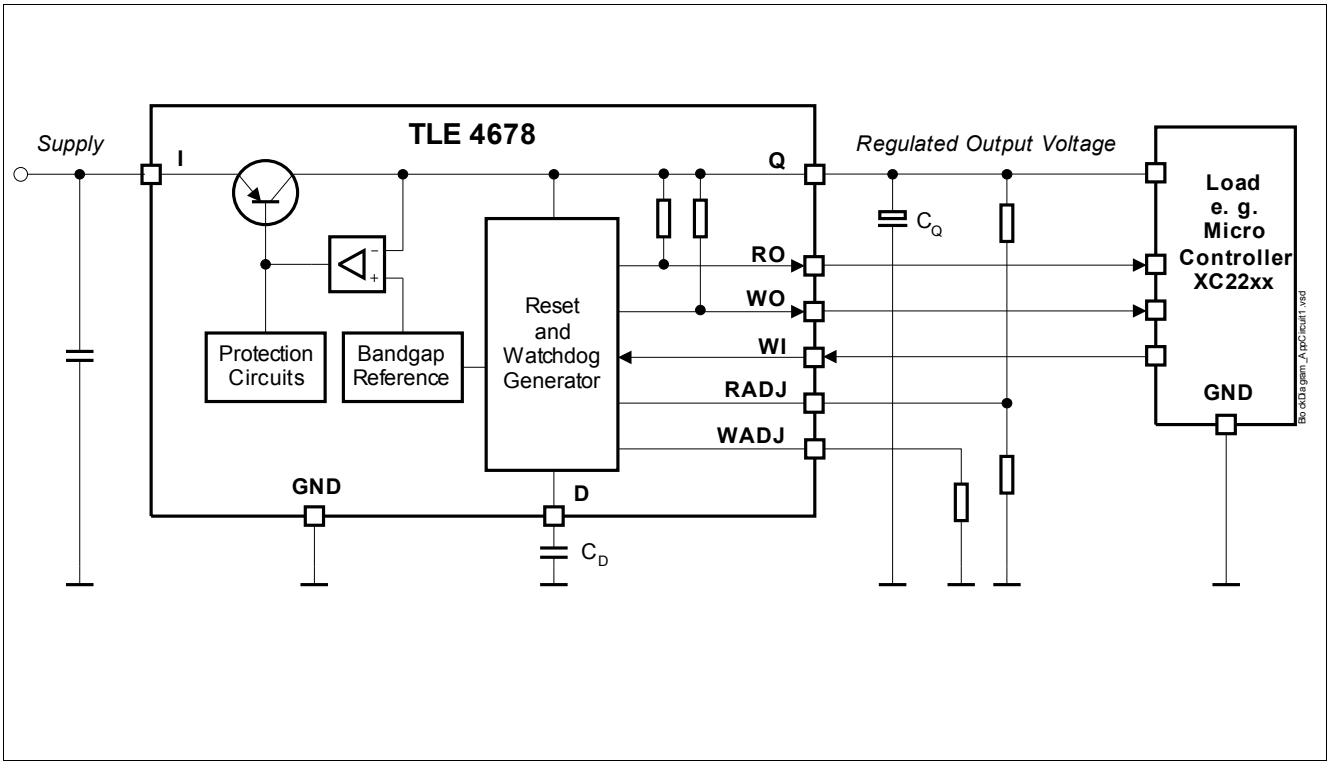


Figure 1 Block diagram and simplified application circuit

2 Pin configuration

2.1 Pin assignment PG-DSO-14

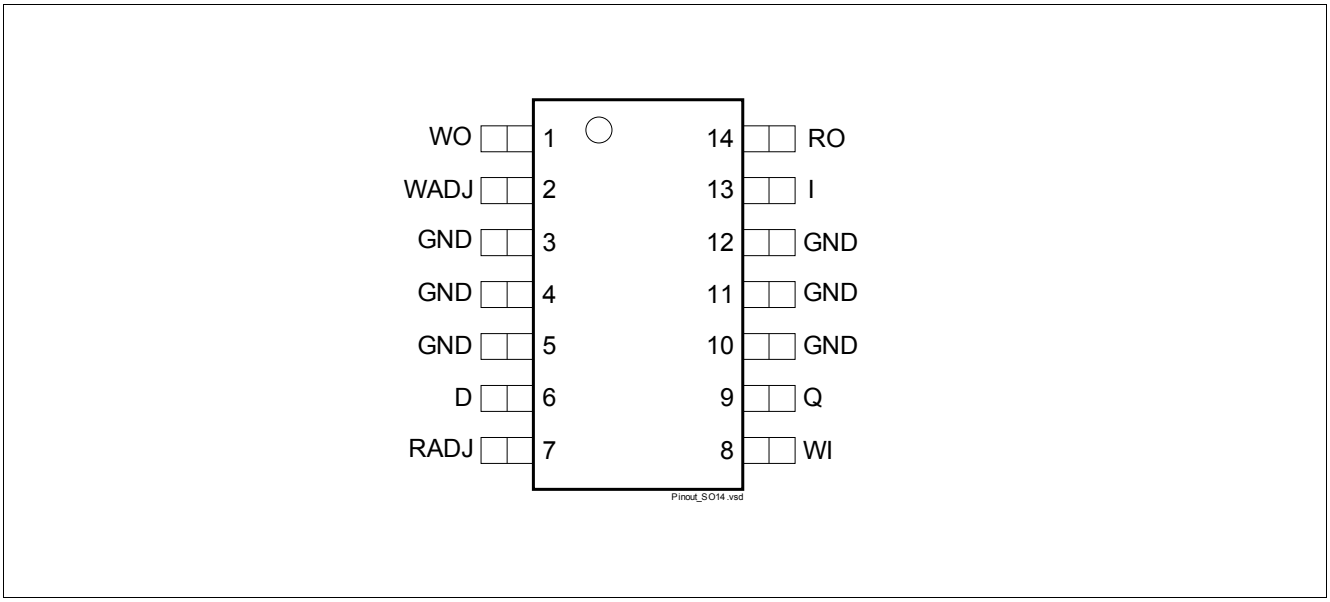


Figure 2 Pin assignment PG-DSO-14 package

2.2 Pin definitions and functions PG-DSO-14

Pin	Symbol	Function
1	WO	**Watchdog output** Open collector output with an internal pull-up resistor to the output Q. An additional external pull-up resistor to the output Q is optional. Leave open if the watchdog function is not needed.
2	WADJ	**Watchdog activating threshold adjust** An external resistor to GND determines the watchdog activating threshold. Connect directly to GND for disabling the watchdog. Connect directly to GND if the watchdog function is not needed. Connect to output Q via 270 kΩ resistor for permanently activating the watchdog.
3, 4, 5, 10, 11, 12	GND	**IC ground** Interconnect the GND pins on PCB. Connect to heat sink area.
6	D	**Reset delay and watchdog timing** Connect a ceramic capacitor D (pin 6) to GND for reset delay and watchdog timing adjustment. Leave only open if both the reset and the watchdog function are not needed.
7	RADJ	**Reset switching threshold adjust** For reset threshold adjustment connect to a voltage divider from output Q to GND. For triggering the reset at the internally determined threshold, connect this pin directly to GND. Connect directly to GND if the reset function is not needed.

Pin configuration

Pin	Symbol	Function
8	WI	**Watchdog input** Positive edge triggered input, usable for microcontroller monitoring. Connect to GND if the watchdog function is not needed.
9	Q	**5 V regulator output** Block to GND with a capacitor close to the IC pins, respecting capacitance and ESR requirements given in the **Chapter 3.2**.
13	I	**Regulator input and IC supply** For compensating line influences, a capacitor to GND close to the IC pins is recommended.
14	RO	**Reset output** Open collector output with an internal pull-up resistor to the output Q. An additional external pull-up resistor to the output Q is optional. Leave open if the reset function is not needed.

2.3 Pin assignment PG-SSOP-14

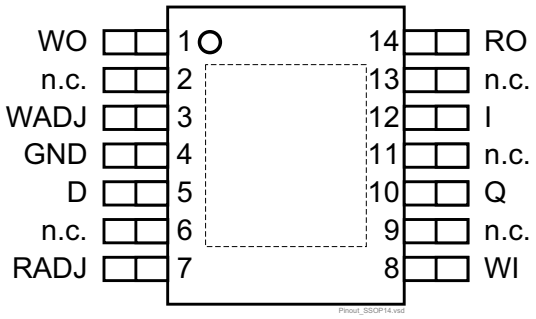


Figure 3 Pin assignment PG-SSOP-14 package

2.4 Pin definitions and functions PG-SSOP-14

Pin	Symbol	Function
1	WO	**Watchdog output** Open collector output with an internal pull-up resistor to the output Q. An additional external pull-up resistor to the output Q is optional. Leave open if the watchdog function is not needed.
3	WADJ	**Watchdog activating threshold adjust** An external resistor to GND determines the watchdog activating threshold. Connect directly to GND for disabling the watchdog. Connect directly to GND if the watchdog function is not needed. Connect to output Q via 270 kΩ resistor for permanently activating the watchdog.

Pin configuration

Pin	Symbol	Function
4	GND	**IC ground** Interconnect with the exposed pad and heatsink area on PCB.
5	D	**Reset delay and watchdog timing** Connect a ceramic capacitor D (pin 5) to GND for reset delay and watchdog timing adjustment. Leave only open if both, the reset and the watchdog function are not needed.
7	RADJ	**Reset switching threshold adjust** For reset threshold adjustment connect to a voltage divider from output Q to GND. For triggering the reset at the internally determined threshold, connect this pin directly to GND. Connect directly to GND if the reset function is not needed.
8	WI	**Watchdog input** Positive edge triggered input, usable for microcontroller monitoring. Connect to GND if the watchdog function is not needed.
10	Q	**5 V regulator output** Block to GND with a capacitor close to the IC pins, respecting capacitance and ESR requirements given in the **Chapter 3.2**.
12	I	**Regulator input and IC supply** For compensating line influences, a capacitor to GND close to the IC pins is recommended.
14	RO	**Reset output** Open collector output with an internal pull-up resistor to the output Q. An additional external pull-up resistor to the output Q is optional. Leave open if the reset function is not needed.
2, 6, 9, 11, 13	n. c.	**Internally not connected** Connection to GND on PCB recommended.
Exposed pad		Connect to heat sink area on PCB. Interconnect with GND.

3 General product characteristics

3.1 Absolute maximum ratings

Table 1 Absolute maximum ratings[1)]

T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage rating							
Regulator input and IC supply I	V_I	-42	–	45	V	–	P_4.1.1
Regulator output Q	V_Q	-1	–	7	V	–	P_4.1.2
Reset output RO	V_{RO}	-0.3	–	7	V	–	P_4.1.3
Reset delay and watchdog timing D	V_D	-0.3	–	7	V	–	P_4.1.4
Reset Switching threshold adjust RADJ	V_{RADJ}	-0.3	–	7	V	–	P_4.1.5
Watchdog input WI	V_{WI}	-0.3	–	7	V	–	P_4.1.6
Watchdog output WO	V_{WO}	-0.3	–	7	V	–	P_4.1.7
Watchdog activating threshold adjust WADJ	V_{WADJ}	-0.3	–	7	V	–	P_4.1.8
Temperature							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.9
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.10
ESD susceptibility							
ESD resistivity	$V_{ESD,HBM}$	-3	–	3	kV	Human Body Model [2)] Pin 13 (Input) only.	P_4.1.11
		-2	–	2	kV	Human Body Model [2)] All pins except pin 13 (Input)	P_4.1.12
	$V_{ESD,CDM}$	-1	–	1	kV	Charged Device Model [3)]	P_4.1.13

1) Not subject to production test, specified by design.

2) ESD susceptibility, Human Body Model “HBM” according to EIA/JESD 22-A114B.

3) ESD susceptibility, Charged Device Model “CDM” according to EIA/JESD22-C101 or ESDA STM5.3.1.

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

3.2 Functional range

Table 2 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range for normal operation	$V_{I(nor)}$	$V_Q + V_{dr}$	–	45	V	1)	P_4.2.1
Extended input voltage range	$V_{I(ext)}$	3.3	–	45	V	2)	P_4.2.2
Input voltage transient immunity	$\Delta V_I/\Delta t$	-10	–	20	V/µs	$\Delta V_I \leq 10$ V; $V_I > 9$ V; No trigger of WO, RO. 3)	P_4.2.3
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.4
Output capacitor requirements	C_Q	10	–	–	µF	4)	P_4.2.5
	ESR_{CQ}	–	–	3	Ω	5)	P_4.2.6

1) For specification of the output voltage V_Q and the dropout voltage V_{dr}, see **Chapter 4**.
2) The output voltage V_Q will follow the input voltage, but is outside the specified range. For details see **Chapter 4**.
3) Transient measured directly at the input pin. Not subject to production test, specified by design.
4) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.
5) Relevant ESR value at f = 10 kHz.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

3.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
TLE4678GM (PG-DSO-14)							
Junction – Soldering point	R_{thJSP}	–	27	–	K/W	Pins 3 - 5 and 10 - 12 fixed to T_A [1]	P_4.3.1
Junction – Ambient	R_{thJA}	–	104	–	K/W	Footprint only [1] [2]	P_4.3.2
		–	73	–	K/W	300 mm² PCB heatsink area [1] [2]	P_4.3.3
		–	65	–	K/W	600 mm² PCB heatsink area [1] [2]	P_4.3.4
		–	63	–	K/W	2s2p PCB [1] [3]	P_4.3.5
TLE4678EL (PG-SSOP-14)							
Junction to case	R_{thJC}	–	10	–	K/W	[1]	P_4.3.6
Junction to ambient	R_{thJA}	–	140	–	K/W	Footprint only [1] [2]	P_4.3.7
		–	63	–	K/W	300 mm² PCB heatsink area [1] [2]	P_4.3.8
		–	53	–	K/W	600 mm² PCB heatsink area [1] [2]	P_4.3.9
		–	47	–	K/W	2s2p PCB [1] [3]	P_4.3.10

1) Not subject to production test; specified by design.

2) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The product (chip+package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 × 70 µm Cu).

3) Specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip+package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

4 Voltage regulator

4.1 Description voltage regulator

The output voltage V_Q is controlled by comparing a portion of it to an internal reference and driving a PNP pass transistor accordingly. Saturation control as a function of the load current prevents any oversaturation of the pass element. The control loop stability depends on the output capacitor C_Q, the load current, the chip temperature and the poles/zeros introduced by the integrated circuit. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the table **Table 3.2** have to be maintained. For details see also the typical performance graph "Output Capacitor Series Resistor ESR_{CQ} vs. Output Current I_Q". Also, the output capacitor shall be sized to buffer load transients.

An input capacitor C_I is not needed for the control loop stability, but recommended to buffer line influences. Connect the capacitors close to the IC terminals.

Protection circuitry prevents the IC as well as the application from destruction in case of catastrophic events. These safeguards contain output current limitation, reverse polarity protection as well as thermal shutdown in case of overtemperature.
In order to avoid excessive power dissipation that could never be handled by the pass element and the package, the maximum output current is decreased at input voltages above V_I = 22 V.
The thermal shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, a junction temperature above 150°C is outside the maximum rating and therefore reduces the IC lifetime.
The TLE4678GM allows a negative supply voltage. However, several small currents are flowing into the IC increasing its junction temperature. This has to be considered for the thermal design, respecting that the thermal protection circuit is not operating during reverse polarity condition.

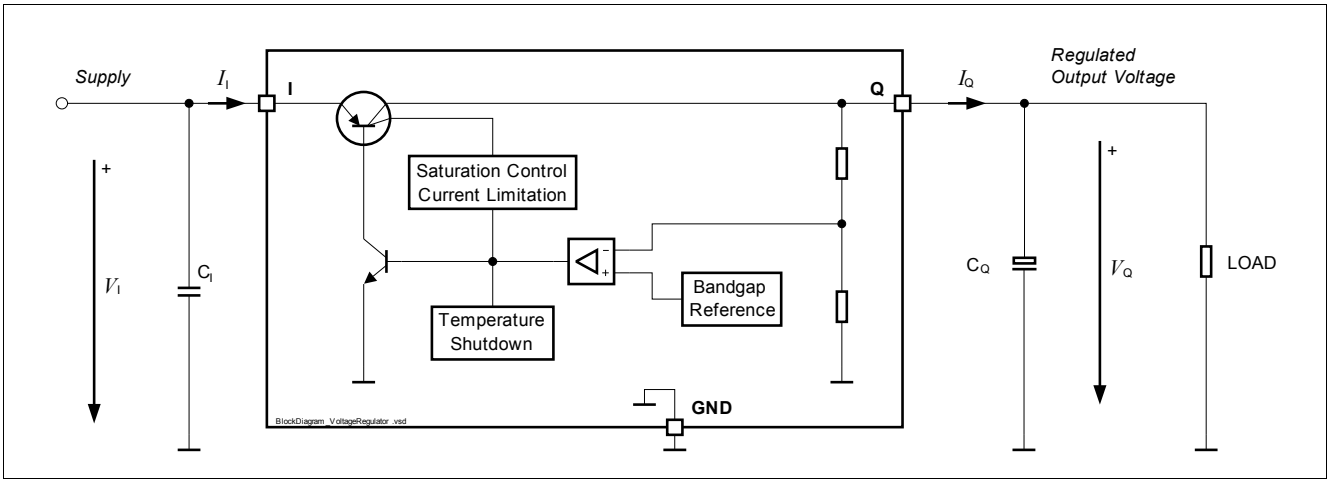


Figure 4 Block diagram voltage regulator circuit

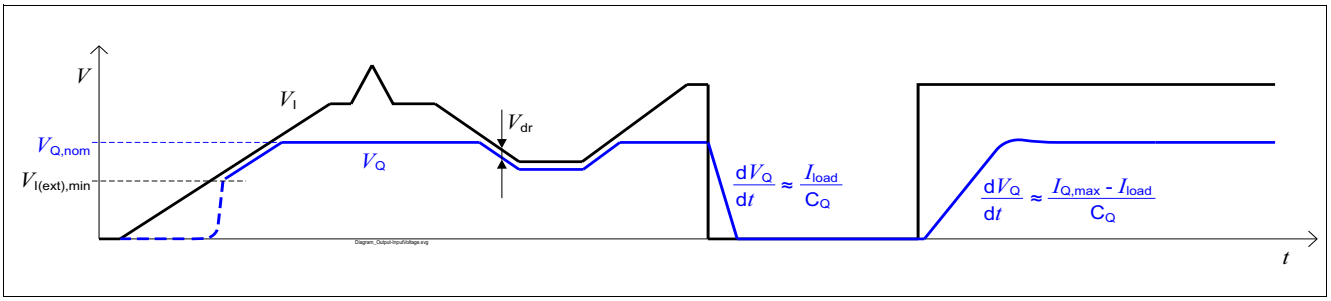


Figure 5 Output voltage vs. input voltage

4.2 Electrical characteristics voltage regulator

Table 4 Electrical characteristics voltage regulator

V_I = 13.5 V, T_j = -40°C to +150°C, all voltages with respect to ground, direction of currents as shown in **Figure 4** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage	V_Q	4.9	5.0	5.1	V	0 mA ≤ I_Q ≤ 200 mA; 8 V ≤ V_I ≤ 18 V	P_5.2.1
						0 mA ≤ I_Q ≤ 150 mA; 6 V ≤ V_I ≤ 18 V	P_5.2.2
						0 mA ≤ I_Q ≤ 100 mA; 18 V ≤ V_I ≤ 32 V T_j ≤ 105°C 1) 2)	P_5.2.3
						0 mA ≤ I_Q ≤ 10 mA; 32 V ≤ V_I ≤ 45 V T_j ≤ 105°C 1) 2)	P_5.2.4
						0.3 mA ≤ I_Q ≤ 100 mA; 18 V ≤ V_I ≤ 32 V 1)	P_5.2.5
						0.3 mA ≤ I_Q ≤ 10 mA; 32 V ≤ V_I ≤ 45 V 1)	P_5.2.6
Load regulation steady-state	$\lvert\Delta V_{Q,load}\rvert$	–	5	30	mV	I_Q = 1 mA to 150 mA; V_I = 6 V	P_5.2.7
Line regulation steady-state	$\lvert\Delta V_{Q,line}\rvert$	–	5	20	mV	V_I = 6 V to 32 V; I_Q = 5 mA	P_5.2.8
Power supply ripple rejection	*PSRR*	60	65	–	dB	f_{ripple} = 100 Hz; V_{ripple} = 1 Vpp 2)	P_5.2.9
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	90	200	mV	I_Q = 50 mA 3)	P_5.2.10
		–	165	350	mV	I_Q = 150 mA 3)	P_5.2.11
Output current limitation	$I_{Q,max}$	201	350	500	mA	0 V ≤ V_Q ≤ 4.8 V	P_5.2.12
Reverse current	I_Q	-1.5	-0.7	–	mA	V_I = 0 V; V_Q = 5 V	P_5.2.13

Table 4 Electrical characteristics voltage regulator (cont'd)

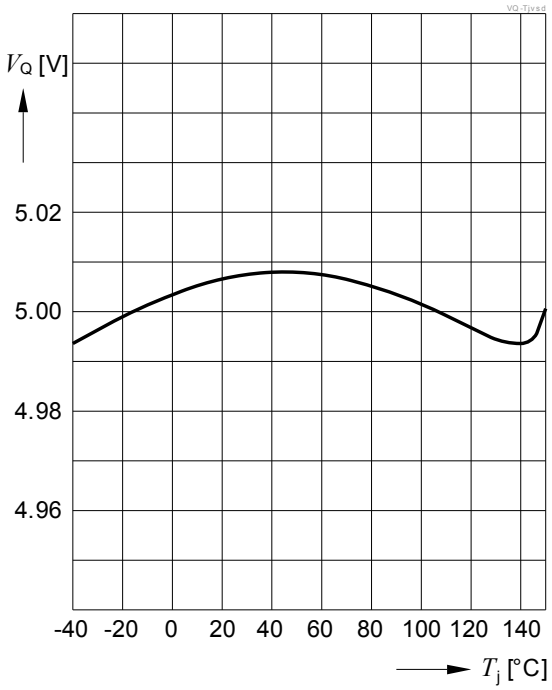
V_I = 13.5 V, T_j = -40°C to +150°C, all voltages with respect to ground, direction of currents as shown in **Figure 4** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reverse current at negative input voltage	I_I	-2	-1	–	mA	V_I = -16 V; V_Q = 0 V	P_5.2.14
		-5	-3	–	mA	V_I = -42 V; V_Q = 0 V	P_5.2.15
Overtemperature shutdown threshold	$T_{j,sd}$	151	–	200	°C	T_j increasing 2)	P_5.2.16
Overtemperature shutdown threshold hysteresis	$T_{j,hy}$	–	20	–	K	T_j decreasing 2)	P_5.2.17

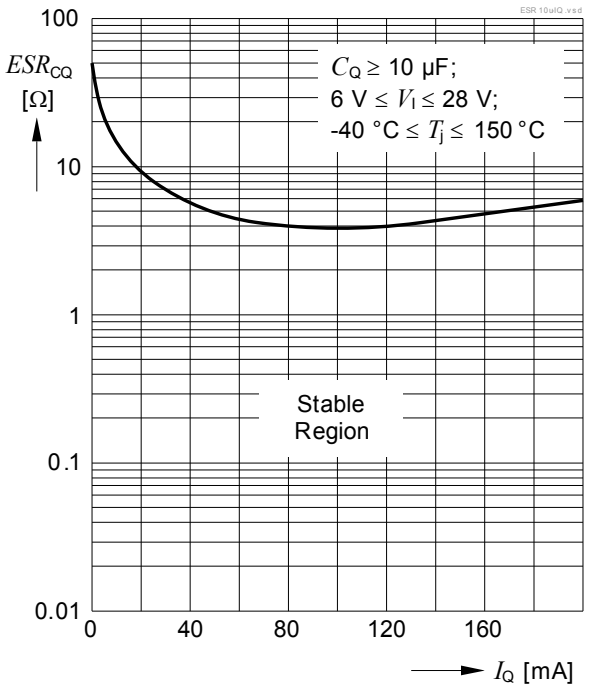
1) See typical performance graph for details.
2) Parameter not subject to production test; specified by design.
3) Measured when the output voltage V_Q has dropped 100 mV from its nominal value.

4.3 Typical performance characteristics voltage regulator

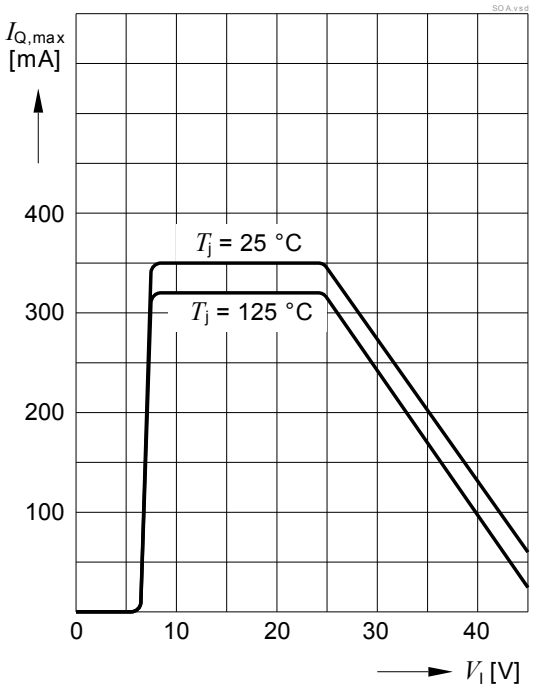
Output voltage V_Q vs. junction temperature T_j



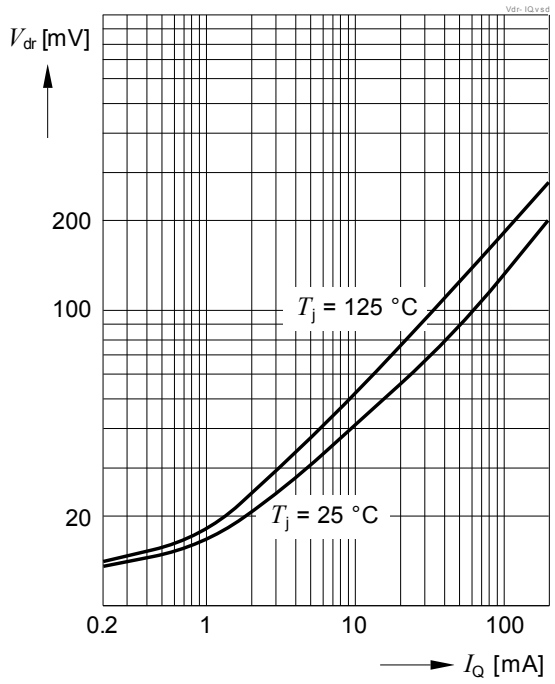
Output capacitor series resistor ESR_{CQ} vs. output current I_Q



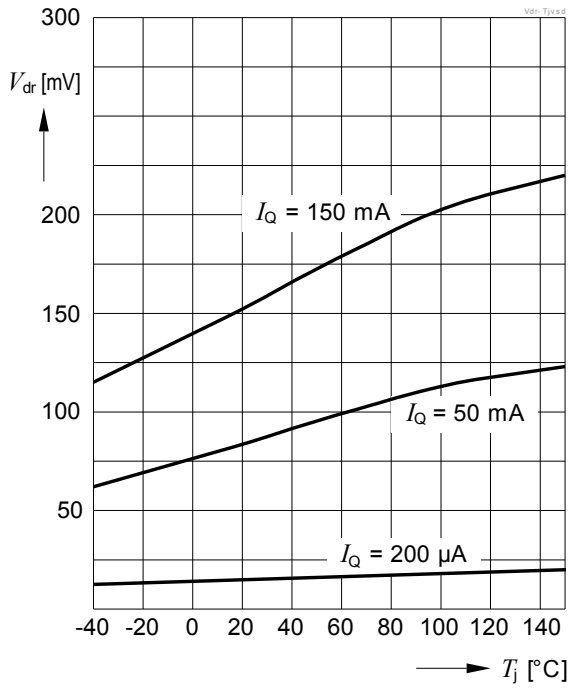
Output current limitation $I_{Q,max}$ vs. input voltage V_I



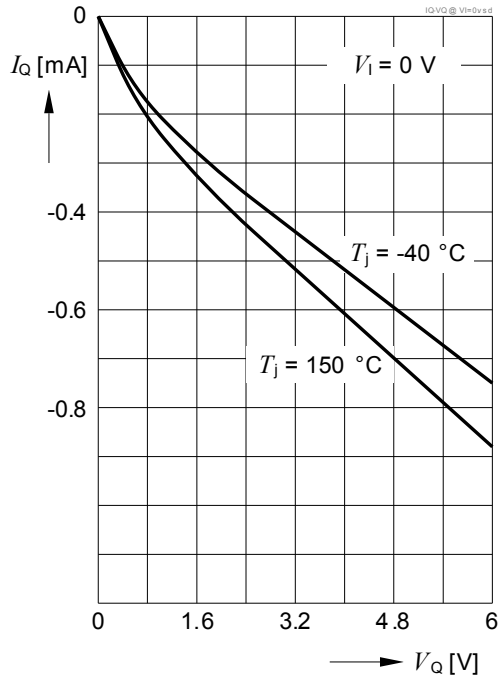
Dropout voltage V_{dr} vs. output current I_Q



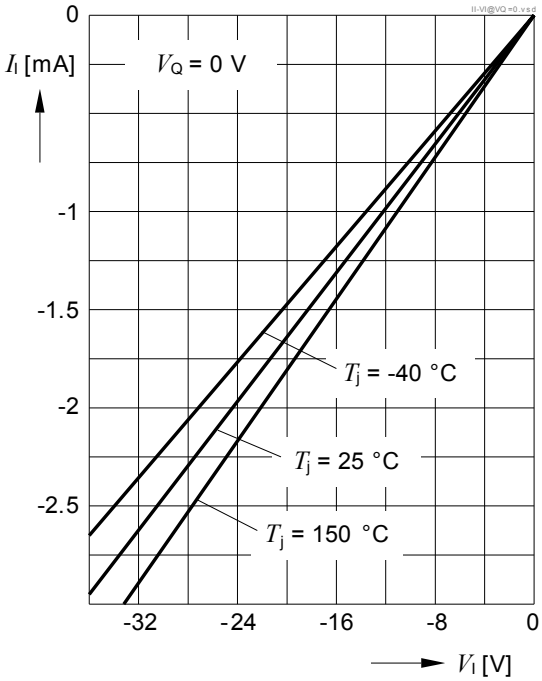
Dropout voltage V_{dr} vs. junction temperature T_j



Reverse output current I_Q vs. output voltage V_Q



Reverse current I_I vs. input voltage V_I



5 Current consumption

5.1 Electrical characteristics current consumption

Table 5 Electrical characteristics current consumption

V_I = 13.5 V, T_j = -40°C to +150°C, all voltages with respect to ground, direction of currents as shown in **Figure 6** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption watchdog deactivated $I_q = I_I - I_Q$	I_{q1}	–	70	80	µA	$I_Q \le 200$ µA; $T_j \le 25$°C Watchdog deactivated	P_6.1.1
		–	77	85	µA	$I_Q \le 200$ µA; $T_j \le 85$°C Watchdog deactivated	P_6.1.2
Current consumption $I_q = I_I - I_Q$	I_{q2}	–	117	130	µA	$I_Q \le 2$ mA; $T_j \le 25$°C Watchdog activated	P_6.1.3
		–	127	135	µA	$I_Q \le 2$ mA; $T_j \le 85$°C Watchdog activated	P_6.1.4
		–	1	2	mA	I_Q = 50 mA	P_6.1.5
		–	5.5	8	mA	I_Q = 150 mA	P_6.1.6

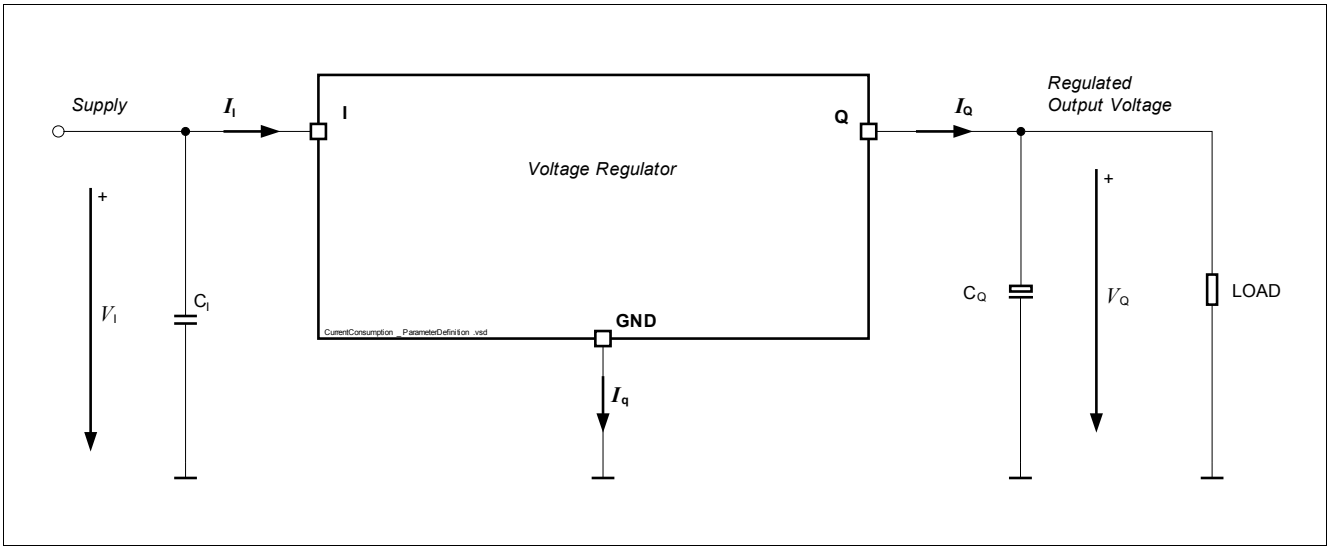
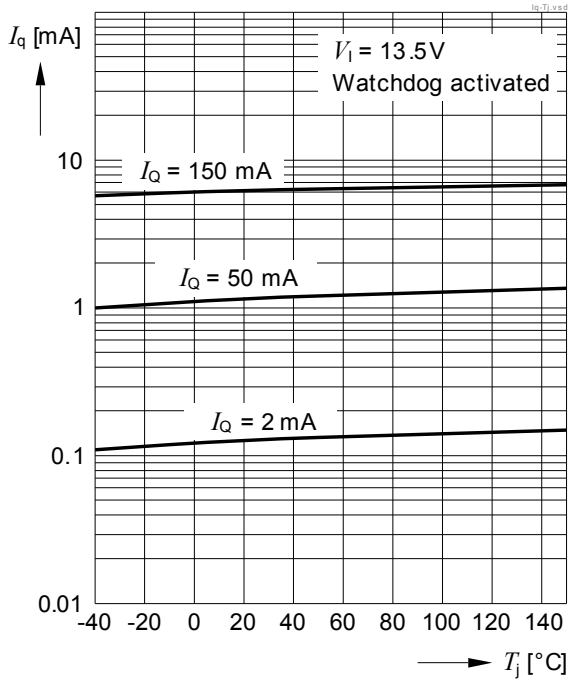


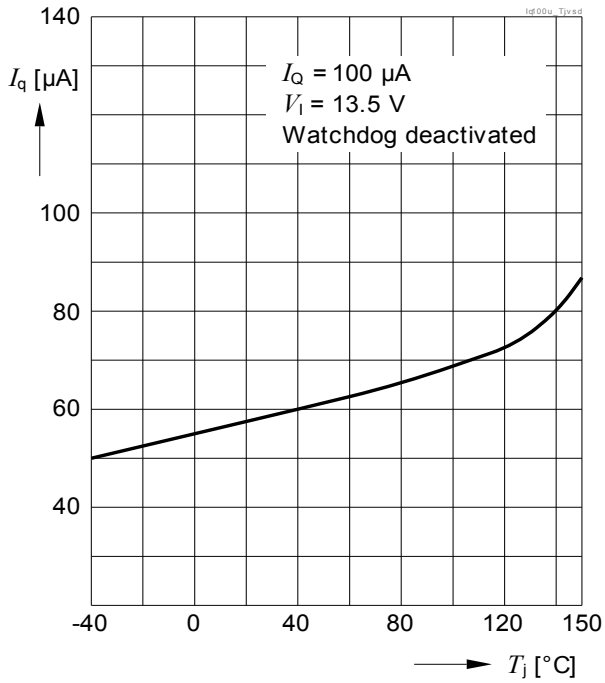
Figure 6 Parameter definition

5.2 Typical performance characteristics current consumption

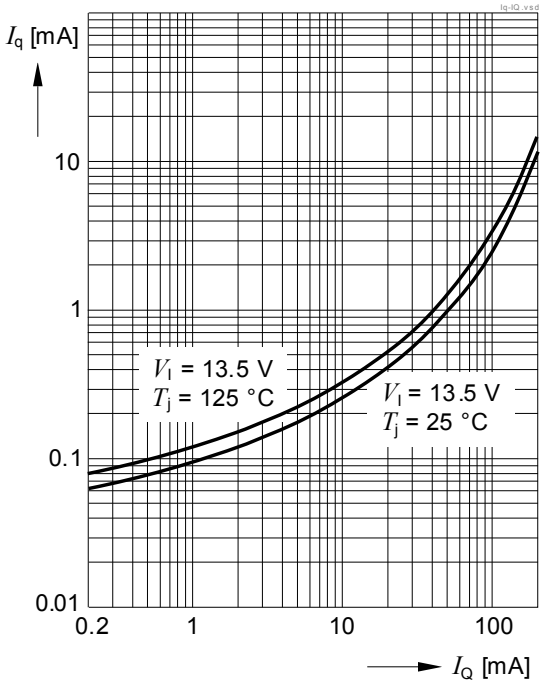
Current consumption I_q vs. junction temperature T_j



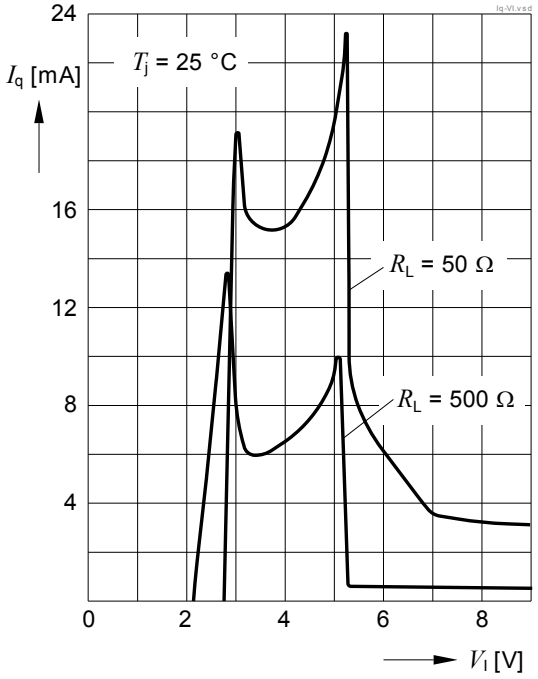
Current consumption I_q vs. junction temperature T_j



Current consumption I_q vs. output current I_Q



Current consumption I_q vs. input voltage V_I



6 Reset function

6.1 Description reset function

The reset function provides several features:

Output undervoltage reset

An output undervoltage condition is indicated by setting the reset output “RO” to “low”. This signal might be used to reset a microcontroller during low supply voltage.

Power-on reset delay time

The power-on reset delay time $t_{d,PWR-ON}$ allows a microcontroller and oscillator to start up. This delay time is the time period from exceeding the upper reset switching threshold $V_{RT,hi}$ until the reset is released by switching the reset output “RO” from “low” to “high”. The power-on reset delay time $t_{d,PWR-ON}$ is defined by an external delay capacitor C_D connected to pin “D” which is charged up by the delay capacitor charge current $I_{D,ch}$ starting from V_D = 0 V.

In case a power-on reset delay time $t_{d,PWR-ON}$ different from the value for C_D = 100 nF is required, the delay capacitor’s value can be derived from the specified value given in P_7.2.15:

$$C_D = 100\ nF \times t_{d,PWR-ON} / t_{d,PWR-ON,100nF} \quad (6.1)$$

with

- $t_{d,PWR-ON}$: Desired power-on reset delay time.
- $t_{d,PWR-ON,100nF}$: Power-on reset delay time specified in P_7.2.15.
- C_D: Delay capacitor required.

The formula is valid for $C_D \geq 10$ nF. For precise timing calculations consider also the delay capacitor’s tolerance.

Undervoltage reset delay time

Unlike the power-on reset delay time, the undervoltage reset delay time t_d considers a short output undervoltage event where the delay capacitor C_D is assumed to be discharged to $V_D = V_{DST,lo}$ only before the charging sequence starts. Therefore, the undervoltage reset delay time t_d is defined by the delay capacitor charge current $I_{D,ch}$ starting from $V_D = V_{DST,lo}$ and the external delay capacitor C_D.

A delay capacitor C_D for a different undervoltage reset delay time as specified in P_7.2.14 can be calculated similar as above:

$$C_D = 100\ nF \times t_d / t_{d,100nF} \quad (6.2)$$

with

- t_d: Desired undervoltage reset delay time.
- $t_{d,100nF}$: Power-on reset delay time specified in P_7.2.14.
- C_D: Delay capacitor required

The formula is valid for $C_D \geq 10$ nF. For precise timing calculations consider also the delay capacitor’s tolerance.

Reset function

Reset reaction time

In case the output voltage of the regulator drops below the output undervoltage lower reset threshold $V_{RT,lo}$, the delay capacitor C_D is discharged rapidly. Once the delay capacitor's voltage has reached the lower delay switching threshold $V_{DST,lo}$, the reset output "RO" will be set to "low".

Additionally to the delay capacitor discharge time $t_{rr,d}$, an internal reaction time $t_{rr,int}$ applies. Hence, the total reset reaction rime $t_{rr,total}$ becomes:

$$t_{rr,total} = t_{rr,int} + t_{rr,d} \quad (6.3)$$

with

- $t_{rr,total}$: Total reset reaction time.
- $t_{rr,int}$: Internal reset reaction time; see P_7.2.16.
- $t_{rr,d}$: Delay capacitor discharge time. For a capacitor C_D different from the value specified in P_7.2.17, see typical performance graphs.

Reset output "RO"

The reset output "RO" is an open collector output with an integrated pull-up resistor. In case a lower-ohmic "RO" signal is desired, an external pull-up resistor to the output "Q" can be connected. Since the maximum "RO" sink current is limited, the optional external resistor $R_{RO,ext}$ must not be lower than specified in P_7.2.8.

Reset output "RO" Low for $V_Q \geq 1$ V

In case of an undervoltage reset condition reset output "RO" is held "low" for $V_Q \geq 1$ V, even if the input voltage V_I is 0 V. This is achieved by supplying the reset circuit from the output capacitor.

Reset adjust function

The undervoltage reset switching threshold can be adjusted according to the application's needs by connecting an external voltage divider (R_{ADJ1}, R_{ADJ2}) at pin "RADJ". For selecting the default threshold connect pin "RADJ" to GND. The reset adjustment range is given in P_7.2.6.

When dimensioning the voltage divider, take into consideration that there will be an additional current constantly flowing through the resistors.

With a voltage divider connected, the reset switching threshold $V_{RT,adj}$ is calculated as follows:

$$V_{RT,adj} = V_{RADJ,th} \times (R_{ADJ,1} + R_{ADJ,2}) / R_{ADJ,2} \quad (6.4)$$

with

- $V_{RT,adj}$: Desired reset switching threshold.
- $R_{ADJ,1}$, $R_{ADJ,2}$: Resistors of the external voltage divider, see **Figure 7**.
- $V_{RADJ,th}$: Reset adjust switching threshold given in P_7.2.5.

Reset function

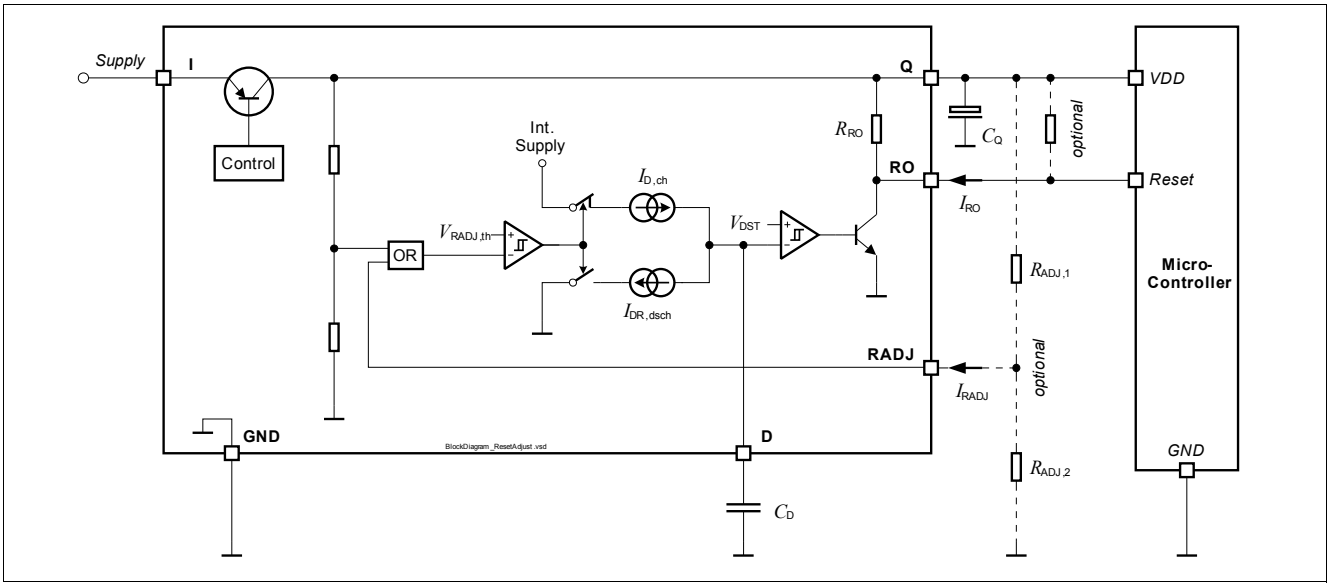


Figure 7 Block diagram reset circuit

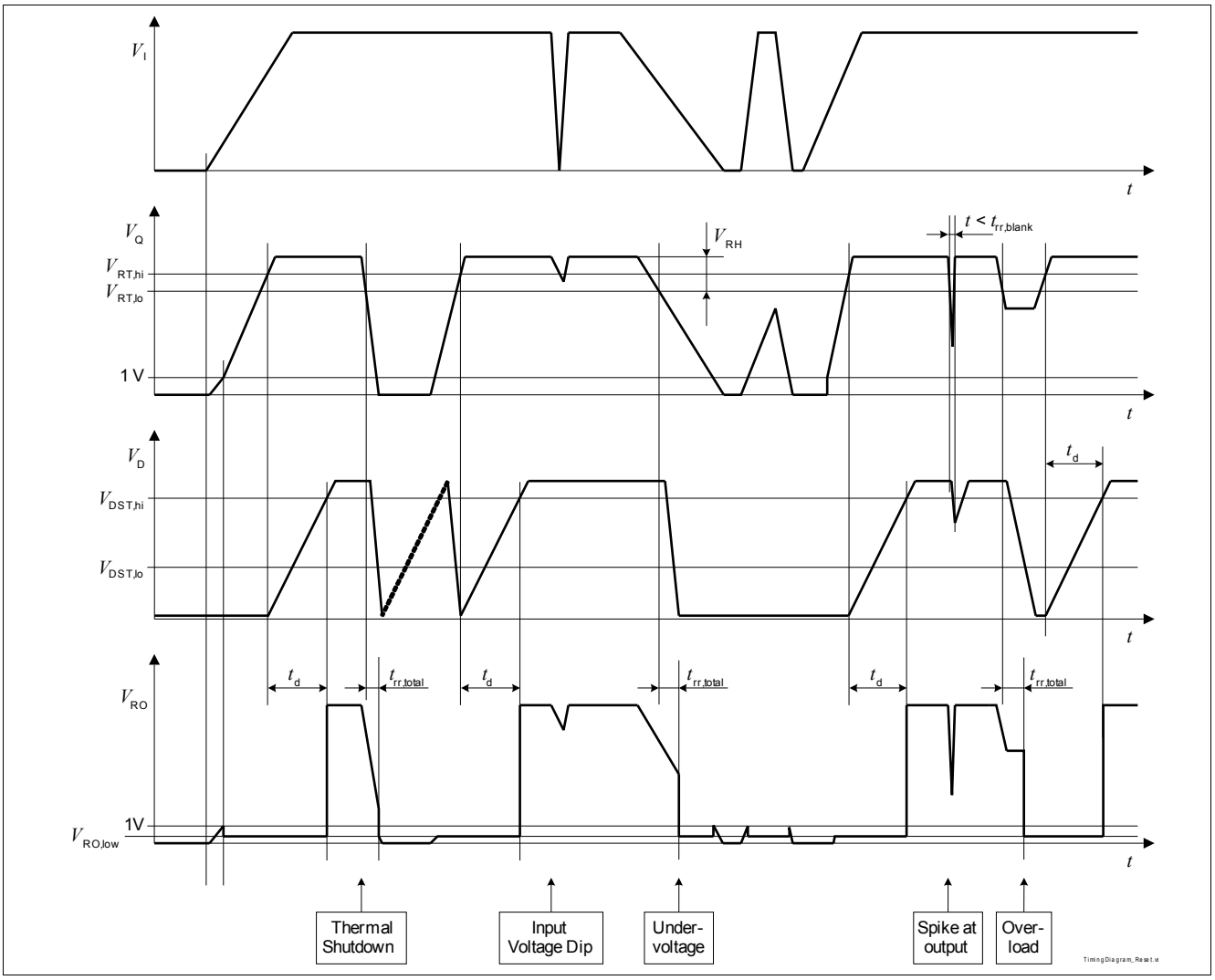


Figure 8 Timing diagram reset

6.2 Electrical characteristics reset function

Table 6 Electrical characteristics reset function

V_I = 13.5 V, T_j = -40°C to +150°C, all voltages with respect to ground, direction of currents as shown in **Figure 7** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output undervoltage reset comparator default values (pin RADJ = GND)							
Output undervoltage reset lower switching threshold	$V_{RT,lo}$	4.6	4.7	4.8	V	V_I = 0 V V_Q decreasing RADJ = GND	P_7.2.1
Output undervoltage reset upper switching threshold	$V_{RT,hi}$	4.7	4.8	4.9	V	V_I within operating range V_Q increasing RADJ = GND	P_7.2.2
Output undervoltage reset switching hysteresis	$V_{RT,hy}$	60	120	–	mV	V_I within operating range RADJ = GND.	P_7.2.3
Output undervoltage reset headroom	V_{RH}	250	300	–	mV	Calculated Value: V_Q - $V_{RT,lo}$ V_I within operating range I_Q = 50 mA RADJ = GND	P_7.2.4
Reset threshold adjustment							
Reset adjust lower switching threshold	$V_{RADJ,th}$	1.176	1.20	1.224	V	V_I = 0 V 3.2 V ≤ V_Q < 5 V	P_7.2.5
Lower reset threshold adjustment range [1)]	$V_{RT,adj}$	3.20	–	$V_{RT,lo}$	V	–	P_7.2.6
Reset output RO							
Reset output low voltage	$V_{RO,low}$	–	0.2	0.4	V	V_I = 0 V; $R_{RO,ext}$ = 3.3 kΩ; 1 V ≤ V_Q ≤ $V_{RT,low}$	P_7.2.7
Reset output external pull-up resistor to Q	$R_{RO,ext}$	3	–	–	kΩ	V_I = 0 V; V_{RO} = 0.4 V 1 V ≤ V_Q ≤ $V_{RT,low}$	P_7.2.8
Reset output internal pull-up resistor	R_{RO}	20	30	40	kΩ	Internally connected to Q	P_7.2.9
Reset delay timing							
Upper delay switching threshold	$V_{DST,hi}$	–	1.21	–	V	–	P_7.2.10
Lower delay switching threshold	$V_{DST,lo}$	–	0.30	–	V	–	P_7.2.11
Delay capacitor charge current	$I_{D,ch}$	–	2.8	–	µA	V_D = 1 V	P_7.2.12

Table 6 Electrical characteristics reset function (cont'd)

V_I = 13.5 V, T_j = -40°C to +150°C, all voltages with respect to ground, direction of currents as shown in **Figure 7** (unless otherwise specified)

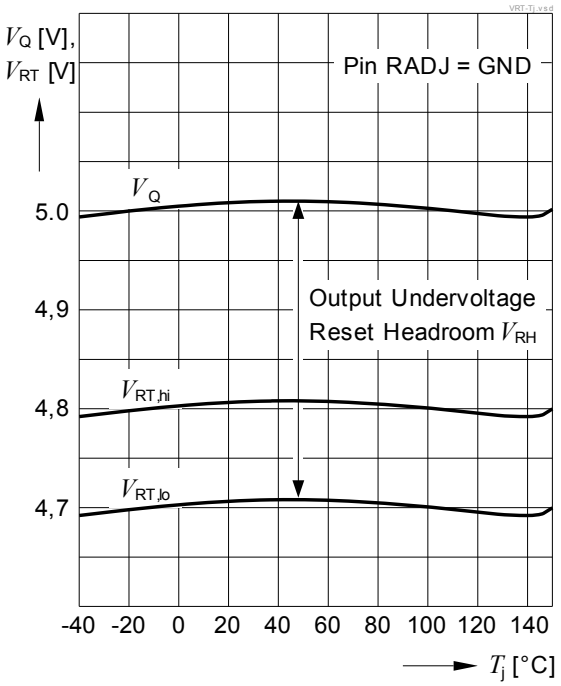
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Delay capacitor reset discharge current	$I_{DR,dsch}$	–	80	–	mA	V_D = 1 V	P_7.2.13
Undervoltage reset delay time	$t_{d,100nF}$	23	31	41	ms	Calculated value; C_D = 100 nF 2); C_D discharged to $V_{DST,lo}$	P_7.2.14
Power-on reset delay time	$t_{d,PWR-ON,100nF}$	30	43	56	ms	Calculated value; C_D = 100 nF 2); C_D discharged to 0 V;	P_7.2.15
Internal reset reaction time	$t_{rr,int}$	–	9	15	µs	C_D = 0 nF	P_7.2.16
Delay capacitor discharge time	$t_{rr,d,100nF}$	–	1.5	3	µs	C_D = 100 nF 2)	P_7.2.17
Total reset reaction time	$t_{rr,total,100nF}$	–	10.5	18	µs	Calculated Value: $t_{rr,d,100nF} + t_{rr,int}$; C_D = 100 nF 2)	P_7.2.18

1) Related parameters ($V_{RT,hi}$, $V_{RT,hy}$) are scaled linear when the reset switching threshold is modified.

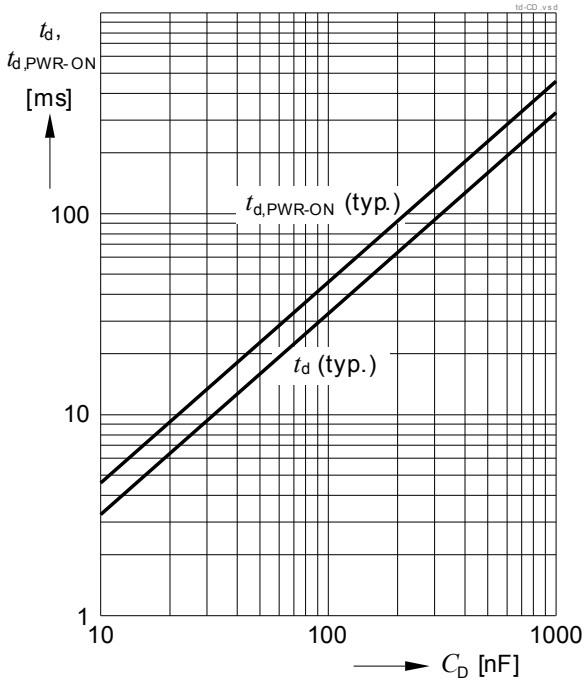
2) For programming a different delay and reset reaction time, see **Chapter 6.1**.

6.3 Typical performance characteristics reset function

Undervoltage reset switching thresholds $V_{RT,lo}$, $V_{RT,hi}$ vs. junction temperature T_j



Reset delay time t_d, $t_{d,PWR-ON}$ vs. delay capacitor C_D



7 Watchdog function

7.1 Description

The TLE4678 features a load dependent watchdog function with a programmable activating threshold as well as programmable watchdog timing.

The watchdog function monitors a microcontroller, including time base failures. In case of a missing rising edge within a certain pulse repetition time, the watchdog output is set to 'low'. The programming of the expected watchdog pulse repetition time can be easily done by an external reset delay capacitor.

The watchdog output "WO" is separated from the reset output "RO". Hence, the watchdog output might be used as an interrupt signal for the microcontroller independent from the reset signal. It is possible to interconnect pin "WO" and pin "RO" in order to establish a wire-or function with a dominant low signal.

Programmable watchdog activation threshold and hysteresis

In case a microcontroller is set to sleep mode or to low power mode, its current consumption is very low and the controller might not be able to send any watchdog pulses to the regulators watchdog input "WI". In order to avoid unwanted wake-up signals due to missing edges at pin "WI", the TLE4678 watchdog function can be activated dependent on the regulator's output current. The TLE4678 comprises a default watchdog activating threshold $I_{Q,WDact,th}$ with a small hysteresis $I_{Q,WDact,hy}$. The thresholds can be increased by connecting an external resistor $R_{WADJ,ext}$ to pin "WADJ". For using the default watchdog activating threshold, leave pin "WADJ" open.

The following equation calculates the external resistor $R_{WADJ,ext}$ that is needed at pin "WADJ" for activating the watchdog at a desired output current $I_{Q,WDact,th}$:

(7.1)

$$R_{WADJ,ext} = \frac{F_{WDact,th} \times R_{WADJ,int}}{(R_{WADJ,int} \times I_{Q,WDact,th}) - F_{WDact,th}}$$

for $I_{Q,WDact,th}$ larger than the default value given in P_8.2.1.

At decreasing output current, the deactivation threshold then would be:

(7.2)

$$I_{Q,WDdeact,th} = F_{WDdeact,th} \times \frac{R_{WADJ,int} + R_{WADJ,ext}}{R_{WADJ,int} \times R_{WADJ,ext}}$$

The watchdog activating threshold hysteresis $I_{Q,WDact,hy}$ calculates:

(7.3)

$$I_{Q,WDact,hy} = F_{WDact,hy} \times \frac{R_{WADJ,int} + R_{WADJ,ext}}{R_{WADJ,int} \times R_{WADJ,ext}}$$

with:

- $I_{Q,WDact,th}$: Desired "watchdog activating threshold".
- $R_{WADJ,int}$: Internal watchdog adjust resistor.

Watchdog function

- $R_{WADJ,ext}$: External watchdog adjust resistor.
- $F_{WDact,th}$: Activating threshold factor.
- $F_{WDdeact,th}$: Deactivating threshold factor.
- $F_{WDact,hy}$: Activating threshold factor hysteresis.

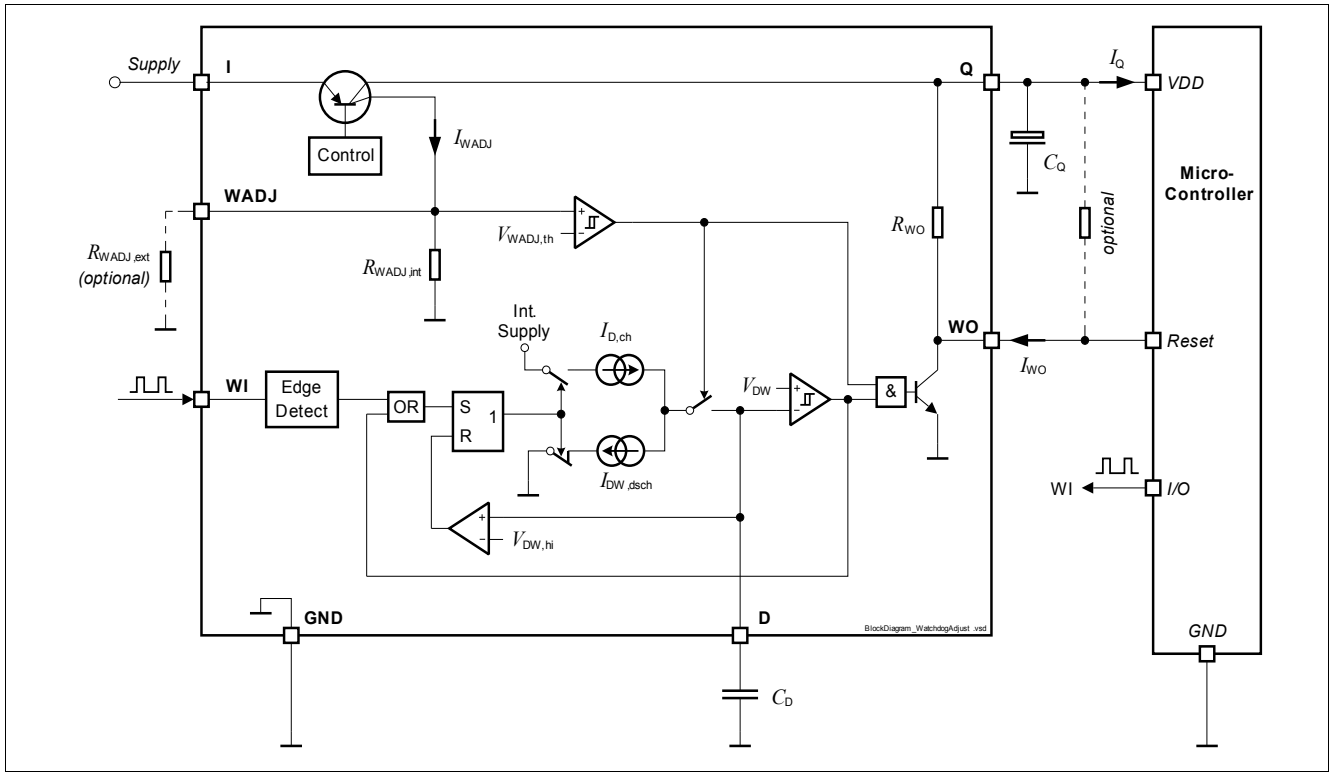


Figure 9 Block diagram watchdog circuit

Watchdog output “WO”

The watchdog output “WO” is an open collector output with an integrated pull-up resistor. In case a lower-ohmic “WO” signal is desired, an external pull-up resistor to the output “Q” can be connected. Since the maximum “WO” sink current is limited, the optional external resistor $R_{WO,ext}$ needs to be sized to comply with the watchdog output sink current (see P_8.2.15 and P_8.2.16).

Watchdog input “WI”

The watchdog is triggered by a positive edge at the watchdog input “WI”. The signal is filtered by a band-pass filter and therefore its amplitude and slope have to comply with the specification P_8.2.10 to P_8.2.14. For details on the test pulse applied, see **Figure 10**.

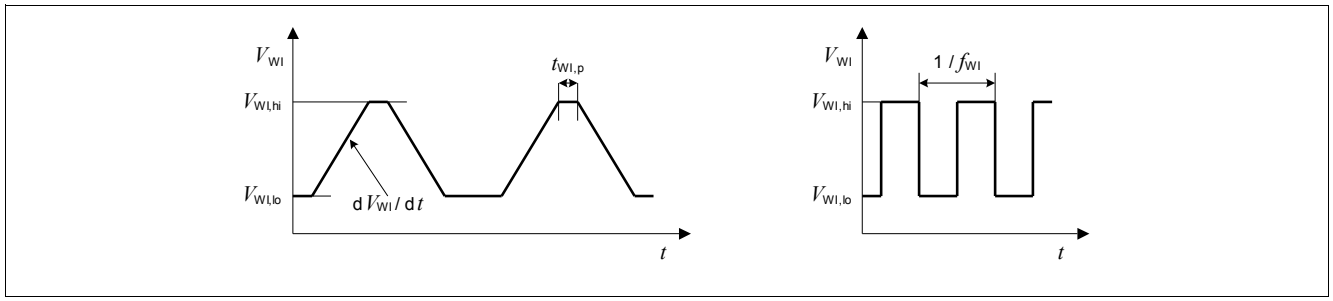


Figure 10 Test pulses watchdog input WI

Watchdog function

Watchdog timing

Positive edges at the watchdog input pin “WI” are expected within the watchdog trigger time frame $t_{WI,tr}$, otherwise a low signal at pin “WO” is generated. If a watchdog low signal at pin “WO” is generated, it remains low for $t_{WD,lo}$. All watchdog timings are defined by charging and discharging the capacitor C_D at pin “D”. Thus, the watchdog timing can be programmed by selecting C_D. For timing details see also **Figure 11**.

In case a watchdog trigger time period $t_{WI,tr}$ different from the value for $C_D = 100$ nF is required, the delay capacitor’s value can be derived from the specified value given in P_8.2.22:

$$C_D = 100\text{nF} \times t_{WI,tr} / t_{WI,tr,100nF} \quad (7.4)$$

The watchdog output low time $t_{WD,lo}$ and the watchdog period $t_{WD,p}$ then becomes:

$$t_{WD,lo} = t_{WD,lo,100nF} \times C_D / 100\ \text{nF} \quad (7.5)$$

$$t_{WD,p} = t_{WI,tr} + t_{WD,lo} \quad (7.6)$$

The formula is valid for $C_D \geq 10$nF. For precise timing calculations consider also the delay capacitor’s tolerance.

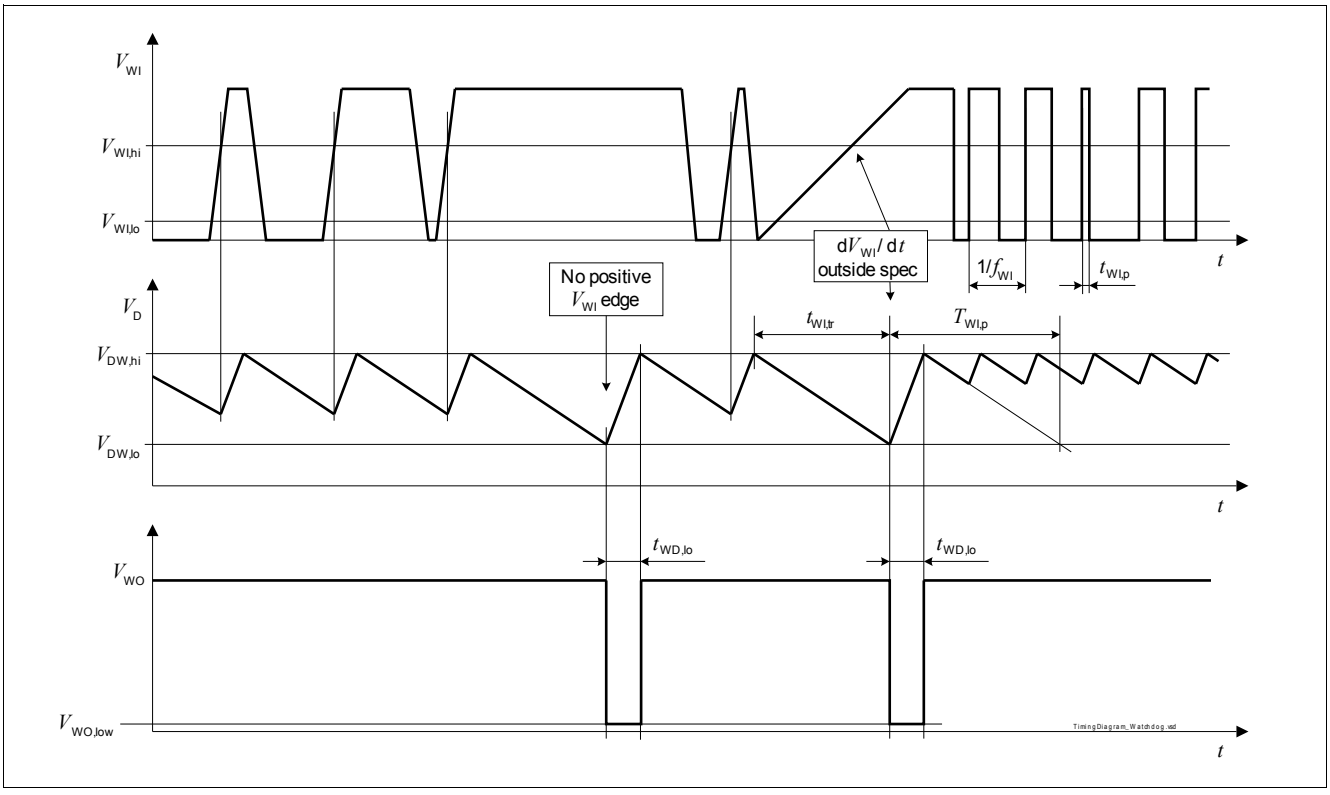


Figure 11 Timing diagram watchdog

7.2 Electrical characteristics watchdog function

Table 7 Electrical characteristics watchdog function

V_I = 13.5 V, T_j = -40°C to +150°C, all voltages with respect to ground, direction of currents as shown in **Figure 9** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Default watchdog activating threshold (pin WADJ left open)							
Watchdog activating threshold	$I_{Q,WDact,th}$	0.65	1.1	1.5	mA	I_Q increasing	P_8.2.1
Watchdog deactivating threshold	$I_{Q,WDdeact,th}$	0.55	0.9	–	mA	I_Q decreasing	P_8.2.2
Watchdog activating threshold hysteresis	$I_{Q,WDact,hy}$	50	200	–	µA	–	P_8.2.3
Adjustable watchdog activating threshold (external resistor connected to pin WADJ)							
Activating threshold	$V_{WADJ,th}$	–	693	–	mV	–	P_8.2.4
Current ratio	I_Q / I_{WADJ}	–	208	–	–	V_{WADJ} = 0V	P_8.2.5
Internal watchdog adjust resistor	$R_{WADJ,int}$	96	131	175	kΩ	–	P_8.2.6
Activating threshold factor	$F_{WDact,th}$	127	144	162	mA × kΩ	Calculated value [1]	P_8.2.7
Deactivating threshold factor	$F_{WDdeact,th}$	104	118	–	mA × kΩ	Calculated value [1]	P_8.2.8
Activating threshold switching hysteresis factor	$F_{WDact,hy}$	7	26	–	mA × kΩ	Calculated value [1]	P_8.2.9
Watchdog input WI							
Watchdog input low signal valid	$V_{WI,lo}$	–	–	0.8	V	– [2]	P_8.2.10
Watchdog input high signal valid	$V_{WI,hi}$	2.6	–	–	V	– [2]	P_8.2.11
Watchdog input high signal pulse length	$t_{WI,p}$	0.5	–	–	µs	$V_{WI} \geq V_{WI,high}$ [2]	P_8.2.12
Watchdog input signal slew rate	$\Delta V_{WI}/\Delta t$	1	–	–	V/µs	$V_{WI,low} \leq V_{WI} \leq V_{WI,high}$ [2]	P_8.2.13
Watchdog input signal frequency capture range	f_{WI}	–	–	1	MHz	Square wave, 50% duty cycle [2]	P_8.2.14

Watchdog function

Table 7 Electrical characteristics watchdog function (cont'd)

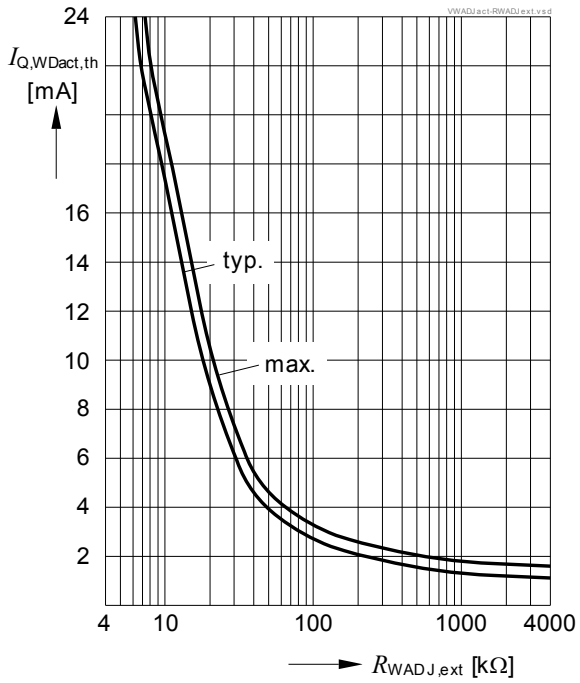
V_I = 13.5 V, T_j = -40°C to +150°C, all voltages with respect to ground, direction of currents as shown in **Figure 9** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Watchdog output WO							
Watchdog output low voltage	$V_{WO,low}$	–	0.2	0.4	V	I_{WO} = 1 mA; Watchdog active; V_{WI} = 0 V	P_8.2.15
Watchdog output maximum sink current	$I_{WO,max}$	1.5	13	30	mA	V_{WO} = 0.8 V; Watchdog active; V_{WI} = 0 V	P_8.2.16
Watchdog output internal pull-up resistor	R_{WO}	20	30	40	kΩ	–	P_8.2.17
Watchdog timing							
Delay capacitor charge current	I_D	–	2.78	–	µA	V_D = 1 V	P_8.2.18
Delay capacitor watchdog discharge current	$I_{DW,disch}$	–	1.39	–	µA	V_D = 1 V	P_8.2.19
Upper watchdog timing threshold	$V_{DW,hi}$	–	1.2	–	V	–	P_8.2.20
Lower watchdog timing threshold	$V_{DW,lo}$	–	0.7	–	V	–	P_8.2.21
Watchdog trigger time	$t_{WI,tr,100nF}$	25	36	47	ms	Calculated value; C_D = 100 nF 3)	P_8.2.22
Watchdog output low time	$t_{WD,lo,100nF}$	13	18	23	ms	Calculated value; C_D = 100 nF 3) $V_Q > V_{RT,lo}$	P_8.2.23
Watchdog period	$t_{WD,p,100nF}$	38	54	70	ms	Calculated value; $t_{WI,tr,100nF} + t_{WD,lo,100nF}$ C_D = 100 nF 3)	P_8.2.24

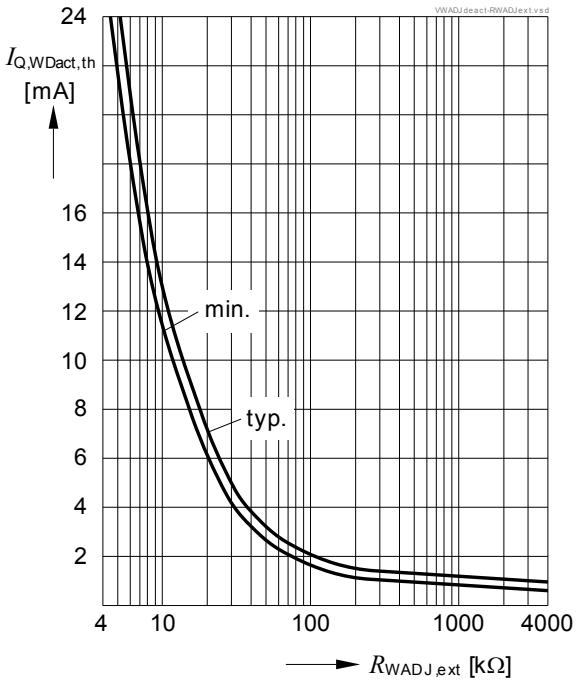
1) See **Chapter 7.1** for calculation hint.
2) For details on the test pulse applied, see **Figure 10**.
3) For programming a different watchdog timing, see **Chapter 7.1**.

7.3 Typical performance characteristics standard watchdog function

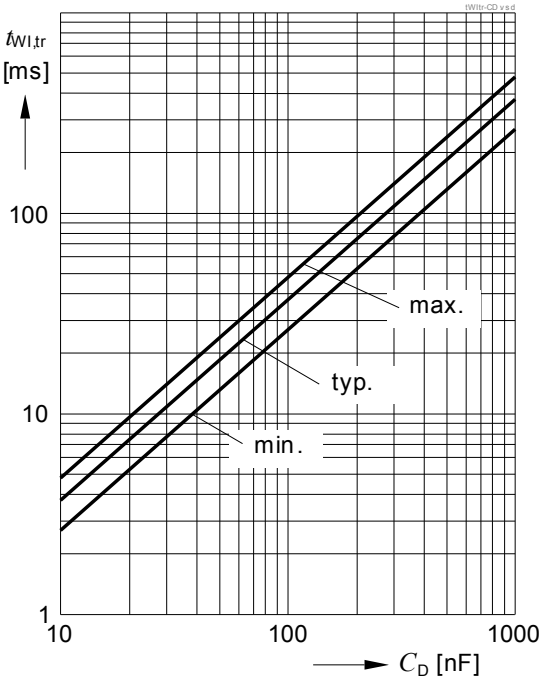
Watchdog activating threshold $V_{WADJact,th}$ vs. external resistor $R_{WADJ,ext}$



Watchdog deactivating threshold $V_{WADJdeact,th}$ vs. external resistor $R_{WADJ,ext}$



Watchdog trigger time $t_{WI,tr}$ vs. delay capacitor C_D



8 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

8.1 Application diagram

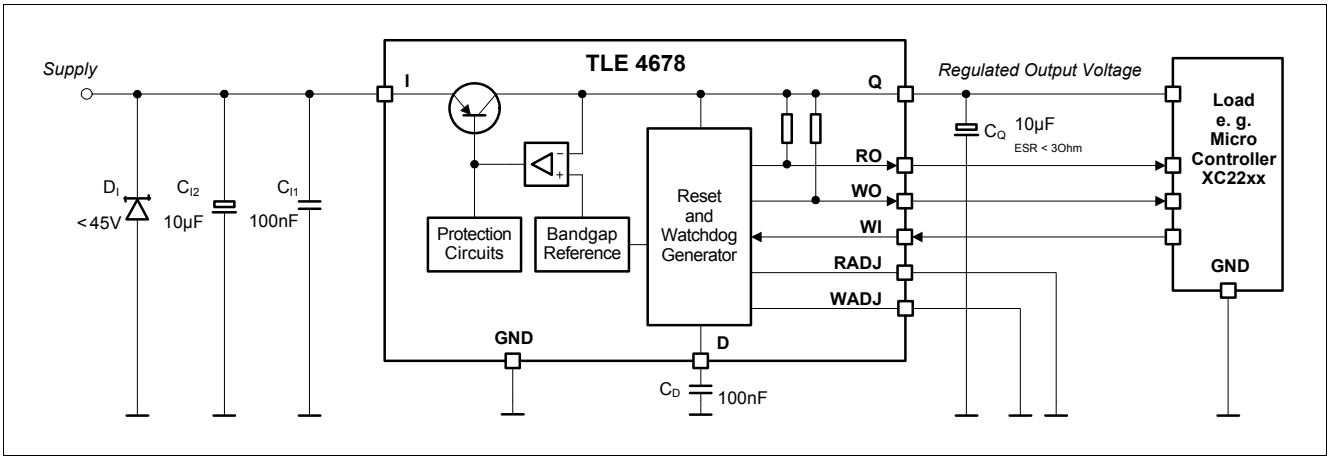


Figure 12 Application diagram with selecting default reset and watchdog activation thresholds

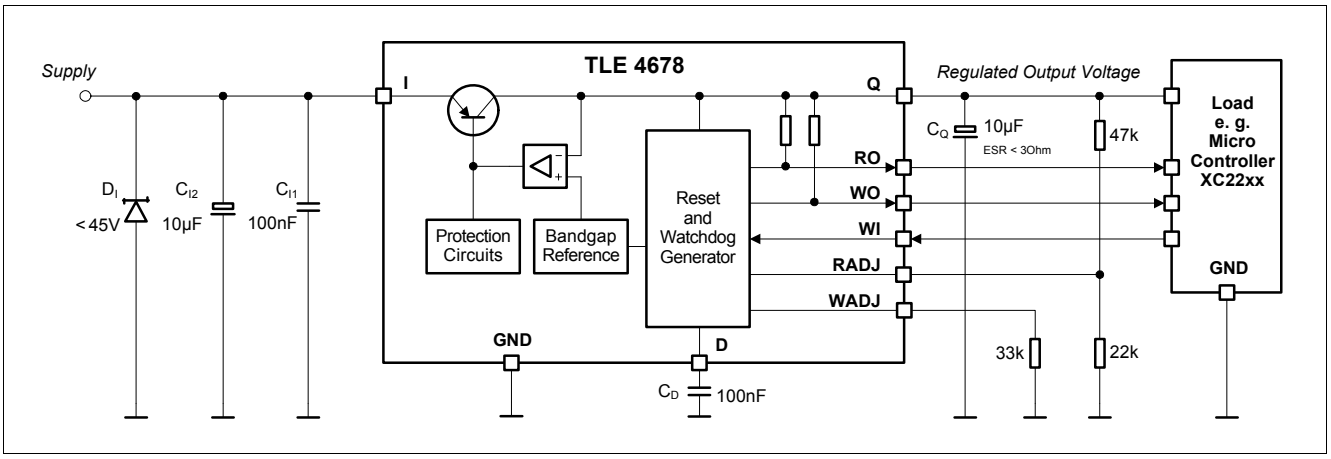


Figure 13 Application diagram with reset and watchdog activation threshold adjustment

8.2 Selection of external components

8.2.1 Input pin

The typical input circuitry for a linear voltage regulator is shown in the application diagram above.

A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line e.g. ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 µF to 470 µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to over-voltage.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in case of possible external disturbances.

8.2.2 Output pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in **Chapter 3.2**. The graph **Output capacitor series resistor ESRCQ vs. output current IQ** shows the stable operation range of the device.

TLE4678 is designed to be stable with extremely low ESR capacitors. According to the automotive environment, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator's output and GND pins and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

8.3 Thermal considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

(8.1)

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q$$

with

- P_D: continuous power dissipation
- V_I: input voltage
- V_Q: output voltage
- I_Q: output current
- I_q: quiescent current

The maximum acceptable thermal resistance R_{thJA} can then be calculated:

(8.2)

$$R_{thJA,\,max} = \frac{T_{j,\,max} - T_a}{P_D}$$

with

- $T_{j,max}$: maximum allowed junction temperature
- T_a: ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in **Chapter 3.3**.

Example

Application conditions:

V_I = 13.5 V

V_Q = 5 V

I_Q = 150 mA

T_a = 75°C

Calculation of $R_{thJA,max}$:

$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q$

= (13.5 V – 5 V) × 150 mA + 13.5 V × 8 mA

= 1.275 W + 0.108 W

= 1.383 W

$R_{thJA,max} = (T_{j,max} - T_a) / P_D$

= (150°C – 75°C) / 1.383 W

= 54.2 K/W

As a result, the PCB design must ensure a thermal resistance R_{thJA} lower than 54.2 K/W. By considering TLE4678EL (PG-SSOP-14 EP package) and according to **Chapter 3.3**, at least 600 mm^2 heatsink area is needed on the FR4 1s0p PCB, or the FR4 2s2p board can be used.

8.4 Reverse polarity protection

TLE4678 is self protected against reverse polarity faults and allows negative supply voltage. External reverse polarity diode is not needed. However, the absolute maximum ratings of the device as specified in **Chapter 3.1** must be kept.

The reverse voltage causes several small currents to flow into the IC hence increasing its junction temperature. As the thermal shut down circuitry does not work in the reverse polarity condition, designers have to consider this in their thermal design.

9 Package information

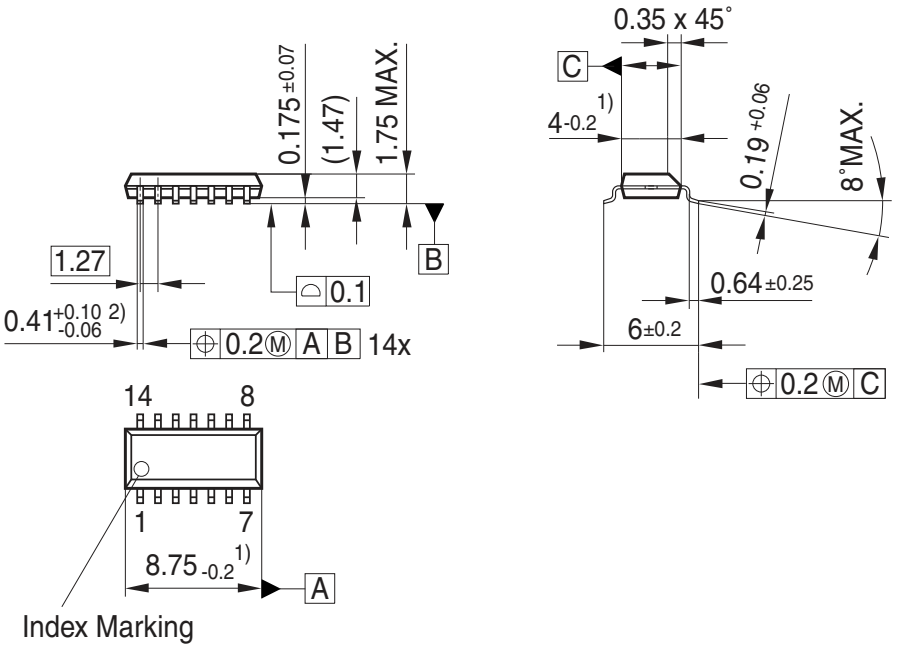


Figure 14 PG-DSO-14[1)]

1) Dimensions in mm

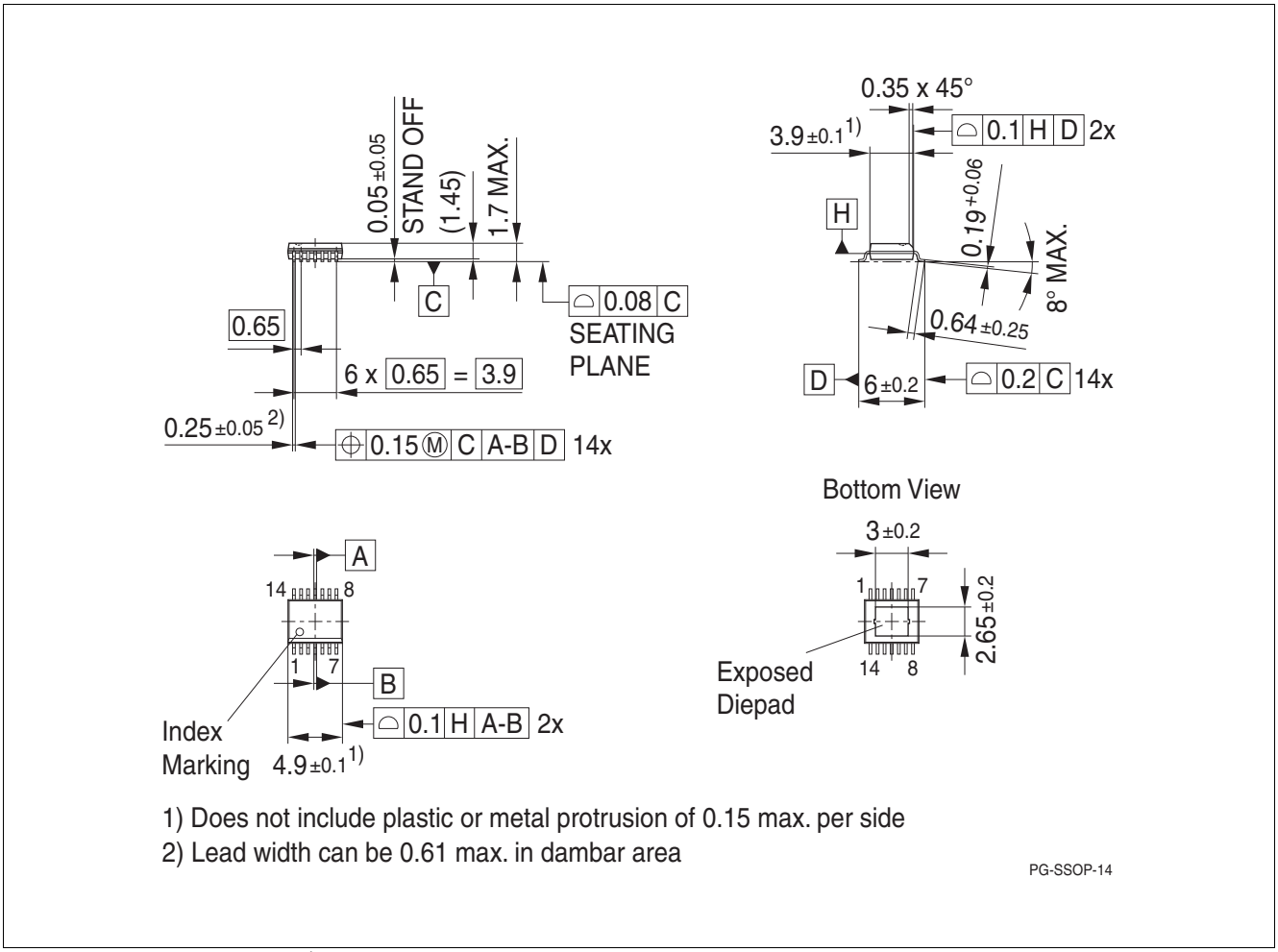


Figure 15 PG-SSOP-14[1)]

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

10 Revision history

Revision	Date	Changes
1.21	2019-09-30	Updated layout and structure Editorial changes.
1.2	2014-10-17	Typical values for I_{q1} and I_{q2} updated in **Electrical characteristics current consumption**. Chapter added: **Application information**. Package Outline PG-SSOP-14 updated: **Package information**
1.1	2009-08-27	Final datasheet version for both package variants. Modified the **Programmable watchdog activation threshold and hysteresis** description for better understanding. **Reset function**: Renamed $V_{RT,new}$ to $V_{RT,adj}$ for better understanding.
1.01	2008-08-19	Added target definition for PG-SSOP-14 package. Modifications: Overview page, thermal resistance table, pin definition, package outlines.
1.0	2008-07-31	Final datasheet initial version.

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