

OPA544

High-Voltage, High-Current OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT CURRENT: 2A min
- WIDE POWER SUPPLY RANGE:
 ± 10 to ± 35 V
- SLEW RATE: 8V/ μ s
- INTERNAL CURRENT LIMIT
- THERMAL SHUTDOWN PROTECTION
- FET INPUT: $I_B = 100$ pA max
- 5-LEAD TO-220 PLASTIC PACKAGE
- 5-LEAD SURFACE MOUNT PACKAGE

APPLICATIONS

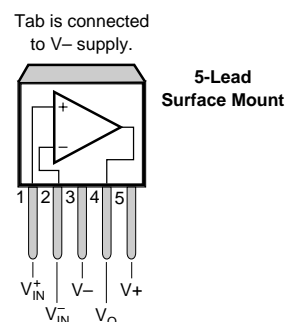
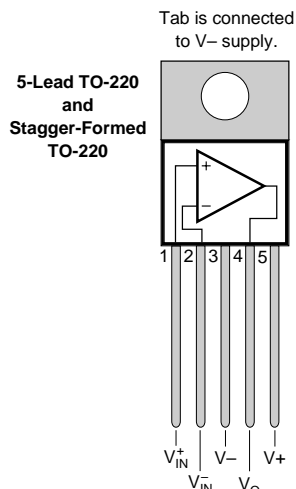
- MOTOR DRIVER
- PROGRAMMABLE POWER SUPPLY
- SERVO AMPLIFIER
- VALVES, ACTUATOR DRIVER
- MAGNETIC DEFLECTION COIL DRIVER
- AUDIO AMPLIFIER

DESCRIPTION

The OPA544 is a high-voltage/high-current operational amplifier suitable for driving a wide variety of high power loads. High performance FET op amp circuitry and high power output stage are combined on a single monolithic chip.

The OPA544 is protected by internal current limit and thermal shutdown circuits.

The OPA544 is available in industry-standard 5-lead TO-220 and 5-lead surface-mount power packages. Its copper tab allows easy mounting to a heat sink for excellent thermal performance. It is specified for operation over the extended industrial temperature range, -40°C to $+85^{\circ}\text{C}$.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: <http://www.burr-brown.com/> • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

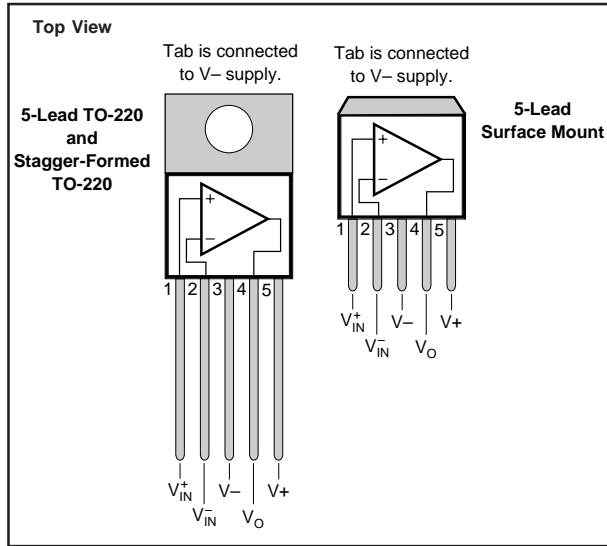
At $T_{CASE} = +25^{\circ}C$, $V_S = \pm 35V$, unless otherwise noted.

| PARAMETER | CONDITION | OPA544T OPA544T-1 OPA544F | | | UNITS |
|---|---|--|---|---|---|
| | | MIN | TYP | MAX | |
| OFFSET VOLTAGE Input Offset Voltage vs Temperature vs Power Supply | Specified Temperature Range $V_S = \pm 10V$ to $\pm 35V$ | | ± 1 ± 10 ± 10 | ± 5 ± 100 | mV $\mu V/^{\circ}C$ $\mu V/V$ |
| INPUT BIAS CURRENT ⁽¹⁾ Input Bias Current vs Temperature Input Offset Current | | $V_{CM} = 0V$ $V_{CM} = 0V$ | | ± 15 See Typical Curve ± 10 | ± 100 ± 100 |
| NOISE Input Voltage Noise Noise Density, $f = 1kHz$ Current Noise Density, $f = 1kHz$ | | | 36 3 | | nV/\sqrt{Hz} fA/\sqrt{Hz} |
| INPUT VOLTAGE RANGE Common-Mode Input Range, Positive Negative Common-Mode Rejection | Linear Operation Linear Operation $V_{CM} = \pm V_S - 6V$ | (V+) -6 (V-) +6 90 | (V+) -4 (V-) +4 106 | | V V dB |
| INPUT IMPEDANCE Differential Common-Mode | | | $10^{12} \parallel 8$ $10^{12} \parallel 10$ | | $\Omega \parallel pF$ $\Omega \parallel pF$ |
| OPEN-LOOP GAIN Open-Loop Voltage Gain | $V_O = \pm 30V$, $R_L = 1k\Omega$ | 90 | 103 | | dB |
| FREQUENCY RESPONSE Gain Bandwidth Product Slew Rate Full-Power Bandwidth Settling Time 0.1% Total Harmonic Distortion | $R_L = 15\Omega$ $60Vp-p$, $R_L = 15\Omega$ $G = -10$, 60V Step | 5 | 1.4 8 See Typical Curve 25 See Typical Curve | | MHz V/ μs μs |
| OUTPUT Voltage Output, Positive Negative Positive Negative Current Output Short-Circuit Current | $I_O = 2A$ $I_O = 2A$ $I_O = 0.5A$ $I_O = 0.5A$ | (V+) -5 (V-) +5 (V+) -4.2 (V-) +4 | (V+) -4.4 (V-) +3.8 (V+) -3.8 (V-) +3.1 See SOA Curves 4 | | V V V V A |
| POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current | $I_O = 0$ | ± 10 | ± 35 ± 12 | ± 35 ± 15 | V V mA |
| TEMPERATURE RANGE Operating Storage Thermal Resistance, θ_{JC} Thermal Resistance, θ_{JC} Thermal Resistance, θ_{JA} | $f > 50Hz$ DC No Heat Sink | -40 -40 | 2.7 3 65 | +85 +125 | $^{\circ}C$ $^{\circ}C$ $^{\circ}C/W$ $^{\circ}C/W$ $^{\circ}C/W$ |

NOTES: (1) High-speed test at $T_J = 25^{\circ}C$.

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CONNECTION DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

| | |
|--|------------------------------------|
| Supply Voltage, V^+ to V^- | 70V |
| Output Current | See SOA Curve |
| Input Voltage | (V^-) -0.7V to (V^+) +0.7V |
| Operating Temperature | -40°C to +125°C |
| Storage Temperature | -40°C to +125°C |
| Junction Temperature | 150°C |
| Lead Temperature (soldering -10s) ⁽¹⁾ | 300°C |

NOTE: (1) Vapor-phase or IR reflow techniques are recommended for soldering the OPA544F surface mount package. Wave soldering is not recommended due to excessive thermal shock and "shadowing" of nearby devices.

PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER ⁽¹⁾ |
|-----------|------------------------------|---------------------------------------|
| OPA544T | 5-Lead TO-220 | 315 |
| OPA544T-1 | 5-Lead Stagger-Formed TO-220 | 323 |
| OPA544F | 5-Lead Surface-Mount | 325 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

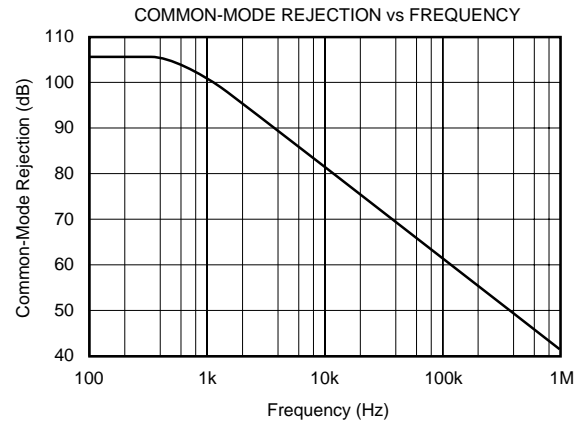
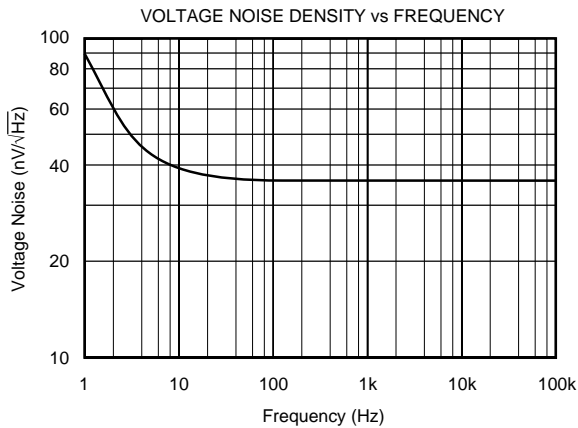
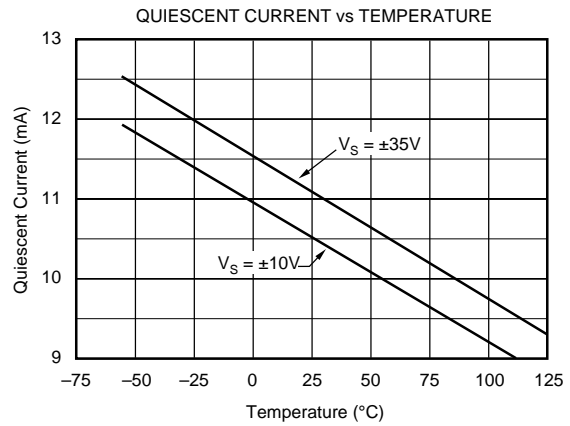
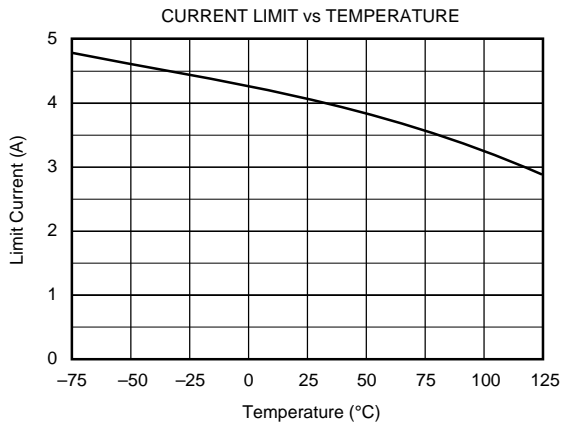
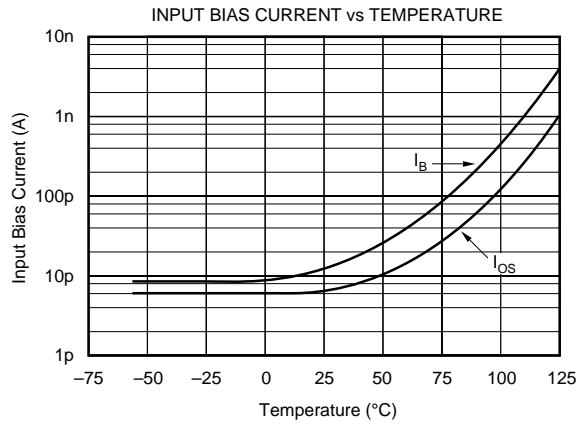
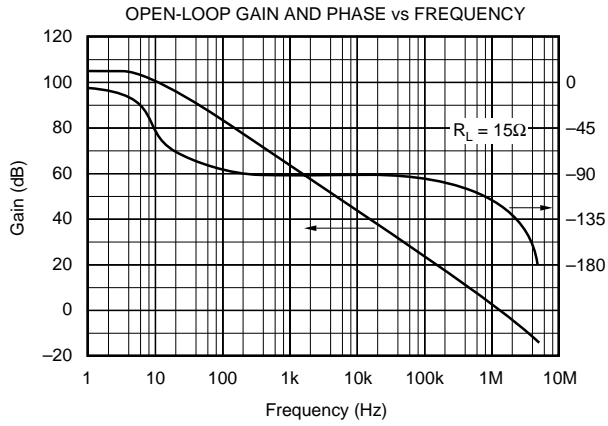
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

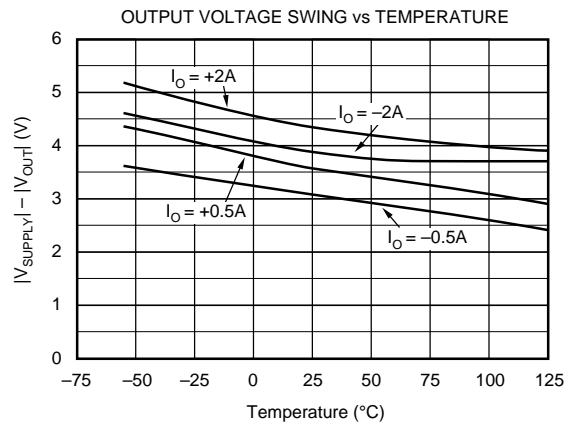
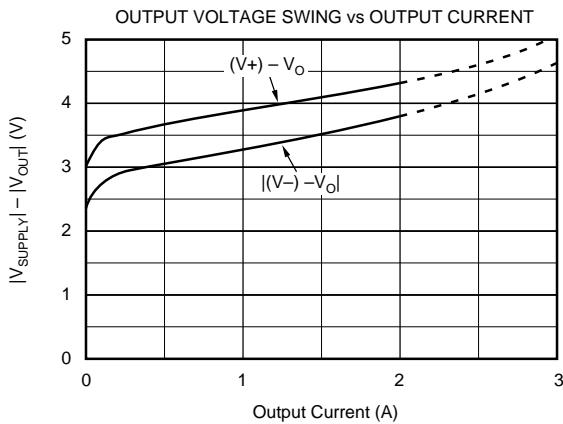
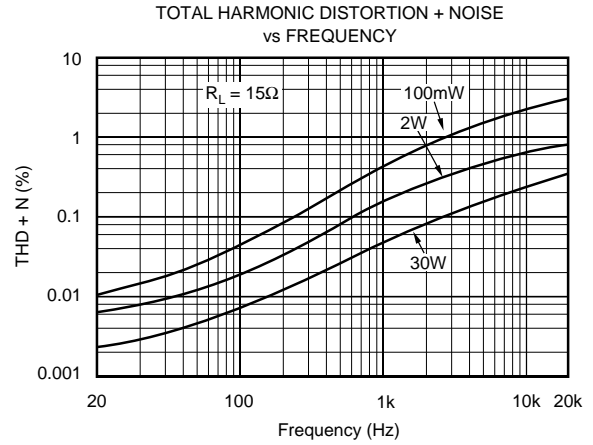
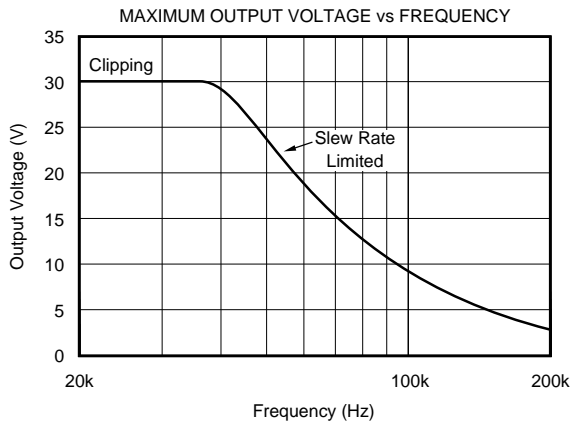
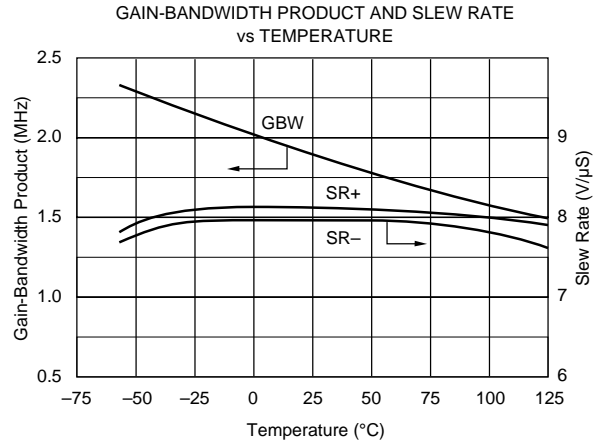
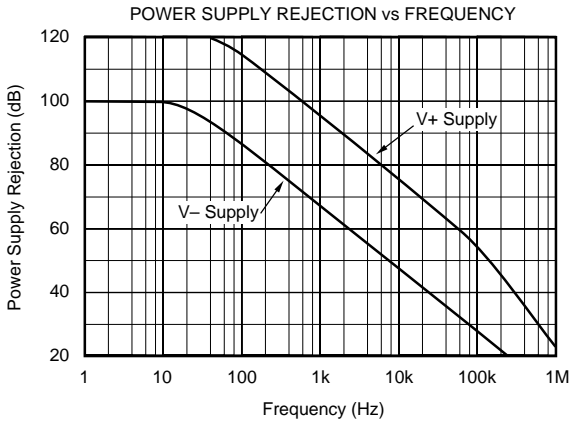
TYPICAL PERFORMANCE CURVES

At $T_{CASE} = +25^{\circ}\text{C}$, $V_S = \pm 35\text{V}$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

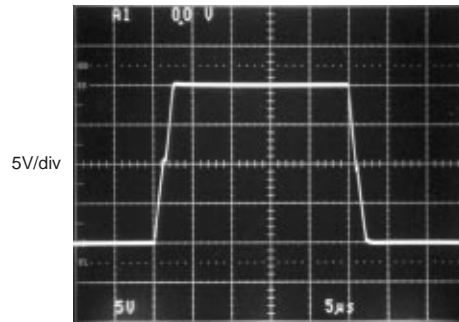
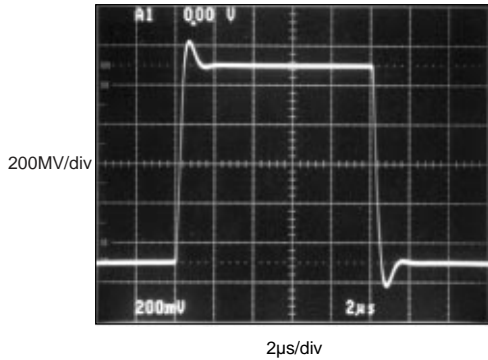
At $T_{CASE} = +25^{\circ}C$, $V_S = \pm 35V$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_{CASE} = +25^{\circ}C$, $V_S = \pm 35V$, unless otherwise noted.

SMALL SIGNAL RESPONSE
 $G = 3$, $C_L = 1nF$



APPLICATIONS INFORMATION

Figure 1 shows the OPA544 connected as a basic non-inverting amplifier. The OPA544 can be used in virtually any op amp configuration. Power supply terminals should be bypassed with low series impedance capacitors. The technique shown, using a ceramic and tantalum type in parallel is recommended. Power supply wiring should have low series impedance and inductance.

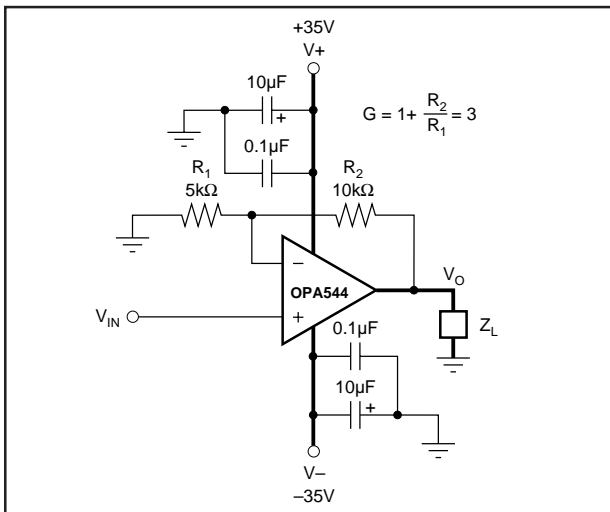


FIGURE 1. Basic Circuit Connections.

SAFE OPERATING AREA

Stress on the output transistors is determined by the output current and the voltage across the conducting output transistor, $V_S - V_O$. The power dissipated by the output transistor is equal to the product of the output current and the voltage across the conducting transistor, $V_S - V_O$. The Safe Operating Area (SOA curve, Figure 2) shows the permissible range of voltage and current.

The safe output current decreases as $V_S - V_O$ increases. Output short-circuits are a very demanding case for SOA. A short-circuit to ground forces the full power supply voltage ($V+$ or $V-$) across the conducting transistor. With $V_S = \pm 35V$ the safe output current is 1.5A (at $25^{\circ}C$). The short-circuit current is approximately 4A which exceeds the SOA. This situation will activate the thermal shutdown circuit in the OPA544. For further insight on SOA, consult Application Bulletin AB-039.

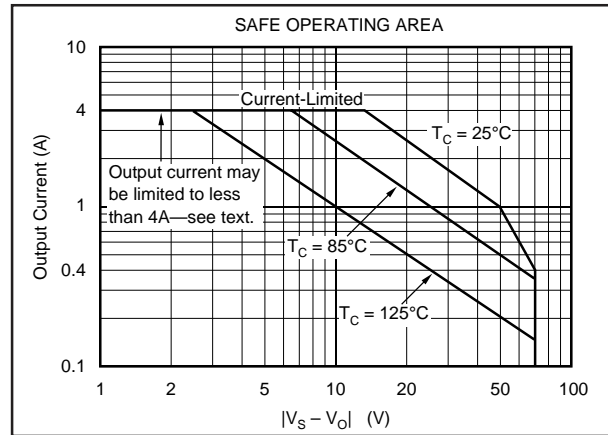


FIGURE 2. Safe Operating Area.

CURRENT LIMIT

The OPA544 has an internal current limit set for approximately 4A. This current limit decreases with increasing junction temperature as shown in the typical curve, Current Limit vs Temperature. This, in combination with the thermal shutdown circuit, provides protection from many types of overload. It may not, however, protect for short-circuit to ground, depending on the power supply voltage, ambient temperature, heat sink and signal conditions.

POWER DISSIPATION

Power dissipation depends on power supply, signal and load conditions. For dc signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor. Power dissipation can be minimized by using the lowest possible power supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a dc output voltage of one-half the power supply voltage. Dissipation with ac signals is lower. Application Bulletin AB-039 explains how to calculate or measure power dissipation with unusual signals and loads.

HEATSINKING

Most applications require a heat sink to assure that the maximum junction temperature is not exceeded. The heat sink required depends on the power dissipated and on ambient conditions. Consult Application Bulletin AB-038 for information on determining heat sink requirements.

The mounting tab of the surface-mount package version should be soldered to a circuit board copper area for good heat dissipation. Figure 3 shows typical thermal resistance from junction to ambient as a function of the copper area.

THERMAL PROTECTION

The OPA544 has thermal shutdown that protects the amplifier from damage. Any tendency to activate the thermal shutdown circuit during normal operation is indication of excessive power dissipation or an inadequate heat sink.

The thermal protection activates at a junction temperature of approximately 155°C. For reliable operation, junction temperature should be limited to 150°C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is activated. Use worst-case load and signal conditions. For good reliability, the thermal protection should trigger more than 25°C above the maximum expected ambient condition of your application. This produces a junction temperature of 125°C at the maximum expected ambient condition.

Depending on load and signal conditions, the thermal protection circuit may produce a duty-cycle modulated output signal. This limits the dissipation in the amplifier, but the rapidly varying output waveform may be damaging to some loads. The thermal protection may behave differently depending on whether internal dissipation is produced by sourcing or sinking output current.

OUTPUT STAGE COMPENSATION

The complex load impedances common in power op amp applications can cause output stage instability. Figure 3 shows an output series R/C compensation network (1Ω in series with 0.01μF) which generally provides excellent stability. Some variation in circuit values may be required with certain loads.

UNBALANCED POWER SUPPLIES

Some applications do not require equal positive and negative output voltage swing. The power supply voltages of the OPA544 do not need to be equal. For example, a -6V negative power supply voltage assures that the inputs of the OPA544 are operated within their linear common-mode range, and that the output can swing to 0V. The V+ power supply could range from 15V to 65V. The total voltage (V- to V+) can range from 20V to 70V. With a 65V positive supply voltage, the device may not be protected from damage during short-circuits because of the larger V_{CE} during this condition.

OUTPUT PROTECTION

Reactive and EMF-generating loads can return load current to the amplifier, causing the output voltage to exceed the power supply voltage. This damaging condition can be avoided with clamp diodes from the output terminal to the power supplies as shown in Figure 4. Fast-recovery rectifier diodes with a 4A or greater continuous rating are recommended.

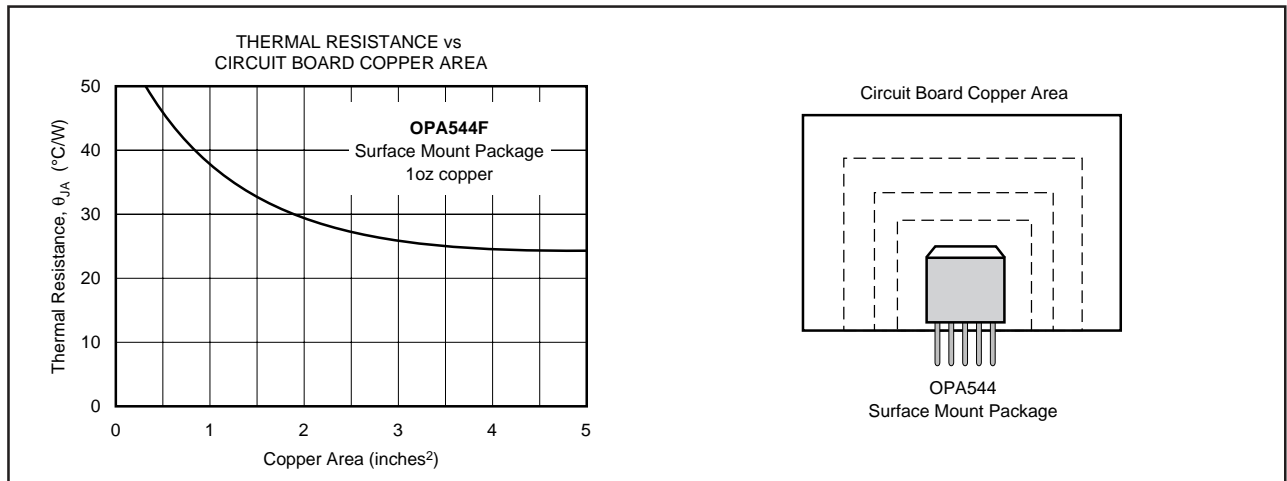


FIGURE 3. Thermal Resistance vs Circuit Board Copper Area.

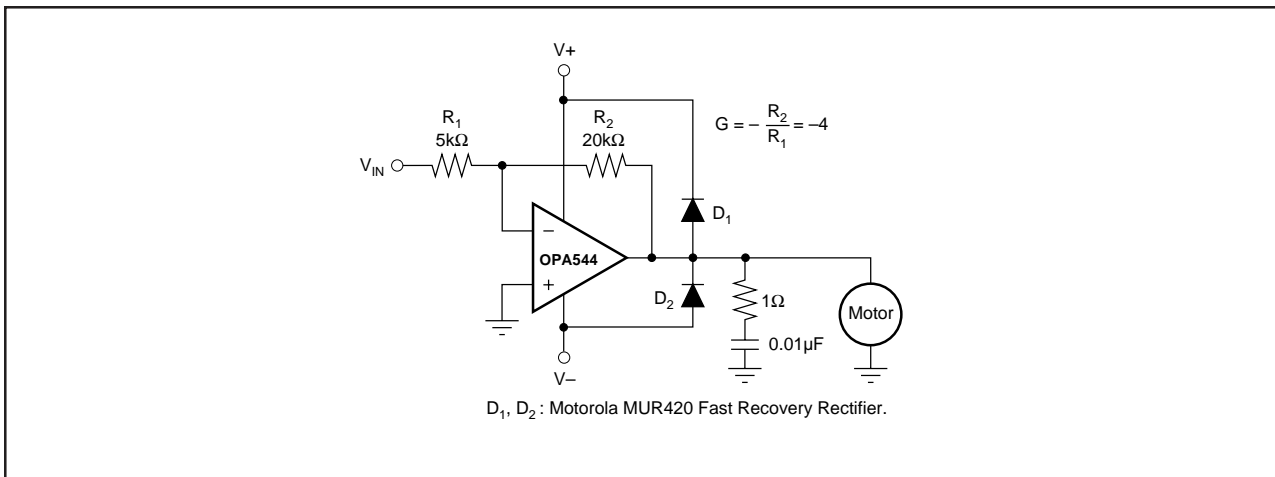


FIGURE 4. Motor Drive Circuit.

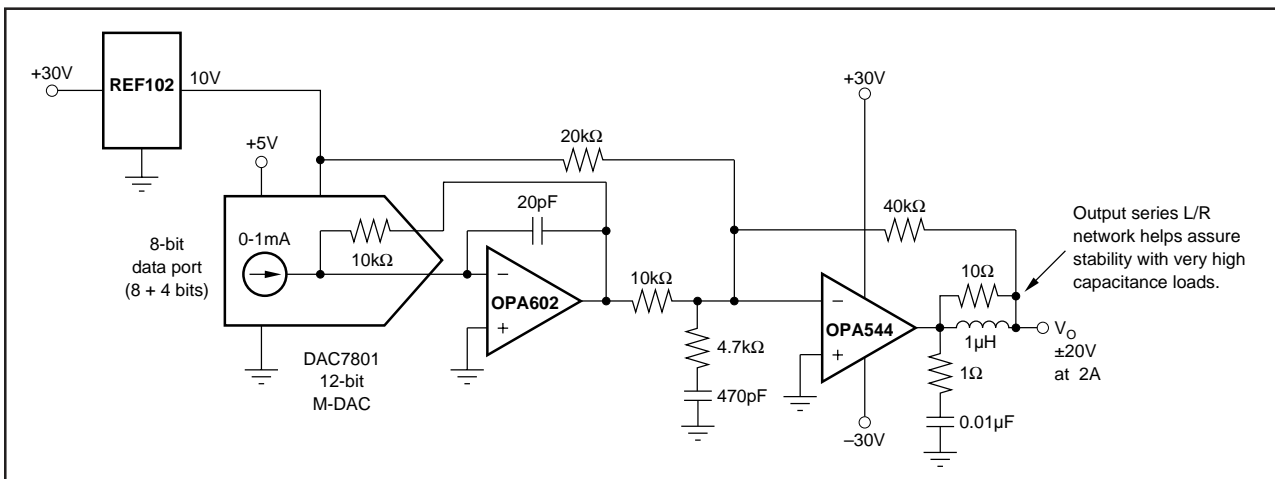


FIGURE 5. Digitally Programmable Power Supply.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|------------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| OPA544F/500 | ACTIVE | DDPAK/ TO-263 | KTT | 5 | 500 | RoHS & Green | Call TI SN | Level-2-260C-1 YEAR | | OPA544F | Samples |
| OPA544FKTTT | ACTIVE | DDPAK/ TO-263 | KTT | 5 | 250 | RoHS & Green | Call TI SN | Level-2-260C-1 YEAR | | OPA544F | Samples |
| OPA544FKTTTG3 | LIFEBUY | DDPAK/ TO-263 | KTT | 5 | 250 | RoHS & Green | SN | Level-2-260C-1 YEAR | | OPA544F | |
| OPA544T | ACTIVE | TO-220 | KC | 5 | 49 | RoHS & Green | Call TI SN | N / A for Pkg Type | -40 to 85 | OPA544T | Samples |
| OPA544TG3 | LIFEBUY | TO-220 | KC | 5 | 49 | RoHS & Green | SN | N / A for Pkg Type | -40 to 85 | OPA544T | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------|--------------|--------------|------|-----|--------|--------|--------|--------|
| OPA544T | KC | TO-220 | 5 | 49 | 546 | 31 | 11930 | 3.17 |
| OPA544TG3 | KC | TO-220 | 5 | 49 | 546 | 31 | 11930 | 3.17 |

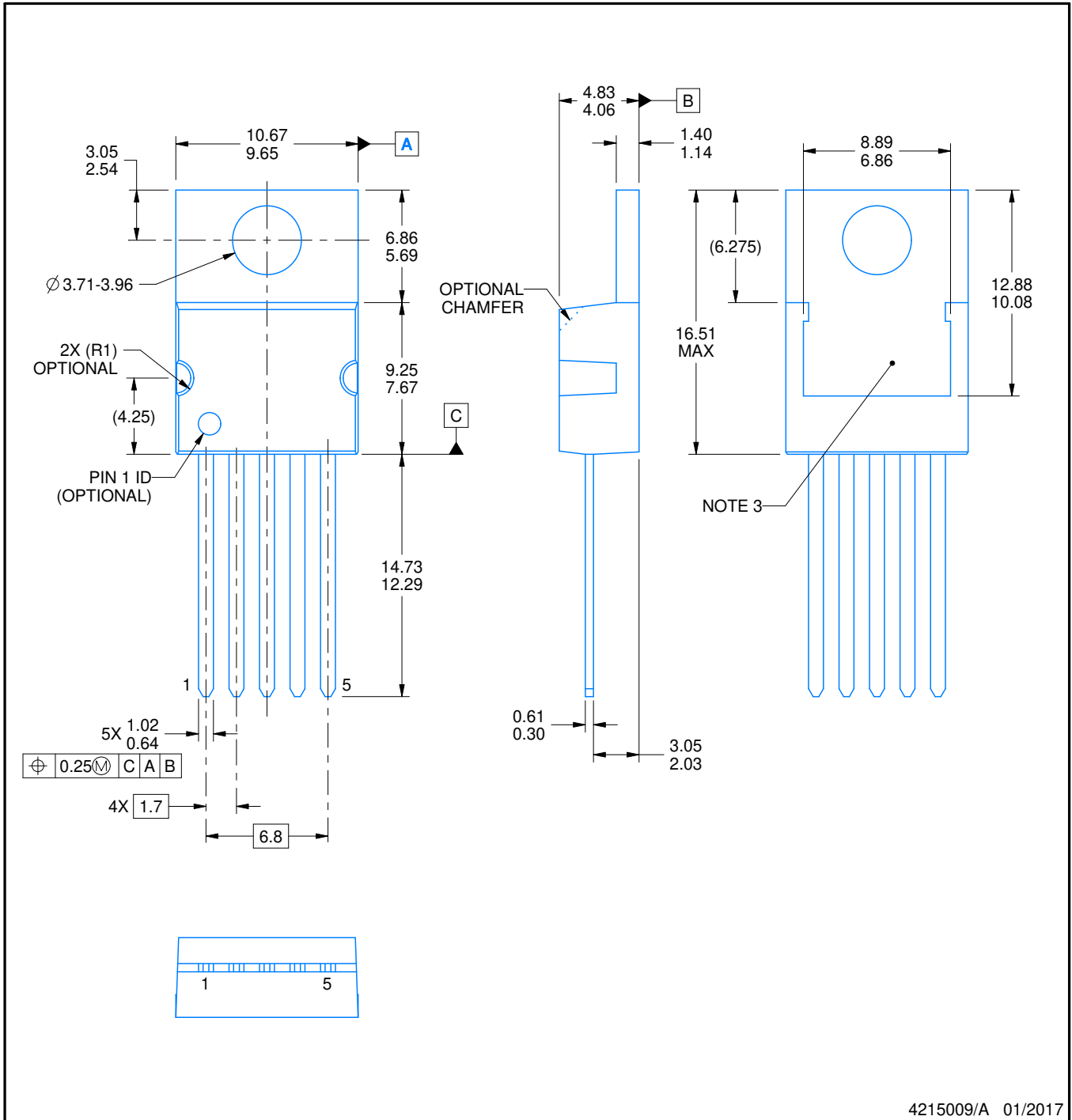
KC0005A



PACKAGE OUTLINE

TO-220 - 16.51 mm max height

TO-220



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NOTES:

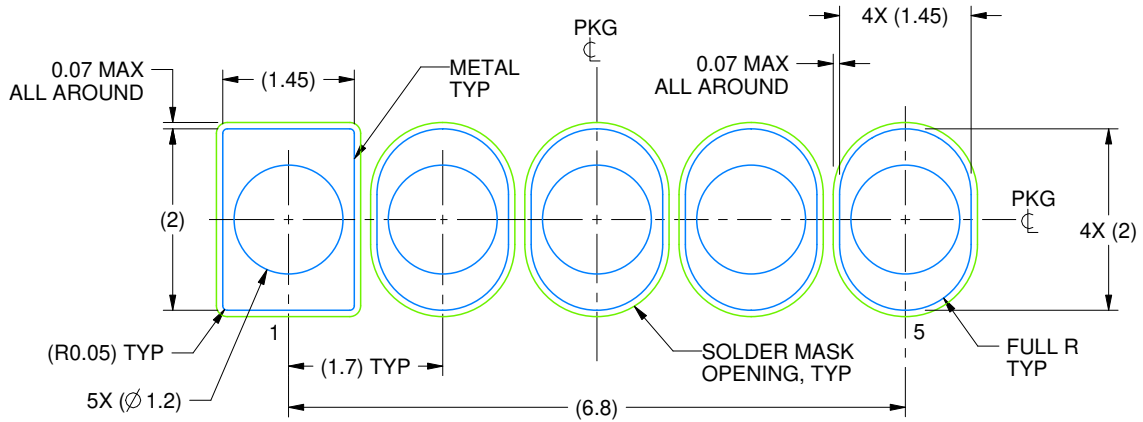
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.

EXAMPLE BOARD LAYOUT

KC0005A

TO-220 - 16.51 mm max height

TO-220

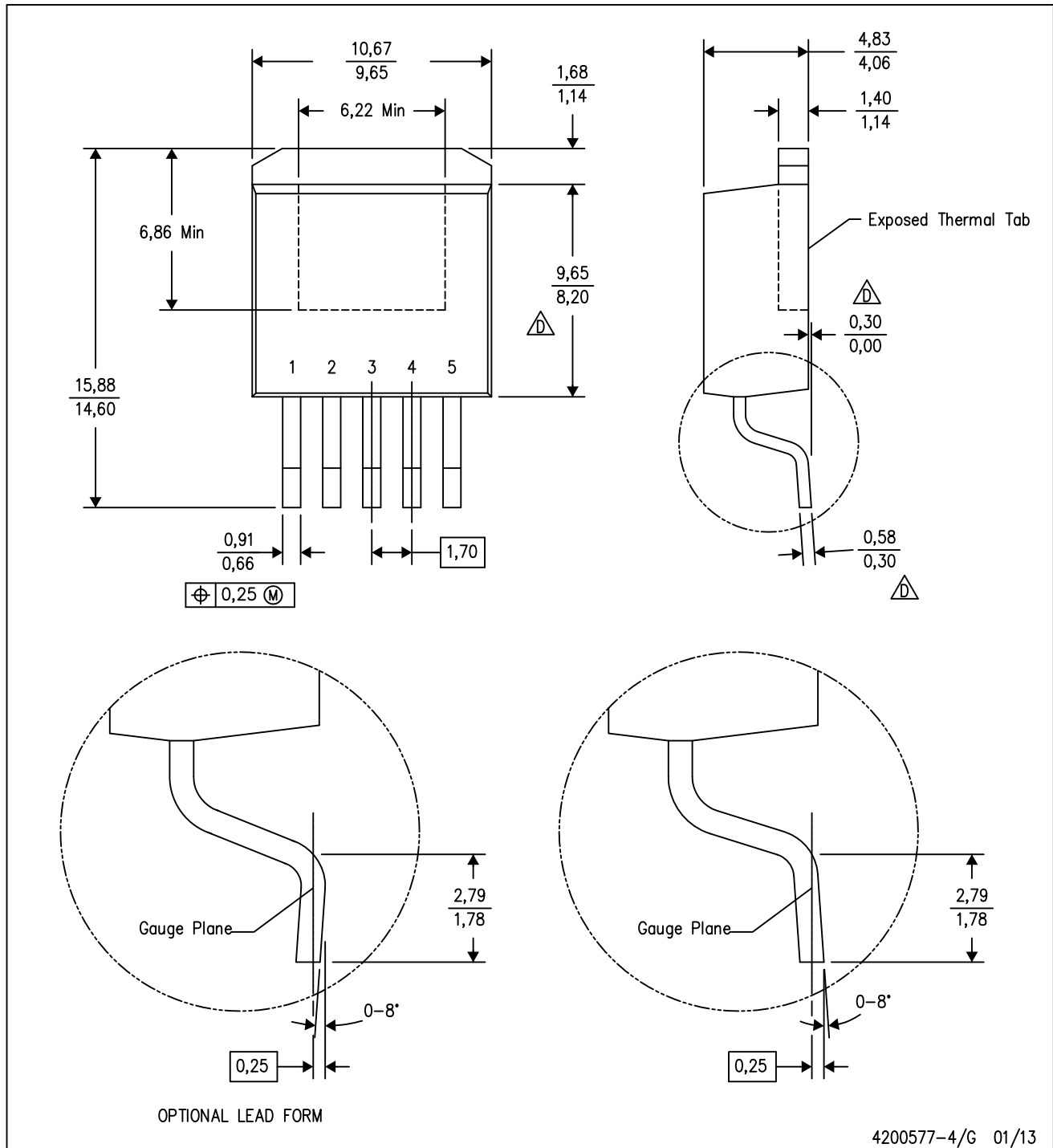


LAND PATTERN
NON-SOLDER MASK DEFINED
SCALE:12X

4215009/A 01/2017

KTT (R-PSFM-G5)

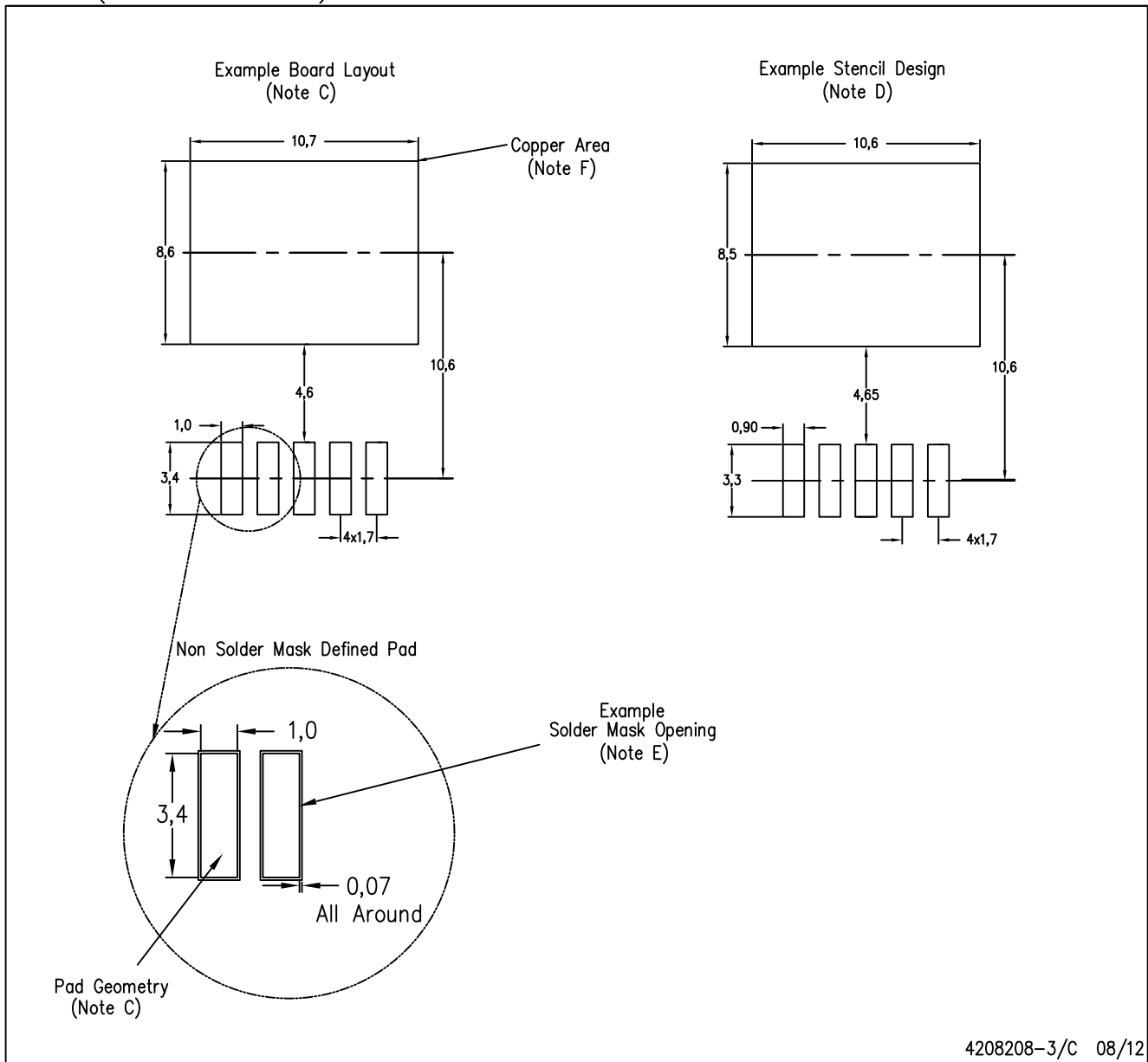
PLASTIC FLANGE-MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- △ Falls within JEDEC TO-263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R-PSFM-G5)

PLASTIC FLANGE-MOUNT PACKAGE



4208208-3/C 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-SM-782 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
 - This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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