

MC14066B

QUAD ANALOG SWITCH/QUAD MULTIPLEXER

The MC14066B consists of four independent switches capable of controlling either digital or analog signals. This quad bilateral switch is useful in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

The MC14066B is designed to be pin-for-pin compatible with the MC14016B, but has much lower ON resistance. Input voltage swings as large as the full supply voltage can be controlled via each independent control input.

- Triple Diode Protection on All Control Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise — 12 nV/ $\sqrt{\text{Cycle}}$, $f \geq 1.0$ kHz typical
- Pin-for-Pin Replacement for CD4016, CD4016, MC14016B
- For Lower R_{ON} , Use The HC4066 High-Speed CMOS Device

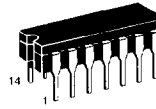
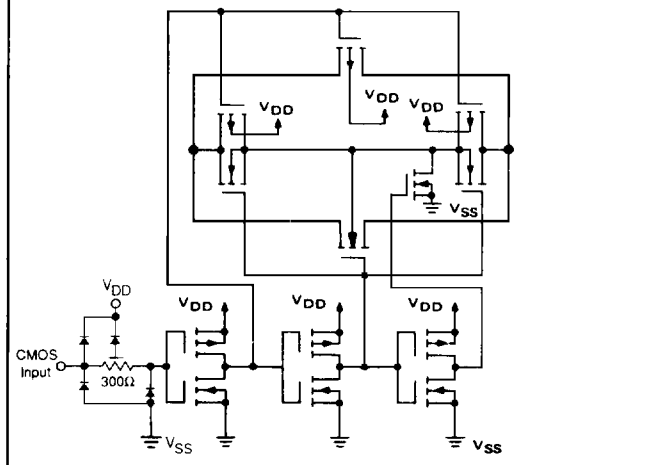
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}	Input Current (DC or Transient), per Control Pin	± 10	mA
I_{sw}	Switch Through Current	± 25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

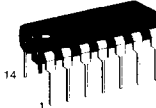
*Maximum Ratings are those values beyond which damage to the device may occur.
 †Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
 Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

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CIRCUIT SCHEMATIC (1/4 OF DEVICE SHOWN)



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646

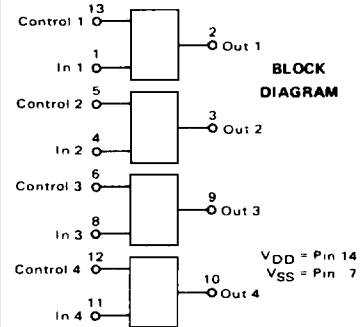


D SUFFIX
SOIC
CASE 751A

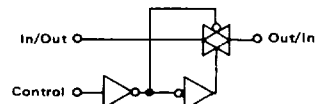
ORDERING INFORMATION

MC14XXXBCP Plastic
 MC14XXXBCL Ceramic
 MC14XXXBD SOIC

$T_A = -55^\circ$ to 125°C for all packages.



LOGIC DIAGRAM AND TRUTH TABLE (1/4 OF DEVICE SHOWN)



Control	Switch
0 = V_{SS}	OFF
1 = V_{DD}	ON

Logic Diagram Restrictions
 $V_{SS} \leq V_{in} \leq V_{DD}$
 $V_{SS} \leq V_{out} \leq V_{DD}$

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V _{DD}	Test Conditions	-55°C		25°C			125°C		Unit	
				Min	Max	Min	Typ #	Max	Min	Max		
SUPPLY REQUIREMENTS (Voltages Referenced to V _{EE})												
Power Supply Voltage Range	V _{DD}	—		3.0	18	3.0	—	18	3.0	18	V	
Quiescent Current Per Package	I _{DD}	5.0 10 15	Control Inputs: V _{in} = V _{SS} or V _{DD} . Switch I/O: V _{SS} ≤ V _{I/O} ≤ V _{DD} , and ΔV _{switch} ≤ 500 mV**	— — —	0.25 0.5 1.0	— — —	0.005 0.010 0.015	0.25 0.5 1.0	— — —	7.5 15 30	μA	
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I _{D(AV)}	5.0 10 15	T _A = 25°C only The channel component, (V _{in} - V _{out})/R _{on} , is not included.)	Typical (0.07 μA/kHz)f - I _{DD} (0.20 μA/kHz)f + I _{DD} (0.36 μA/kHz)f + I _{DD}								μA
CONTROL INPUTS (Voltages Referenced to V _{SS})												
Low-Level Input Voltage	V _{IL}	5.0 10 15	R _{on} = per spec, I _{off} = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V	
High-Level Input Voltage	V _{IH}	5.0 10 15	R _{on} = per spec, I _{off} = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V	
Input Leakage Current	I _{in}	15	V _{in} = 0 or V _{DD}	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA	
Input Capacitance	C _{in}	—		—	—	—	5.0	7.5	—	—	pF	
SWITCHES IN AND OUT (Voltages Referenced to V _{SS})												
Recommended Peak-to-Peak Voltage Into or Out of the Switch	V _{I/O}	—	Channel On or Off	0	V _{DD}	0	—	V _{DD}	0	V _{DD}	V _{p-p}	
Recommended Static or Dynamic Voltage Across the Switch* (Figure 1)	ΔV _{switch}	—	Channel On	0	600	0	—	600	0	300	mV	
Output Offset Voltage	V _{OO}	—	V _{in} = 0 V, No Load	—	—	—	10	—	—	—	μV	
ON Resistance	R _{on}	5.0 10 15	ΔV _{switch} ≤ 500 mV**, V _{in} = V _{IL} or V _{IH} (Control), and V _{in} = 0 to V _{DD} (Switch)	— — —	800 400 220	— — —	250 120 80	1050 500 280	— — —	1200 520 300	Ω	
ΔON Resistance Between Any Two Channels in the Same Package	ΔR _{on}	5.0 10 15		— — —	70 50 45	— — —	25 10 10	70 50 45	— — —	135 95 65	Ω	
Off-Channel Leakage Current (Figure 6)	I _{off}	15	V _{in} = V _{IL} or V _{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA	
Capacitance, Switch I/O	C _{I/O}	—	Switch Off	—	—	—	10	15	—	—	pF	
Capacitance, Feedthrough (Switch Off)	C _{I/O}	—		—	—	—	0.47	—	—	—	pF	

*Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

**For voltage drops across the switch (ΔV_{switch}) >600 mV (>300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

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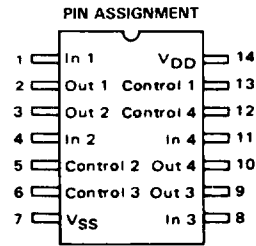
ELECTRICAL CHARACTERISTICS* ($C_L = 50$ pF, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	VDD Vdc	Min	Typ #	Max	Unit	
Propagation Delay Times $V_{SS} = 0$ Vdc Input to Output ($R_L = 10$ k Ω) $t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) C_L - 15.5 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) C_L - 6.0 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) C_L + 4.0 \text{ ns}$ Control to Output ($R_L = 1$ k Ω) (Figure 2) Output "1" to High Impedance Output "0" to High Impedance High Impedance to Output "1" High Impedance to Output "0"	t_{PLH}, t_{PHL}	5.0 10 15	— — —	20 10 7.0	40 20 15	ns	
	t_{PHZ}	5.0 10 15	— — —	40 35 30	80 70 60	ns	
	t_{PLZ}	5.0 10 15	— — —	40 35 30	80 70 60	ns	
	t_{PZH}	5.0 10 15	— — —	60 20 15	120 40 30	ns	
	t_{PZL}	5.0 10 15	— — —	60 20 15	120 40 30	ns	
	Second Harmonic Distortion $V_{SS} = -5$ Vdc $(V_{in} = 1.77$ Vdc, RMS Centered @ 0.0 Vdc, $R_L = 10$ k Ω , $f = 1.0$ kHz)	—	5.0	—	0.1	—	%
	Bandwidth (Switch ON) (Figure 3) $(R_L = 1$ k Ω , $20 \text{ Log } \frac{V_{out}}{V_{in}} = -3$ dB, $C_L = 50$ pF, $V_{in} = 5$ V _{p-p})	—	5.0	—	65	—	MHz
	Feedthrough Attenuation (Switch OFF) $V_{SS} = -5$ Vdc $(V_{in} = 5$ V _{p-p} , $R_L = 1$ k Ω , $f_{in} = 1.0$ MHz) (Figure 3)	—	5.0	—	-50	—	dB
	Channel Separation (Figure 4) $V_{SS} = -5$ Vdc $(V_{in} = 5$ V _{p-p} , $R_L = 1$ k Ω , $f_{in} = 8.0$ MHz) (Switch A ON, Switch B OFF)	—	5.0	—	-50	—	dB
	Crosstalk. Control Input to Signal Output (Figure 5) $V_{SS} = -5$ Vdc $(R_1 = 1$ k Ω , $R_L = 10$ k Ω , Control $t_{TLH} = t_{THL} = 20$ ns)	—	5.0	—	300	—	mV _{p-p}

*The formulas given are for the typical characteristics only at 25°C
 #Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



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TEST CIRCUITS

FIGURE 1 — ΔV ACROSS SWITCH

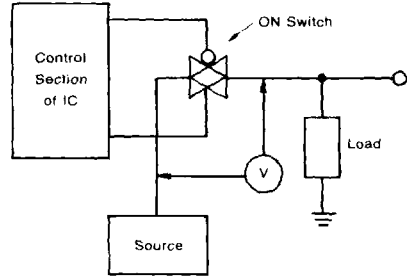


FIGURE 2 — TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

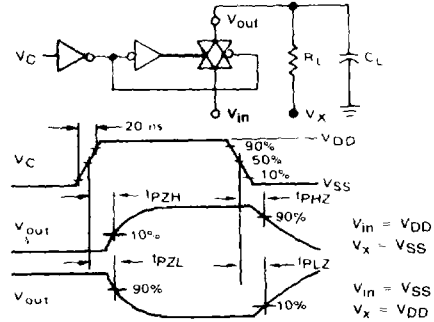


FIGURE 3 — BANDWIDTH AND FEEDTHROUGH ATTENUATION

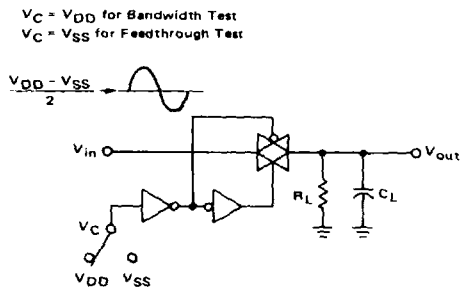


FIGURE 4 — CHANNEL SEPARATION

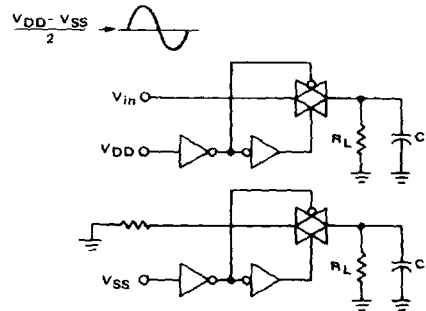


FIGURE 5 — CROSSTALK, CONTROL TO OUTPUT

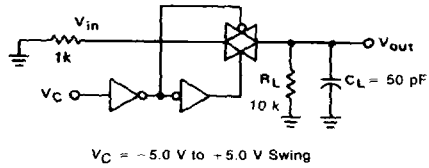
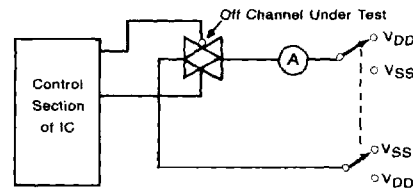
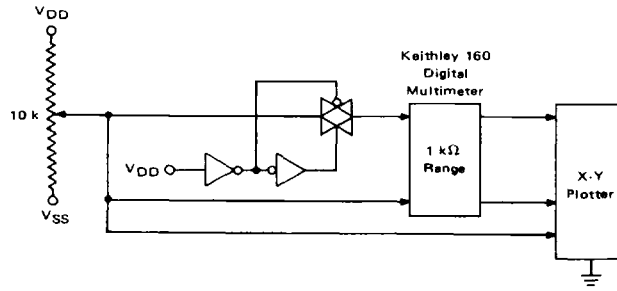


FIGURE 6 — OFF CHANNEL LEAKAGE



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FIGURE 7 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 8 – $V_{DD} = 7.5\text{ V}$, $V_{SS} = -7.5\text{ V}$

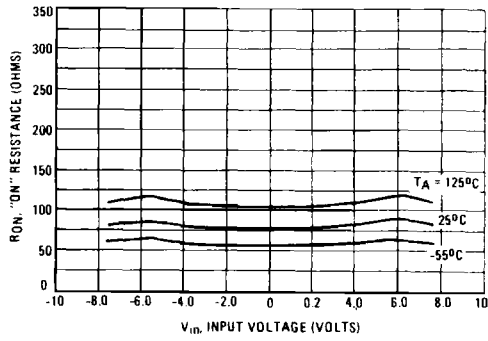


FIGURE 9 – $V_{DD} = 5.0\text{ V}$, $V_{SS} = -5.0\text{ V}$

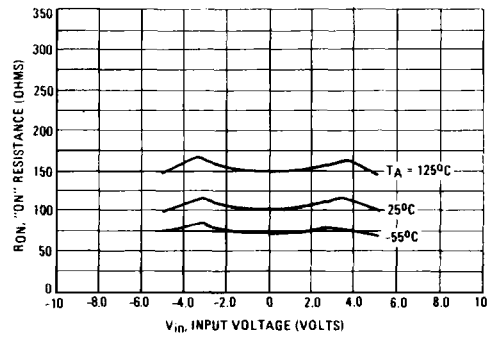


FIGURE 10 – $V_{DD} = 2.5\text{ V}$, $V_{SS} = -2.5\text{ V}$

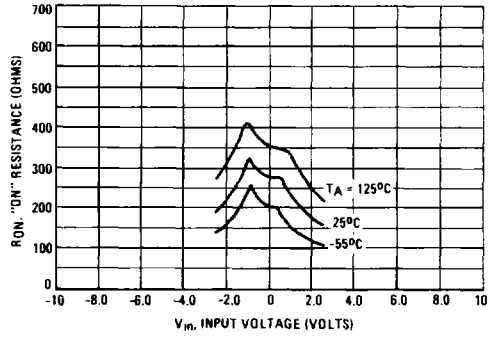
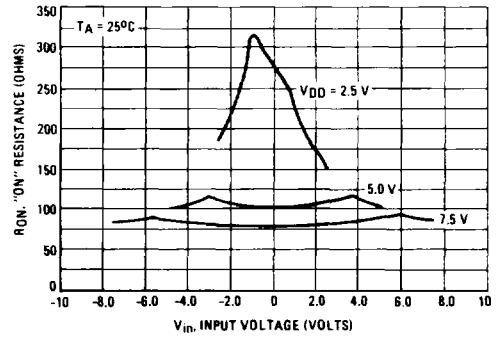


FIGURE 11 – COMPARISON AT 25°C, $V_{DD} = -V_{SS}$



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APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0-to-5 volt digital control signal is used to directly control a 5 volt peak-to-peak analog signal.

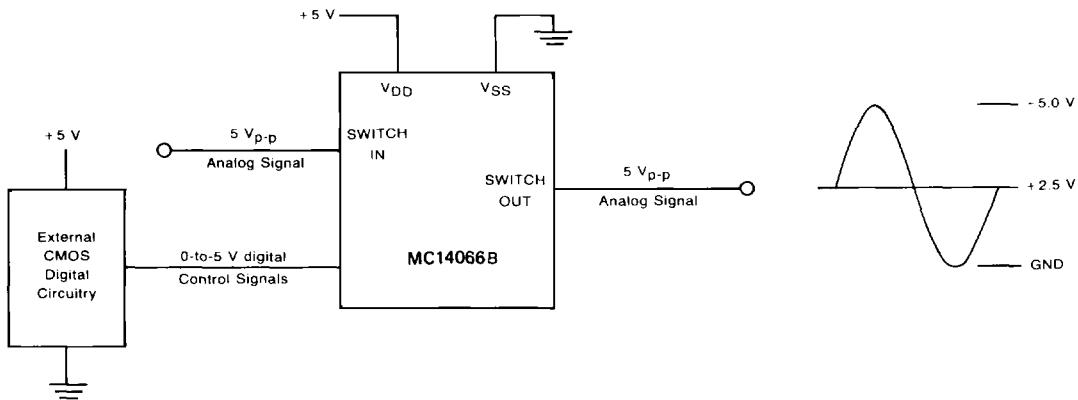
The digital control logic levels are determined by V_{DD} and V_{SS} . The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, $V_{DD} = +5\text{ V} = \text{logic high}$ at the control inputs; $V_{SS} = \text{GND} = 0\text{ V} = \text{logic low}$.

The maximum analog signal level is determined by V_{DD} and V_{SS} . The analog voltage must not swing higher than V_{DD} or lower than V_{SS} .

The example shows a 5 volt peak-to-peak signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{SS} is 18.0 volts. Most parameters are specified up to 15 volts which is the *recommended* maximum difference between V_{DD} and V_{SS} .

FIGURE A — APPLICATION EXAMPLE



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FIGURE B — EXTERNAL GERMANIUM OR SCHOTTKY CLIPPING DIODES

