User's Guide

Using the UCC14240EVM-052 for Biasing Traction Inverter Gate Driver ICs Requiring Single, Positive or Dual, Positive/Negative Bias Power

ABSTRACT

This user's guide provides a description as well as directions for use of the UCC14240EVM-052 to evaluate the UCC14240-Q1, high frequency, integrated transformer, DC-DC converter module from Texas Instruments. This EVM allows designers to quickly and efficiently evaluate the UCC14240-Q1 for use in automotive or industrial applications requiring gate driver IC bias power as high as 2-W, meeting up to 3-kV_{RMS} isolation.

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1 Introduction

The UCC14240-Q1 is a high efficiency, low-emissions, 3 kV_{RMS} Isolated DC-DC Converter capable of delivering up to 2-W of power. Since the UCC14240-Q1 provides isolated power in an integrated package, this allows systems to reduce cost and size by removing the need for separate isolated power supplies. The UCC14240-Q1 delivers class-leading efficiency in power conversion from the primary to the secondary side while removing the need for bulky external transformers or power modules commonly used in existing designs. This integration allows for minimal printed circuit board (PCB) area as well as decreased height profile.

1.1 U1 Component Selection

The UCC14240-Q1 is the default IC used in the UCC14240EVM-052 but any of the alternate versions listed in Table 1-1 can be used for evaluation. Each of the component versions listed in Table 1-1 are pin-to-pin compatible, functionally equivalent, drop in replacements with respect to one another.

Table 1-1. UCC1424x-Q1 Version Differences

General Part Number	Orderable Part Number	Isolation/Surge/Working Voltage
UCC14240-Q1	UCC14240QDWNQ1	3 kVRMS/6.5 kVPK/850 VRMS
UCC14241-Q1	UCC14241QDWNQ1	5 kVRMS/10 kVPK/1 kVRMS

If U1 replacement is required, then TI recommends to always use best practice soldering techniques. Techniques can include taking appropriate ESD precautions and having qualified personnel, skilled at surface mount soldering and board level rework, removing and installing U1. Visually verify the desired UCC1424x-Q1 component version is properly installed in the EVM. If rework on U1 has previously been performed, then visually verify correct orientation of U1 according to Figure 2-1. The pin 1 identifying dot on top of the IC package is oriented at the top left according to Figure 2-1.

1.2 Pin Configuration and Functions

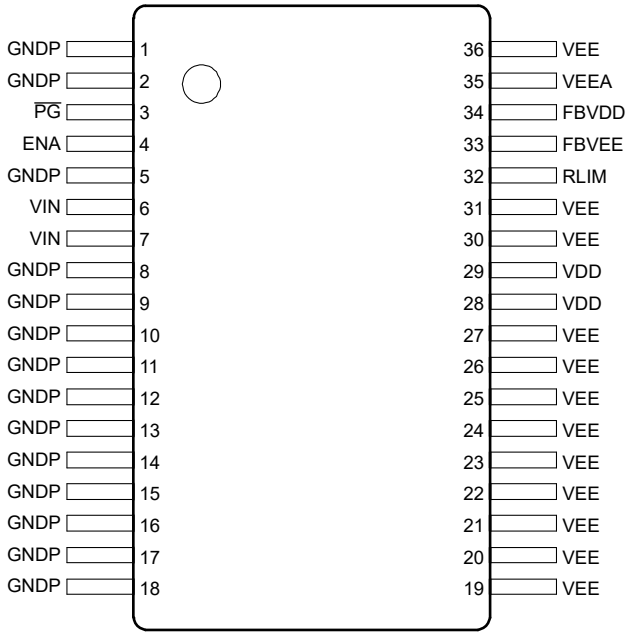


Figure 1-1. DWN Package, 36-Pin SSOP (Top View)

Table 1-2. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
GNDP	1, 2, 5, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18	G	Primary-side ground connection for VIN. PIN 1,2, and 5 are analog ground. PIN 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, and 18 are power ground. Place several vias to copper pours for thermal relief.
$\overline{PG}$	3	O	Active low power-good open-drain output pin. $\overline{PG}$ remains low when (UVLO ≤ V_{VIN} ≤ OVLO); (UVP1 ≤ (VDD – VEE) ≤ OVP1); (UVP2 ≤ (COM – VEE) ≤ OVP2); $T_{J\_Primary}$ ≤ $TSHUTP_{PRIMARY\_RISE}$; and $T_{J\_secondary}$ ≤ $TSHUT_{SECONDARY\_RISE}$
ENA	4	I	Enable pin. Forcing ENA LOW disables the device. Pull HIGH to enable normal device functionality. 5.5-V recommended maximum.
VIN	6, 7	P	Primary input voltage. PIN 6 is for analog input, and PIN 7 is for power input. For PIN 7, connect one 10-µF ceramic capacitor from power VIN PIN 7 to power GNDP PIN 8. Connect a 0.1-µF high-frequency bypass ceramic capacitor close to PIN 7 and PIN 8.
VEE	19, 20, 21, 22, 23, 24, 25,26, 27, 30,31, 36	G	Secondary-side reference connection for VDD and COM. The VEE pins are used for the high current return paths.
VDD	28, 29	P	Secondary-side isolated output voltage from transformer. Connect a 2.2-µF and a parallel 0.1-µF ceramic capacitor from VDD to VEE. The 0.1-µF ceramic capacitor is the high frequency bypass and must be next to the IC pins. A 4.7-µF or 10-µF ceramic capacitor can be used instead of 2.2-µF to further reduce the output ripple voltage.
RLIM	32	P	Secondary-side second isolated output voltage resistor to limit the source current from VDD to COM node, and the sink current from COM to VEE. Connect a resistor from RLIM to COM to regulate the (COM – VEE) voltage.
FBVEE	33	I	Feedback (COM – VEE) output voltage sense pin used to adjust the output (COM – VEE) voltage. Connect a resistor divider from COM to VEE so that the midpoint is connected to FBVEE, and the equivalent FBVEE voltage when regulating is 2.5 V. Add a 330-pF ceramic capacitor for high frequency decoupling in parallel with the low-side feedback resistor. The 330-pF ceramic capacitor for high frequency bypass must be next to the FBVEE and VEEA IC pins on top layer or back layer connected with vias.
FBVDD	34	I	Feedback (VDD – VEE) output voltage sense pin and to adjust the output (VDD – VEE) voltage. Connect a resistor divider from VDD to VEE so that the midpoint is connected to FBVDD, and the equivalent FBVDD voltage when regulating is 2.5 V. Add a 330-pF ceramic capacitor for high frequency decoupling in parallel with the low-side feedback resistor. The 330-pF ceramic capacitor for high frequency bypass must be next to the FBVDD and VEEA IC pins on top layer or back layer connected with vias.
VEEA	35	G	Secondary-side analog sense reference connection for the noise sensitive analog feedback inputs, FBVDD and FBVEE. Connect the low-side feedback resistors and high frequency decoupling filter capacitor close to the VEEA pin and respective feedback pin FBVDD or FBVEE. Connect to secondary-side gate drive lowest voltage reference, VEE. Use a single point connection and place the high frequency decoupling ceramic capacitor close to the VEEA pin.

(1) P = power, G = ground, I = input, O = output

2 Description

The UCC14240EVM-052 is intended to allow designers to evaluate the performance characteristics and capabilities of the UCC14240-Q1 quickly and easily for use in automotive, isolated, gate driver bias applications as well as a variety of isolated industrial bias power applications. The EVM allows users to test functions of the UCC14240-Q1 such as: Enable/Disable (EN) of the device as well as configure the isolated output voltage for 15 V<VDD<20 V, and -5 V<VEE<0 V and easily apply variable loads to the outputs. This EVM allows the user to measure efficiency across the input voltage range and varying output loads according to system requirements. Another feature of the EVM is the ease of probing during test. Test points, are strategically placed and described according to Table 4-1.

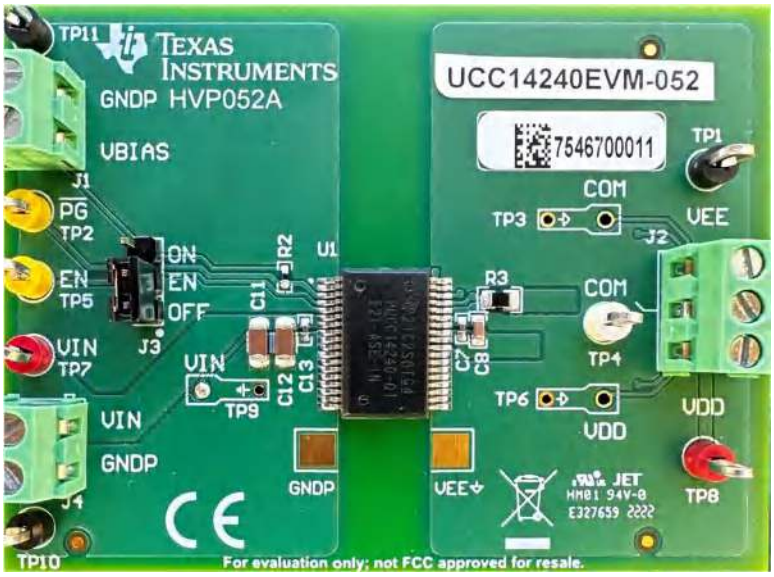


Figure 2-1. UCC14240EVM-052, HVP052A, Top View

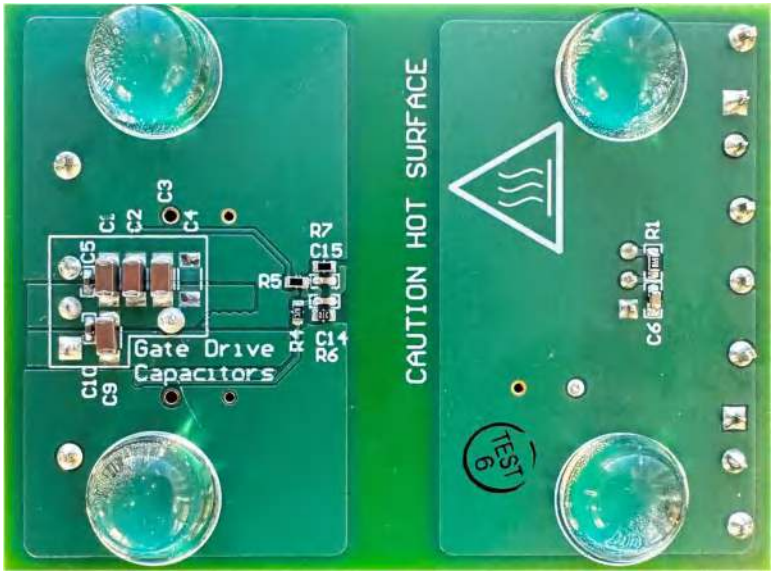


Figure 2-2. UCC14240EVM-052, HVP052A, Bottom View

2.1 EVM Electrical Performance Specifications

Table 2-1. EVM Electrical Specifications

V_{IN} = 24 V, VDD=VDD-VEE = 20 V, VEE=VEE-COM = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage range		21	24	27	V
V_{IN_ON}	Input voltage on		19		21	V
V_{IN_OFF}	Input voltage off		17.1		18.9	V
I_{IN_FL}	Input current at full load	V_{IN} = 21 V, I_{VDD} = 80 mA		130		mA
		V_{IN} = 24 V, I_{VDD} = 80 mA		120		
		V_{IN} = 27 V, I_{VDD} = 80 mA		115		
I_{IN_NL}	Input current at no load	V_{IN} = 21 V, I_{VDD} =I_{VEE} = 0 mA		14		mA
		V_{IN} = 24 V, I_{VDD} =I_{VEE} = 0 mA		13		
		V_{IN} = 27 V, I_{VDD} =I_{VEE} = 0 mA		12		
I_{IN_OFF}	Input current at EN LOW	EN LOW, VDD = VEE = 0 V		550	650	µA
EN to /PG delay		I_{VDD} =I_{VEE} = 0 mA		4	5	ms
OUTPUT CHARACTERISTICS						
VDD-VEE	DC full load set-point	21 V<V_{IN}<27 V, I_{VDD} = 80 mA	19.92	19.94	19.96	V
I_{VDD}	VDD load current range	21 V < V_{IN} < 27 V	0		80	mA
$VDD_{\%LD}$	Load regulation	$VDD_{REG} = \left[\frac{V_{I(min)} - V_{I(max)}}{V_{I(max)}}\right] \times 100\%$ V_{IN}=24 V, 0 mA ≤ I_{VDD} ≤ 80 mA		0.336		%
$VDD_{\%LN}$	Line regulation	$VDD_{REG} = \left[\frac{V_{I(min)} - V_{I(max)}}{V_{I(max)}}\right] \times 100\%$ I_{VDD}=80 mA, 21 V ≤ V_{IN} ≤ 27 V		0.061		%
VDD_{AC}	pk-to-pk AC ripple	I_{VDD} = 80 mA		300	350	mV
VDD_{SS}	Soft-start	I_{VDD} = I_{VEE} = 0 mA		1.8		ms
P_{MAX}	Maximum output power	I_{VDD} = 100 mA, I_{VEE} = 10 mA		1.5	2	W
VEE-COM	DC full load set-point	21 V ≤ V_{IN} ≤ 27 V, I_{VEE} = 10 mA	-5.004		-5.007	V
I_{VEE}	VEE load current range	21 V≤ V_{IN} ≤ 27 V	0		12	mA
VEE_{AC}	pk-to-pk AC ripple	I_{VEE} = 10 mA		110	130	mV
SYSTEM CHARACTERISTICS						
$\eta_{100\%}$	Full load efficiency	I_{VDD} = 80 mA		56		%
$\eta_{50\%}$	Half load efficiency	I_{VDD} = 40 mA		53		%
F_{SW}	Switching frequency (1)	V_{IN} = 21 V, 0 mA < I_{VDD} < 80 mA		16		MHz
		V_{IN} = 24 V, 0 mA < I_{VDD} < 80 mA		13		
		V_{IN} = 27 V, 0 mA < I_{VDD} < 80 mA		27		
$VDD_{(OCL)}$	VDD overcurrent limit	I_{VDD} > 80 mA		130	145	mA
$VEE_{(OCL)}$	VEE overcurrent limit	I_{VEE} > 10 mA		13	15	mA
T_{MAX}	Maximum temperature rise above ambient	I_{VDD} = 80 mA, I_{VEE} = 10 mA		36	40	°C

(1) Switching frequency is specified as primary-side switching frequency. Secondary-side is 2x primary

3 Schematic

Figure 3-1 shows the EVM electrical schematic. C4 is intentionally unpopulated as indicated by a red X on the secondary side, placed directly over the component.

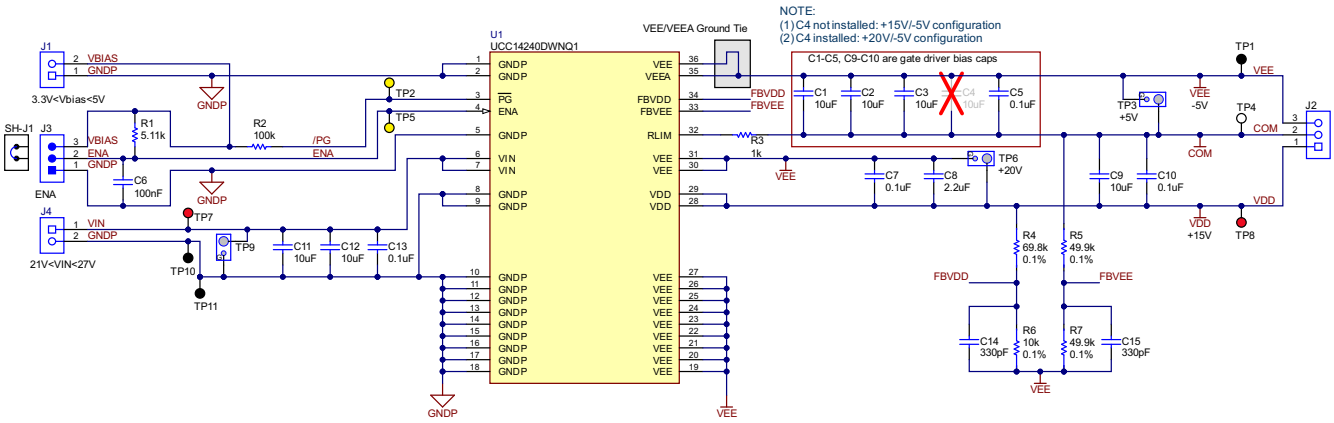


Figure 3-1. UCC14240EVM-052 Schematic Diagram

4 EVM Setup and Operation

4.1 Recommended Test Equipment

- V_{BIAS}: DC power supply1: 5 V, 10 mA
- V_{IN}: DC power supply: 30 V, 300 mA
- I_{VDD}: Electronic load or fixed resistor: 25 V, 200 mA
- I_{VEE}: Electronic load or fixed resistor: 5 V, 10 mA
- (3) DVMs measuring DC voltage < 30 V (V3 in must be a battery powered DVM)
- (3) DVMs measuring DC current < 200 mA on I_{VDD}, I_{VEE}, <300 mA on I_{VIN}
- Oscilloscope: 4 channel, 500 MHz or better, voltage probes, current probes
- Minimum wire gauge 20 AWG to 22 AWG or better
- Thermal camera (optional) or thermocouple to measure U1 case temperature

4.2 External Connections for Easy Evaluation

The UCC14240EVM-052 EVM uses screw terminals for quickly connecting to the V_{IN}, VDD ,and VEE pins. Connecting the appropriate ammeters and voltmeters, as shown in Figure 4-1, allows accurate EVM efficiency measurements to be made.

Connecting Test Equipment

1. Move jumper SH-J1 into the J3:1-2, EN OFF position. This makes sure the EVM cannot start while test equipment is being connected.
2. Connect a +5 V DC bias power supply to J1:1-2 (+3.3 V to +5 V). Set the power supply to 0 V. The +5 V supply at J1 serves as the pullup bias for /PG and ENA. Turn off/disable the +5V DC Bias power supply.
3. Connect the V_{IN} DC power supply capable of 21 V<V_{IN}<27 V, 200 mA at J4:1-2 (V_{IN}). Adjust the power supply to 24 V, and set the current limit to 300 mA. Set the power supply voltage to 24 V. Turn off/disable the V_{IN} power supply.
4. Connect a variable load between J2:1 (VDD) and J2:3 (VEE). If using an electronic load, set to constant current (CC), 80 mA. Leave the load disabled until the EVM is powered.
5. Connect a second load between J2:2 (COM) and J2:3 (VEE). If using an electronic load, set to constant current (CC), 10 mA. Leave the load disabled until the EVM is powered. Since the required load is small, a through-hole, 250-mW, 511-Ω load resistor can be connected between J2:2-3.
6. Some electronic loads are not be able to regulate/stabilize CC when setting in the low mA range. Monitor the input current and load currents by inserting ammeters, A2 and A3, as shown in Figure 4-1. Use a current probe with the oscilloscope to verify the stability of the DC current being regulated by an electronic load.

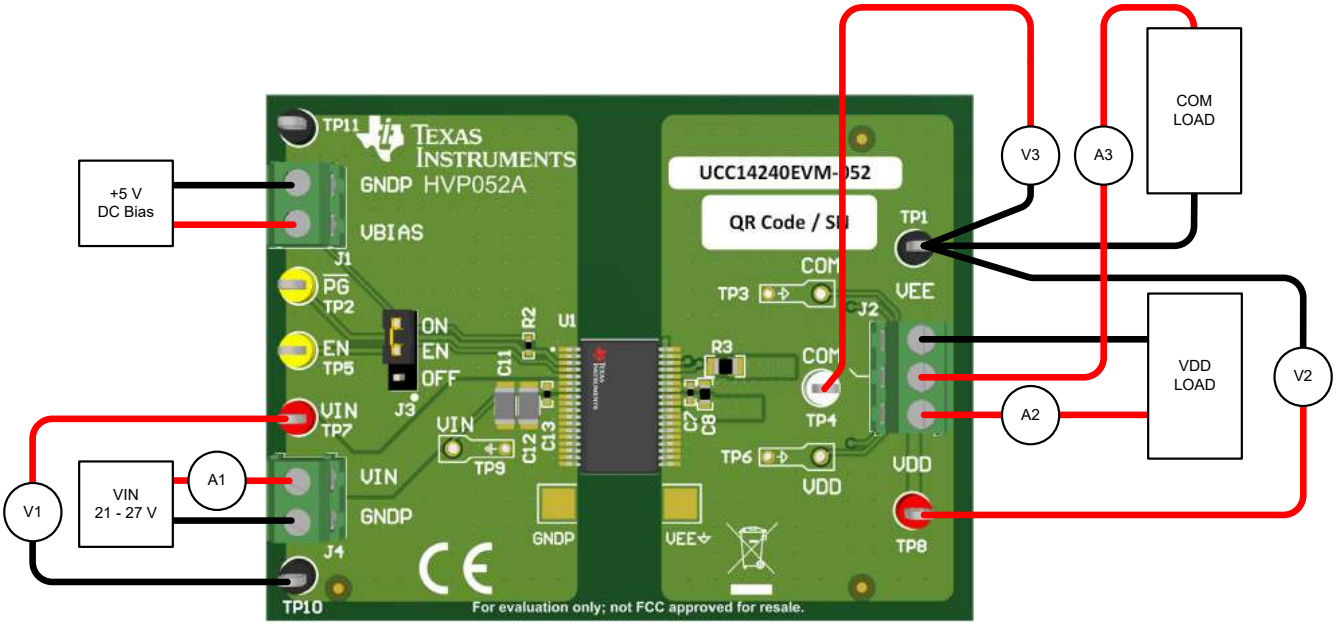


Figure 4-1. Typical Efficiency Measurement Setup

4.3 Powering the EVM

WARNING

- Hot Surface. Contact can cause burns. U1 package surface can reach temperatures of 45°C above ambient. Do not touch!
- Do not test this EVM unless you are trained in the proper safety, handling and testing of power electronics.

4.3.1 Power on for Start-up

1. Verify VIN and +5-V DC bias power supplies are OFF/disabled and no voltage is applied to the UUT
2. Move EN shorting jumper, SH-J1, to the J3:2-3 EN ON position
3. Turn on the V_{IN} DC power supply. Verify 24-V is present at TP7-to-TP10
4. Verify the loads on VDD and VEE are disabled
5. Turn on the +5-V DC bias power supply. EVM is now enabled with VDD and VEE in regulation under no load conditions.
6. Verify 20-V is present on VDD-VEE and 5-V is present on COM-VEE
7. Enable the 80-mA load on VDD-VEE, enable the 10-mA load on COM-VEE
8. The UCC14240-Q1 is now regulating VDD and VEE and processing 1.6-W of isolated output power
9. Vary VIN between 21 V<V_{IN}<27 V, vary I_{VDD} between 0 mA<I_{VDD}<80 mA, vary I_{VEE} between 0 mA<I_{VEE}<10 mA.
10. Insert oscilloscope probes into TP9, TP6 and TP3 for measuring V_{IN}, VDD and VEE start-up, steady state and AC ripple voltage

4.3.2 Power off for Shutdown

1. Move EN shorting jumper SH-1 to the J3:1-2, EN OFF position
2. Turn off the +5 V, DC bias power supply
3. Disable the I_{VDD} load
4. Disable the I_{VEE} load
5. Turn off V_{IN} power supply

4.4 EVM Test Points

Table 4-1 describes the various EVM test points, allowing easy access for connecting oscilloscope probes, DVM test leads and wire connections to lab test equipment as outlined in section 4.1. Pay attention to maintain separation between the primary side, GNDP and secondary side, VEE. Primary-side test points are not to be referenced to VEE through improper test equipment insertion. Likewise, secondary-side test points are not to be referenced to GNDP through improper test equipment insertion.

Table 4-1. Input, Output, Test Point (I/O/TP) Description

PIN	I/O/TP	COLOR	DESCRIPTION	MIN	TYP	MAX	UNIT
J1	I	Green	VBIAS, EN and /PG bias	3	V_{BIAS}	5	V
J2:1-3	O	Green	Secondary VDD-to-VEE	15		27	V
J2:2-3	O	Green	Secondary COM-to-VEE	0		5	V
J3:1-2	I	Black	EN, off		0		V
J3:2-3	I	Black	EN, on		V_{BIAS}		V
J4	I	Green	V_{IN}, primary input voltage	21	24	27	
TP1	TP	Black	VEE, secondary side reference		0		V
TP2	TP	Yellow	/PG, power good test point		V_{BIAS}		V
TP3	TP	PCB	COM-to-VEE, secondary COM scope probe point	0		5	V
TP4	TP	White	COM-to-VEE, secondary COM output midpoint	0		5	V
TP5	TP	Yellow	EN, enable test point		V_{BIAS}		V
TP6	TP	PCB	VDD-to-VEE, secondary VDD scope probe point	15		28	V
TP7	TP	Red	V_{IN}, positive probe point	21	24	27	V
TP8	TP	Red	VDD, secondary VDD test point	15		28	V
TP9	TP	PCB	V_{IN}-to-GNDP scope probe point	21	24	27	V
TP10	TP	Black	GNDP, shared primary GND test point		0		V
TP11	TP	Black	GNDP, shared primary GND test point		0		V

4.5 Probing the EVM

Using TP4, TP6 and TP10 oscilloscope probe PCB test points: The UCC12240-Q1 is a high frequency DC-DC module that requires careful measurement for accurately capturing transient events and measuring high frequency, AC ripple voltage. Remove the “witch hat” probe tip cover and ground lead from the scope probe. If scope probe ground springs are not available, wrap a piece of 22 AWG bare wire around the scope probe ground ring and insert the probe tip and ground into the EVM as shown in Figure 4-2.

Figure 4-2. UCC14240EVM-052, PCB Scope Probe Test Points

The EVM output nomenclature (VDD, VEE, COM) corresponds to what is commonly used when referring to isolated gate driver ICs. As shown in Figure 3-1, TP4 (COM) is the midpoint of a capacitive divider and is intended to connect to the COM pin of the isolated gate driver IC. When the UCC14240-Q1 is used to bias a gate driver IC, VDD (VDD-COM) and VEE (VEE-COM) are referred to with respect to COM. In this case consider COM as a virtual GND to the gate driver IC. Because the midpoint of the capacitive divider is sensitive to charge imbalance, do not connect any ground-referenced, test equipment to TP4 (COM) when probing the EVM. A battery powered DVM can be used to measure VEE with respect to COM. COM is therefore not be considered as GND but is really a sort of “virtual GND” to the gate driver IC. Since the midpoint of the capacitive divider is sensitive to charge imbalance, for the purpose of probing the EVM, do not to connect any ground-referenced, test equipment to TP4 (COM). A battery powered DVM can be used to measure VEE with respect to COM. When testing the EVM as a stand-alone bias power supply, oscilloscope probing of the secondary-side outputs is limited to TP3 and TP6 which are referenced to VEE. This means VDD displays an oscilloscope measurement of VDD+|VEE| and VEE displays |VEE|. Connecting any ground-referenced test equipment to COM can result in a “false” but safe overcurrent condition causing VDD and VEE to inadvertently drop out of regulation during light load operation.

5 Performance Data

5.1 Efficiency Data

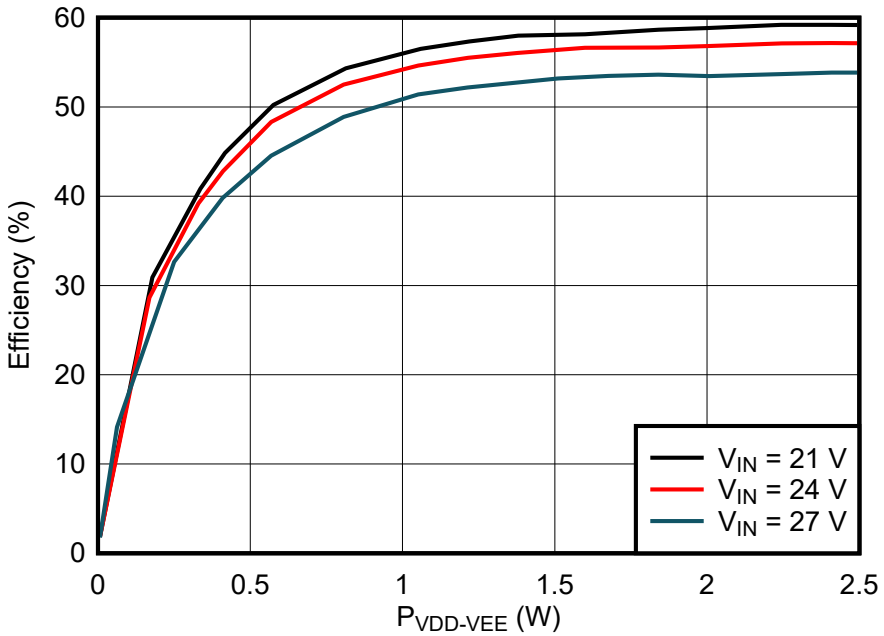


Figure 5-1. Measured Efficiency, VDD-VEE Loading Only

Table 5-1. Efficiency Test Data (VIN = 21 V)

VIN (V)	IIN (mA)	VDD-VEE (V)	$I_{VDD-VEE}$ (mA)	VDD-VEE (V)	VEE-COM (V)	PIN (W)	$P_{VDD-VEE}$ (W)	Eff (%)
21.01	14.24	20.00	0.24	14.99	-5.01	0.30	0.00	1.61
21.02	27.53	20.00	8.94	14.98	-5.02	0.58	0.18	30.90
21.01	39.19	20.00	16.82	14.98	-5.02	0.82	0.34	40.83
21.01	44.30	19.99	20.87	14.98	-5.02	0.93	0.42	44.83
21.01	54.58	19.99	28.82	14.98	-5.01	1.15	0.58	50.23
21.01	71.32	19.97	40.75	14.97	-5.01	1.50	0.81	54.32
21.01	89.26	19.96	53.07	14.96	-5.01	1.88	1.06	56.50
21.01	101.25	19.96	61.11	14.95	-5.01	2.13	1.22	57.33
21.01	113.31	19.95	69.19	14.95	-5.01	2.38	1.38	57.98
21.01	130.94	19.94	80.21	14.94	-5.01	2.75	1.60	58.13
21.01	149.49	19.93	92.43	14.92	-5.00	3.14	1.84	58.65
21.01	161.91	19.92	100.46	14.92	-5.00	3.40	2.00	58.83
21.01	180.41	19.91	112.68	14.91	-5.00	3.79	2.24	59.19
21.01	193.37	19.90	120.85	14.90	-5.00	4.06	2.40	59.20
21.01	206.61	19.89	129.05	14.89	-5.00	4.34	2.57	59.14
21.01	224.86	19.56	142.54	14.58	-5.00	4.72	2.79	59.01
21.01	226.61	18.97	146.61	13.97	-5.00	4.76	2.78	58.41

Table 5-2. Efficiency Test Data (VIN = 24 V)

VIN (V)	IIN (mA)	VDD-VEE (V)	$I_{VDD-VEE}$ (mA)	VDD-VEE (V)	VEE-COM (V)	PIN (W)	$P_{VDD-VEE}$ (W)	Eff (%)
24.02	12.68	20.01	0.24	15.00	-5.01	0.30	0.00	1.58
24.02	24.59	20.01	8.46	14.99	-5.02	0.59	0.17	28.65
24.01	35.03	20.00	16.48	14.99	-5.02	0.84	0.33	39.19
24.10	39.79	20.00	20.53	14.98	-5.02	0.96	0.41	42.80
24.01	49.07	19.99	28.47	14.98	-5.01	1.18	0.57	48.31
24.01	63.99	19.98	40.38	14.97	-5.01	1.54	0.81	52.51
24.01	80.19	19.97	52.68	14.97	-5.01	1.93	1.05	54.64
24.01	91.16	19.96	60.86	14.96	-5.01	2.19	1.21	55.51
24.01	102.36	19.96	69.02	14.96	-5.01	2.46	1.38	56.04
24.01	117.56	19.95	80.14	14.94	-5.01	2.82	1.60	56.63
24.01	135.40	19.93	92.39	14.93	-5.01	3.25	1.84	56.65
24.01	146.78	19.93	100.47	14.92	-5.00	3.52	2.00	56.81
24.01	163.68	19.92	112.72	14.91	-5.00	3.93	2.24	57.12
24.01	175.42	19.91	120.91	14.91	-5.00	4.21	2.41	57.15
24.01	187.31	19.90	129.05	14.90	-5.00	4.50	2.57	57.10
24.01	209.10	19.82	143.10	14.81	-5.02	5.02	2.84	56.49
24.01	216.32	19.51	150.83	14.50	-5.00	5.19	2.94	56.65
24.01	221.88	18.53	158.98	13.54	-5.01	5.33	2.95	55.28

Table 5-3. Efficiency Test Data (VIN = 27 V)

VIN (V)	IIN (mA)	VDD-VEE (V)	$I_{VDD-VEE}$ (mA)	VDD-VEE (V)	VEE-COM (V)	PIN (W)	$P_{VDD-VEE}$ (W)	Eff (%)
27.01	12.54	20.01	0.24	15.00	-5.01	0.34	0.00	1.42
27.02	16.39	20.02	3.13	15.00	-5.02	0.44	0.06	14.13
27.01	28.36	20.01	12.50	14.99	-5.02	0.77	0.25	32.64
27.01	38.11	20.01	20.49	14.99	-5.02	1.03	0.41	39.81
27.01	47.30	20.00	28.45	14.98	-5.01	1.28	0.57	44.52
27.01	61.11	19.99	40.36	14.98	-5.01	1.65	0.81	48.87
27.01	75.74	19.98	52.63	14.97	-5.01	2.05	1.05	51.40
27.01	86.09	19.97	60.75	14.97	-5.01	2.33	1.21	52.18
27.01	105.15	19.96	75.68	14.95	-5.01	2.84	1.51	53.18
27.01	116.02	19.95	83.99	14.95	-5.01	3.13	1.68	53.47
26.92	127.48	19.94	92.25	14.94	-5.01	3.43	1.84	53.61
26.92	139.46	19.93	100.68	14.93	-5.01	3.75	2.01	53.45
26.92	155.43	19.92	112.73	14.92	-5.01	4.18	2.25	53.67
26.92	166.25	19.92	120.96	14.92	-5.00	4.48	2.41	53.83
26.92	177.31	19.91	129.11	14.91	-5.00	4.77	2.57	53.85
26.92	195.73	19.90	142.57	14.90	-5.00	5.27	2.84	53.84
26.92	207.78	19.89	150.93	14.89	-5.01	5.59	3.00	53.67
26.92	226.81	19.75	163.05	14.74	-5.02	6.11	3.22	52.74
26.92	231.52	19.14	171.17	14.17	-5.01	6.23	3.28	52.57

5.2 Regulation Data

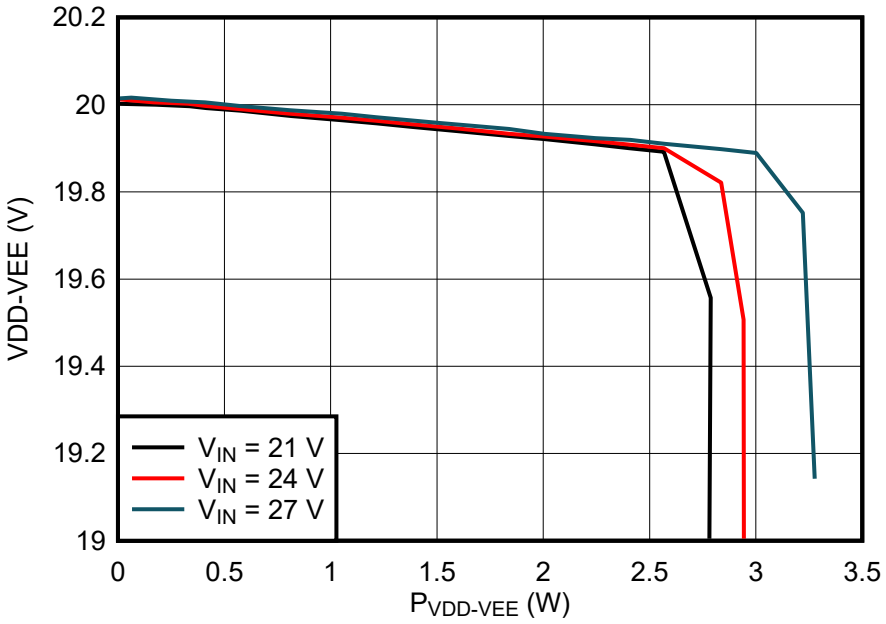


Figure 5-2. Regulation vs Power, VDD-VEE Loading Only

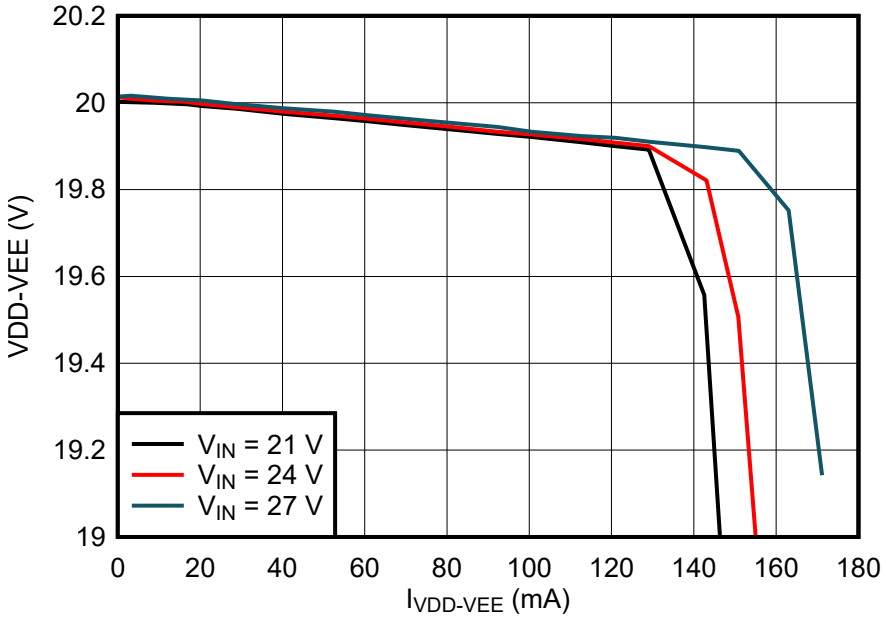


Figure 5-3. Regulation vs Current, VDD-VEE Loading Only

5.3 Steady State Input Current

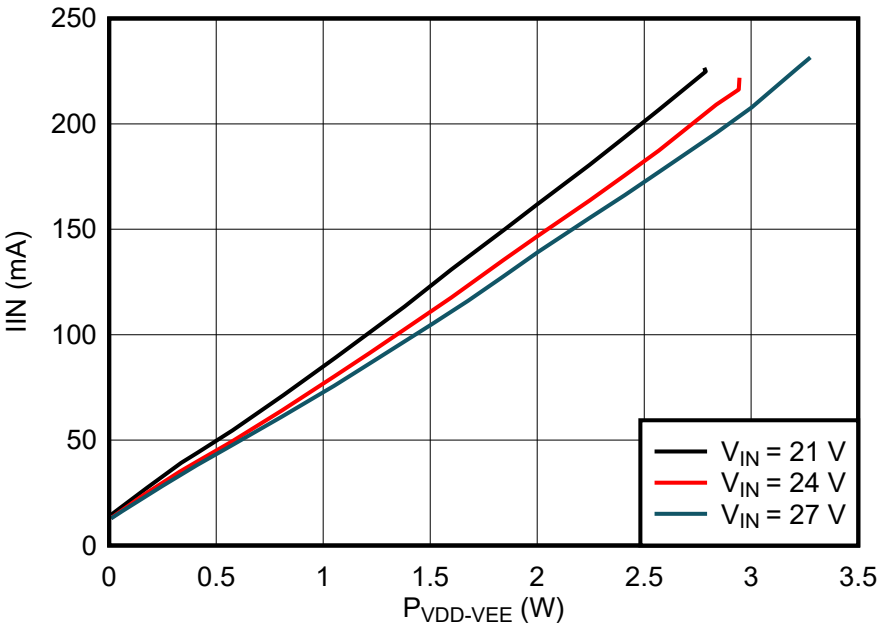
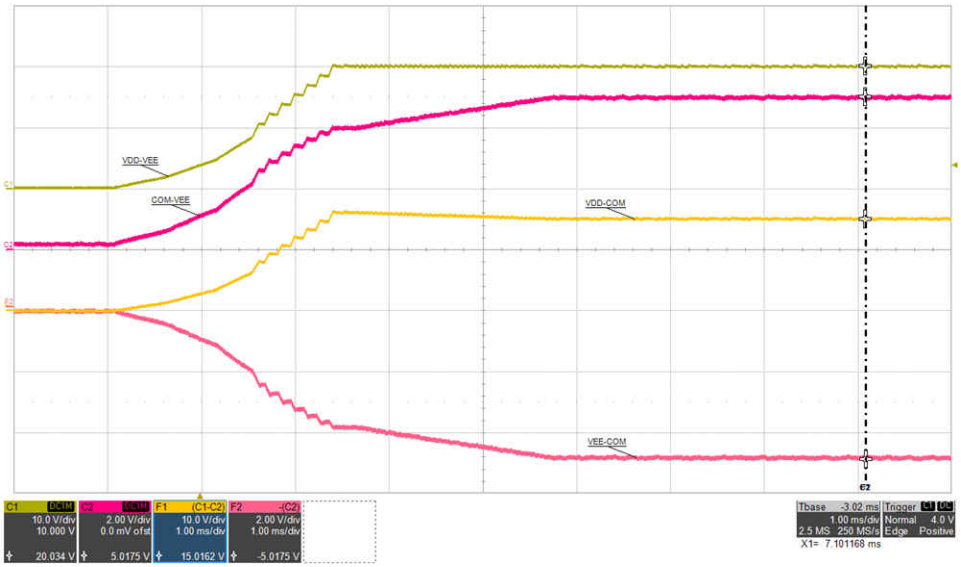


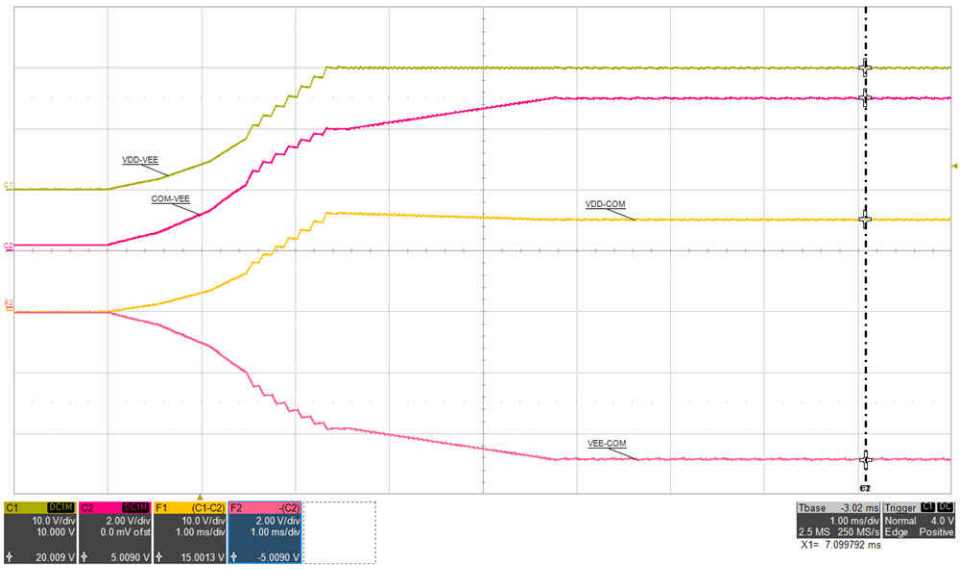
Figure 5-4. Input Current vs Power, VDD-VEE Loading Only

5.4 Start-up Waveforms



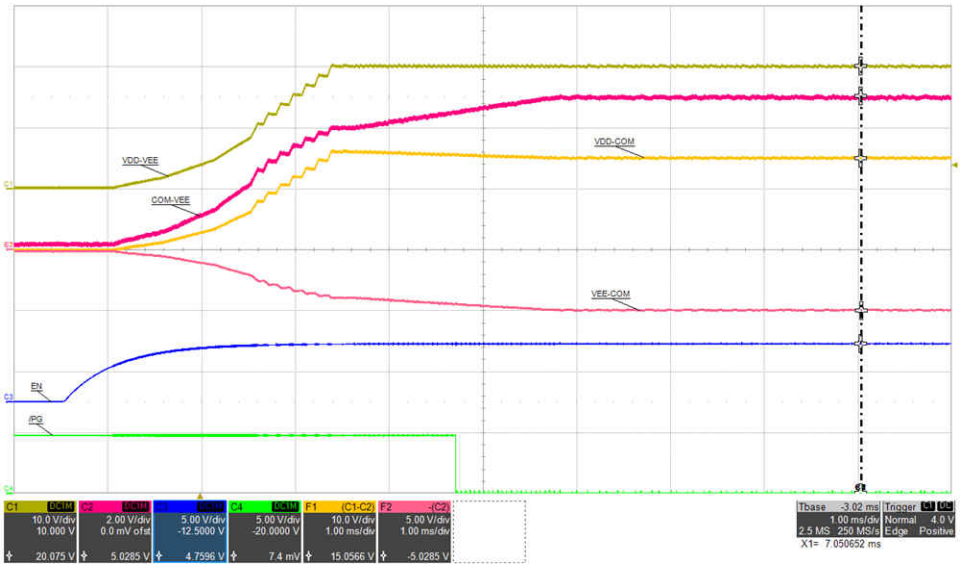
(top: VDD-VEE, 10 V/div,	bot: VEE-COM, 5 V/div),
mid-1: COM-VEE, 2 V/div,	time = 1 ms/div
mid-2: VDD-COM, 10 V/div,	

Figure 5-5. Start-up 1: VIN=24 V, $I_{VDD-VEE}$ = 0 mA



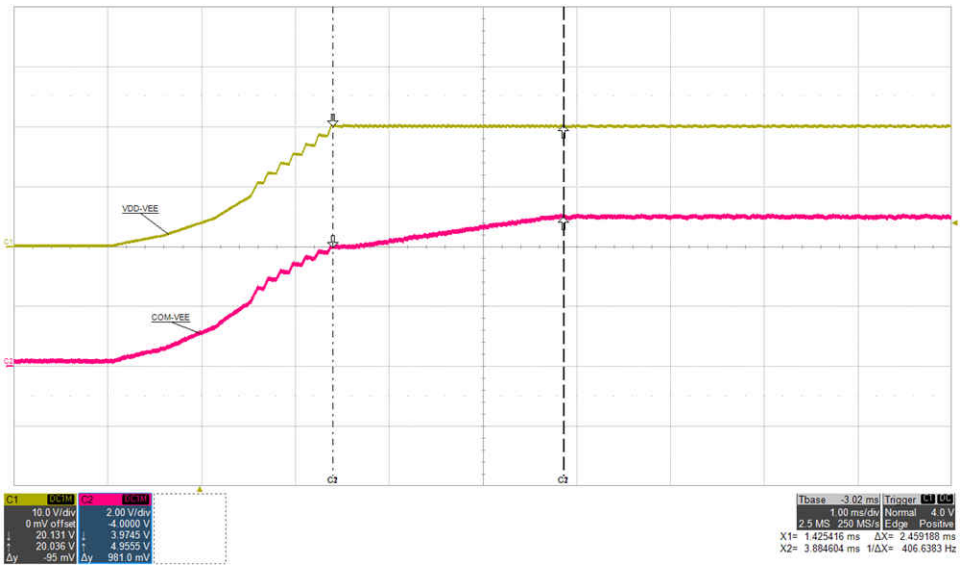
(top: VDD-VEE, 10 V/div,	bot: VEE-COM, 5 V/div),
mid-1: COM-VEE, 5 V/div,	time = 1 ms/div
mid-2: VDD-COM, 10 V/div,	

Figure 5-6. Start-up 2: VIN=24 V, $I_{VDD-VEE}$ = 80 mA



top: VDD-VEE, 10 V/div,	mid-1: COM-VEE, 2 V/div,	mid-2: VDD-COM, 10 V/div,
mid-3: VEE-COM, 5 V/div,	mid-4: EN, 5 V/div,	bot: /PG, 5 V/div),
time = 1 ms/div		

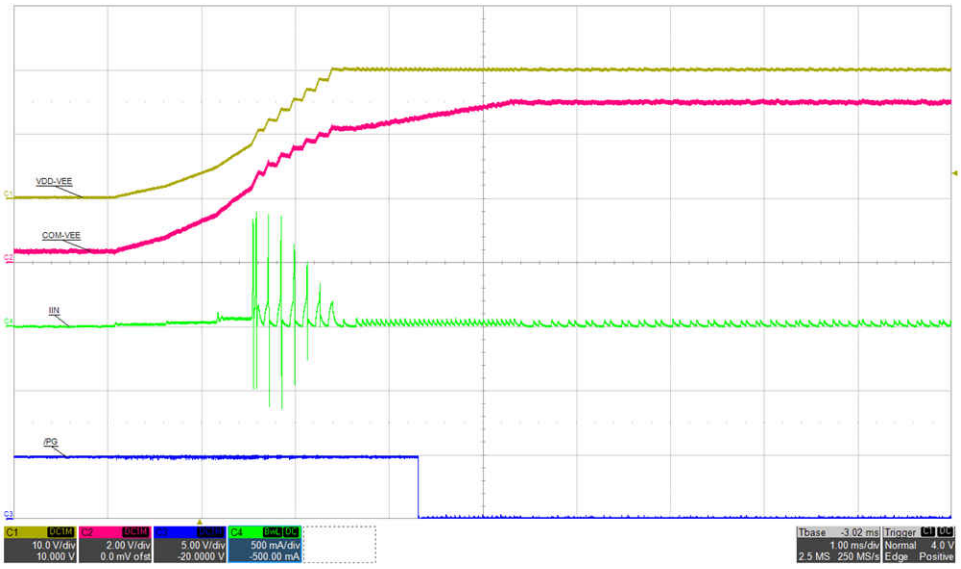
Figure 5-7. Start-up 3: VIN=24 V, $I_{VDD-VEE}$ = 80 mA



top: VDD-VEE, 10 V/div,	bot: COM-VEE, 2 V/div),	time = 1 ms/div

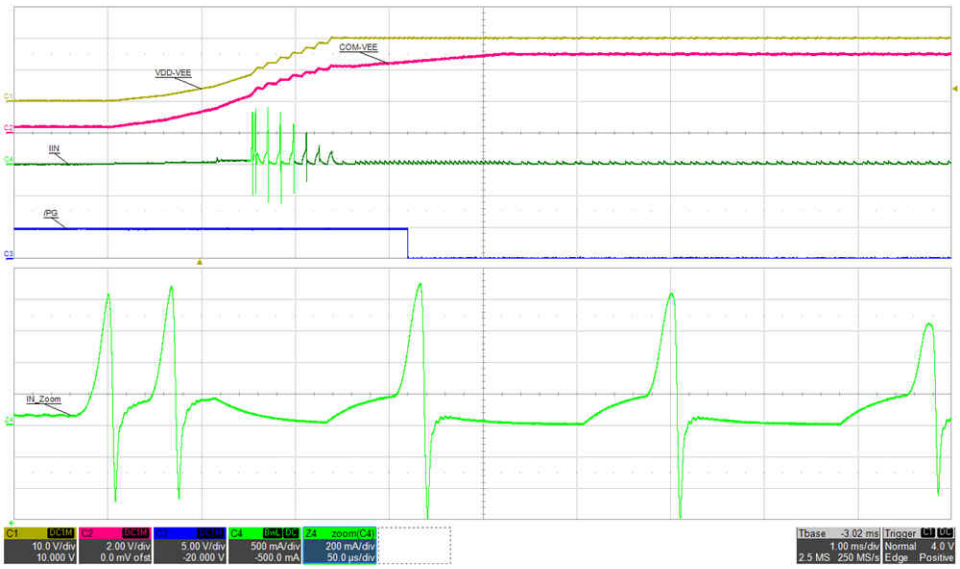
Figure 5-8. Start-up 4: VIN=24 V, IISO = 80 mA

5.5 Inrush Current



top: VDD-VEE, 10 V/div,	bot: /PG, 5 V/div),
mid-1: COM-VEE, 5 V/div,	time = 1 ms/div
mid-2: IIN, 0.5 A/div,	

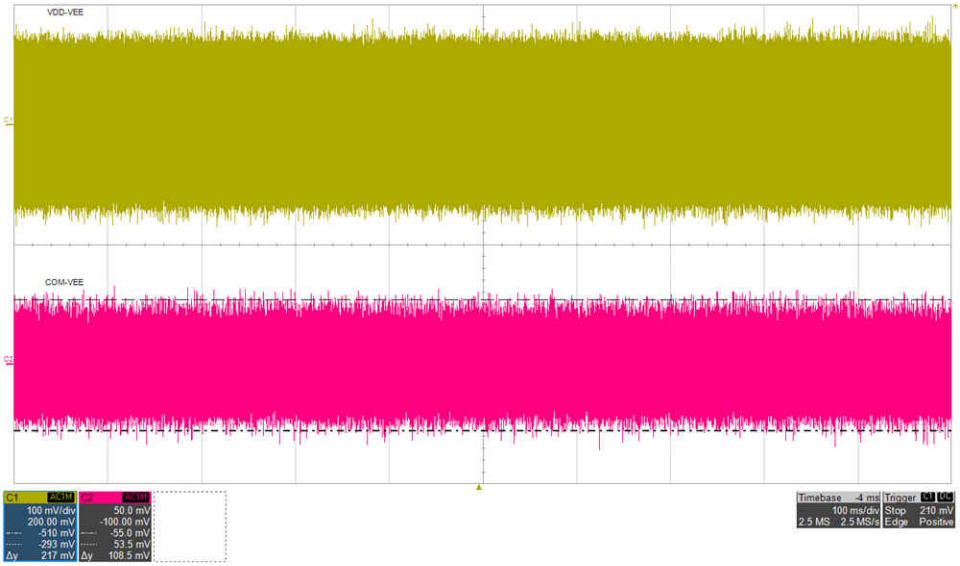
Figure 5-9. Inrush Current: VIN=24 V, $I_{VDD-VEE}$ = 80 mA



top: VDD-VEE, 10 V/div,	bot: /PG, 5 V/div,
mid-1: COM-VEE, 5 V/div,	time = 1 ms/div,
mid-2: IIN, 0.5 A/div,	time_zoom=50 µs/div

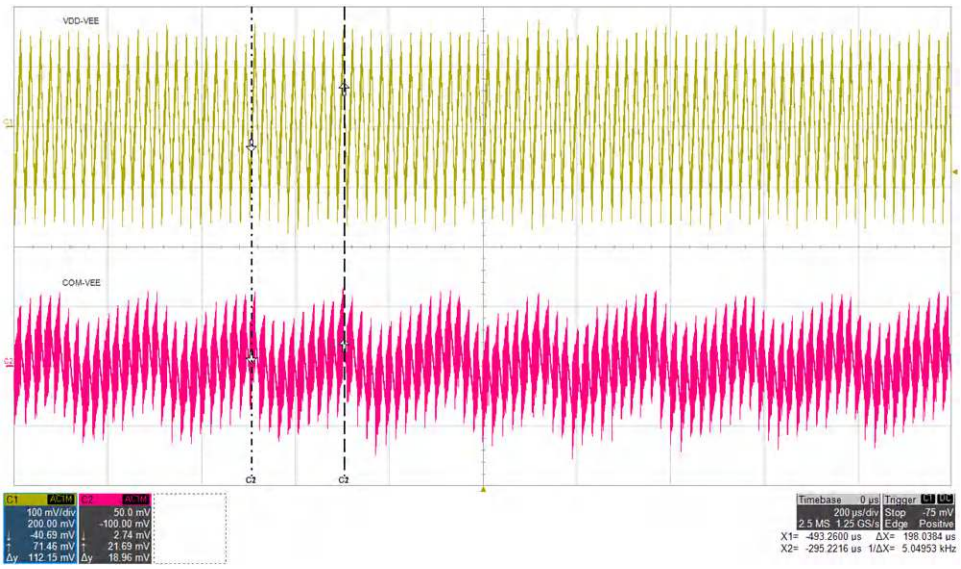
Figure 5-10. Inrush Current: VIN=24 V, $I_{VDD-VEE}$ = 80 mA

5.6 AC Ripple Voltage



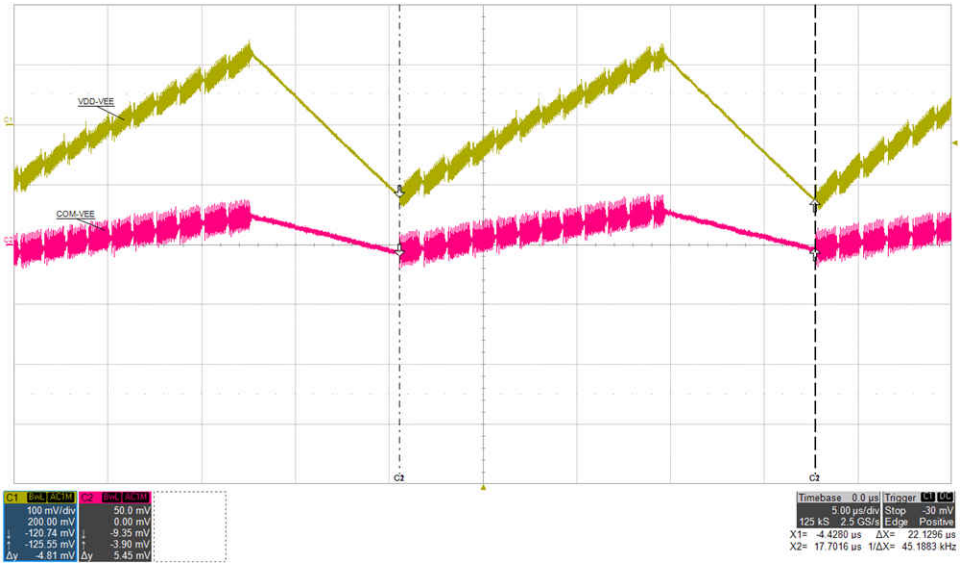
top: VDD-VEE, 100 mV/div,	bot: COM-VEE, 50 mV/div,	time = 100 ms/div

Figure 5-11. VDD_{AC}=300 mV, VEE_{AC}=108 mV, I_{VDD}=80 mA, I_{VEE}=10 mA



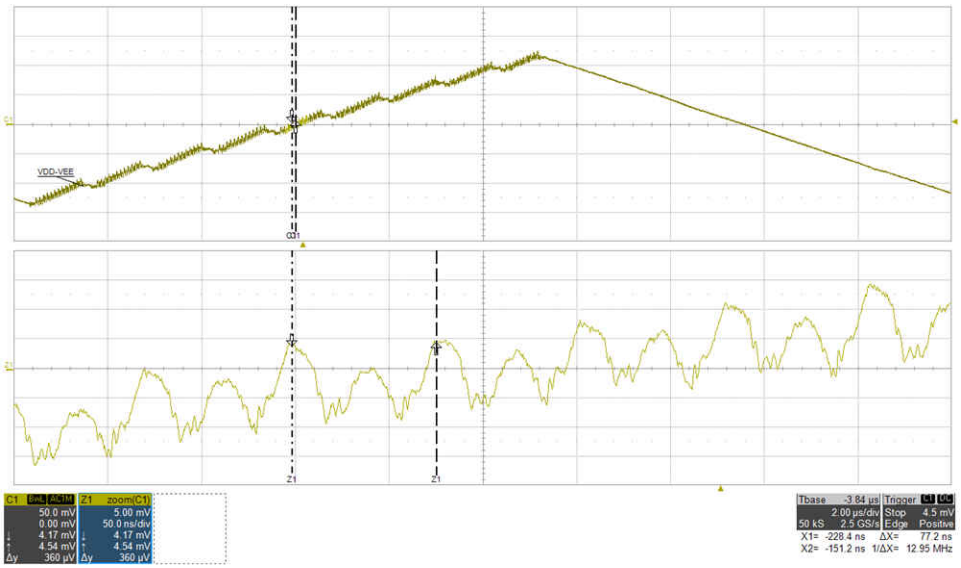
top: VDD-VEE, 100 mV/div,	bot: COM-VEE, 50 mV/div,	time = 200 µs/div

Figure 5-12. AC Ripple: VIN=24 V, IVDD=80 mA, IVEE=10 mA, FSSM = 5 kHz



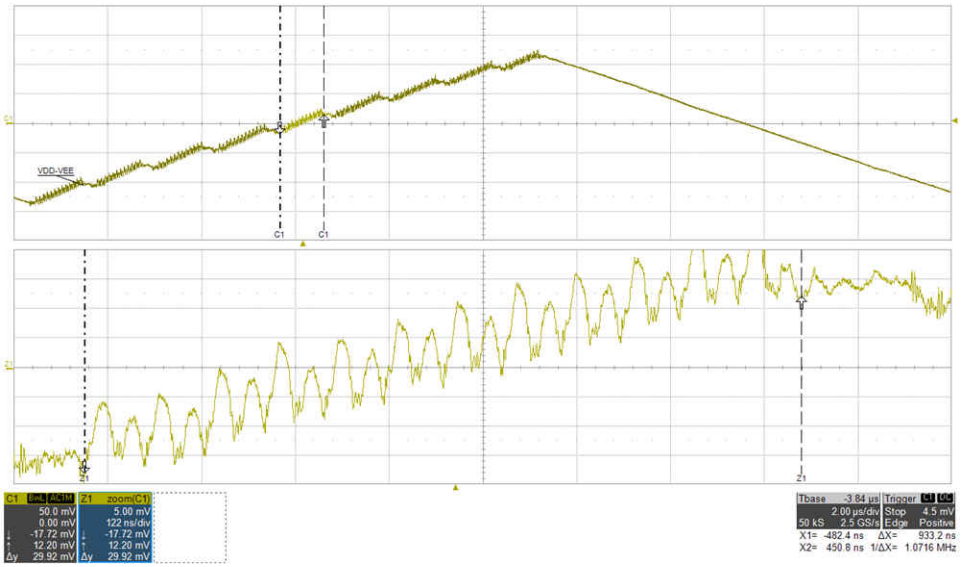
top: VDD-VEE, 100 mV/div,	bot: COM-VEE, 50 mV/div,	time = 5 µs/div

Figure 5-13. AC Ripple: VIN=24 V, IVDD=80 mA, IVEE=10 mA, FMOD=45 kHz



(VDD-VEE, 50 mV/div,	time = 5 µs/div,
Zoom: VDD-VEE, 5 mV/div,	time_zoom=50 ns/div

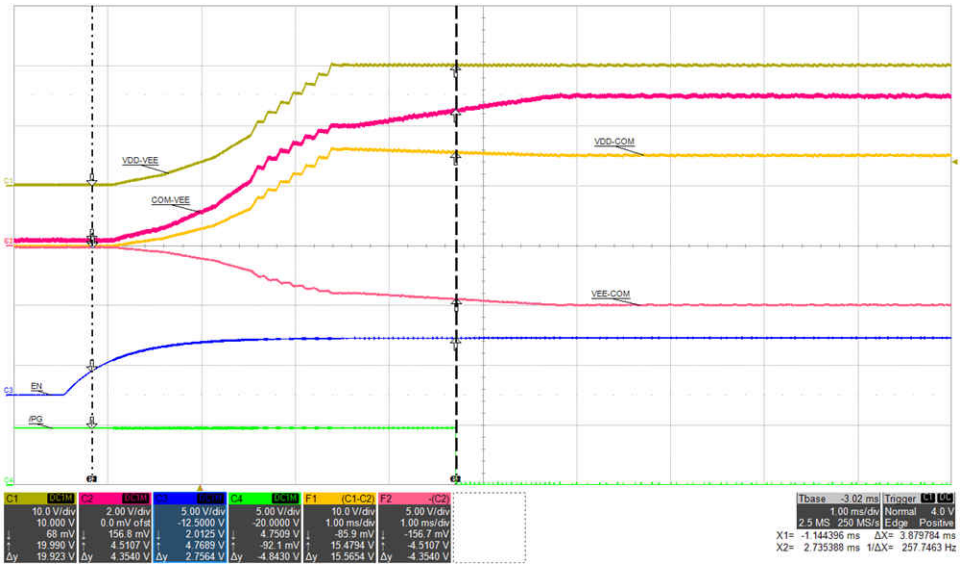
Figure 5-14. AC Ripple: VIN=24 V, IVDD=80 mA, FSW(PRI)=12.95 kHz,



(VDD-VEE, 50 mV/div,	time = 5 µs/div,
Zoom: VDD-VEE, 5 mV/div,	time_zoom=122 ns/div

Figure 5-15. AC Ripple: VIN=24 V, IVDD=80 mA, FBURST=1 MHz,

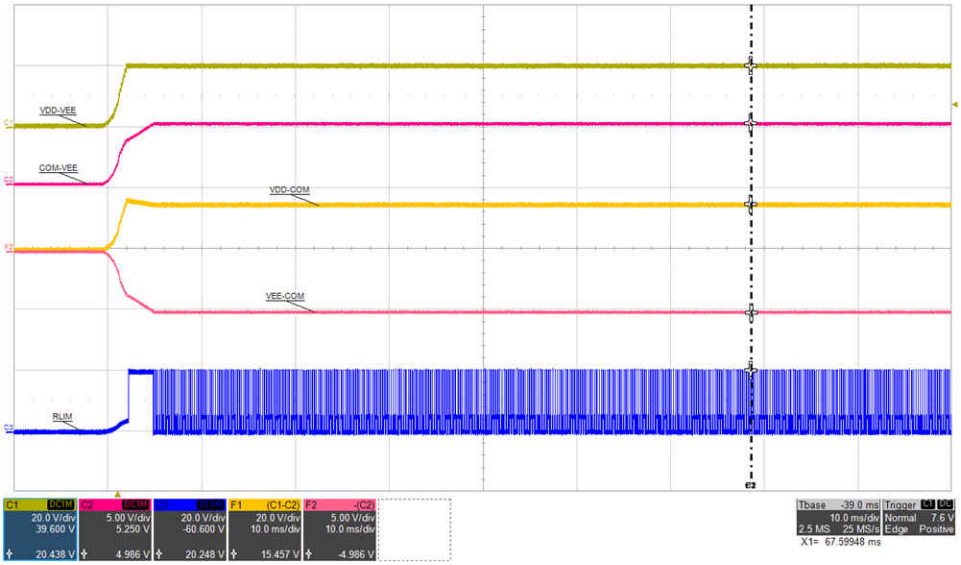
5.7 EN-to-/PG Timing



(top: VDD-VEE, 10 V/div,	mid1: COM-VEE, 2 V/div,	mid2: VDD-COM, 10 V/div,
mid3: VEE-COM, 5 V/div,	mid4: EN, 5 V/div,	bot: /PG, 5 V/div),
time = 1 ms/div		

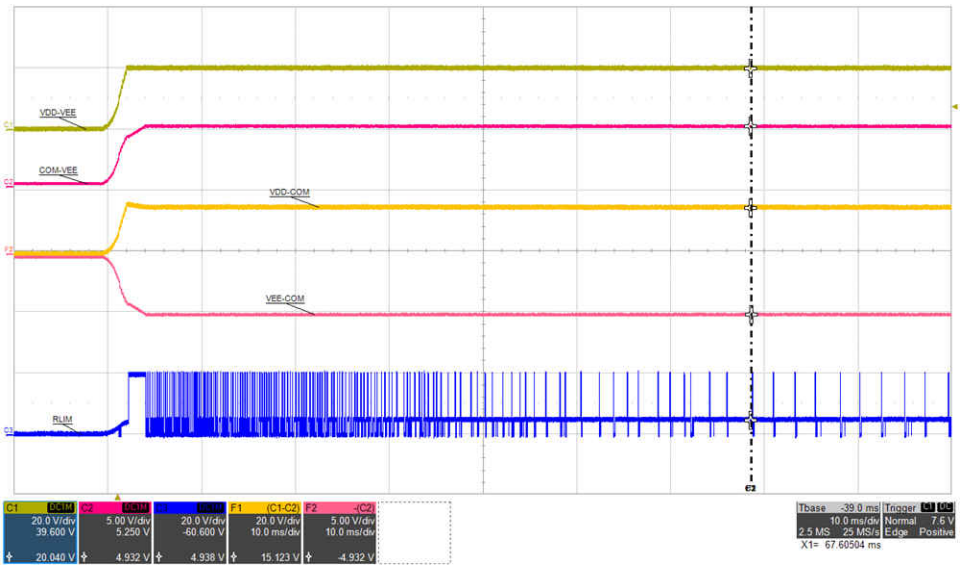
Figure 5-16. ENA to /PG Delay, 3.9 ms, $I_{VDD-VEE}$ = 80 mA

5.8 RLIM



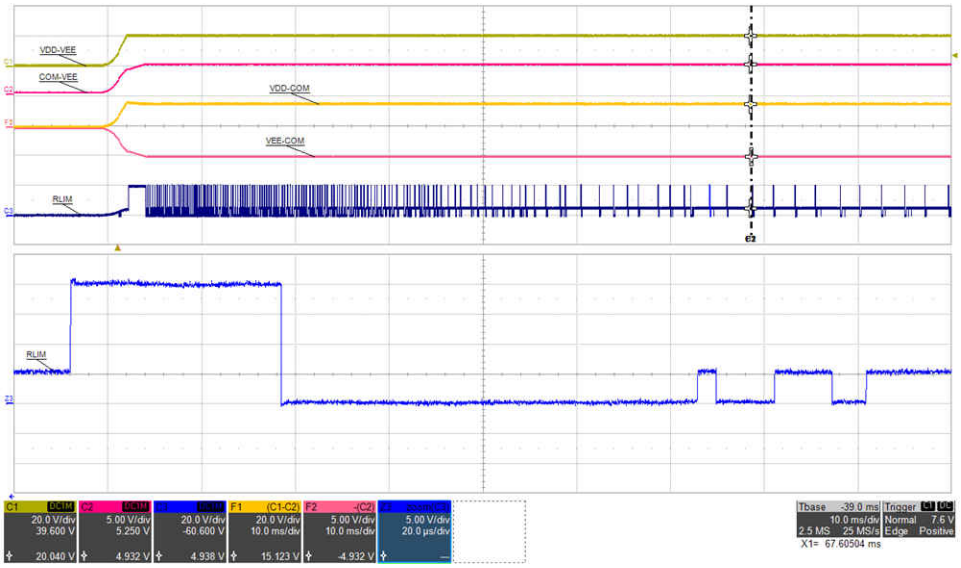
top: VDD-VEE, 20 V/div,	mid-3: VEE-COM, 5 V/div,
mid-1: COM-VEE, 5 V/div,	bot: RLIM, 20 V/div,
mid-2: VDD-COM, 20 V/div,	time = 10 ms/div

Figure 5-17. RLIM: VIN=24 V, $I_{VDD-VEE}$ = 0 mA



top: VDD-VEE, 20 V/div,	mid-3: VEE-COM, 5 V/div,
mid-1: COM-VEE, 5 V/div,	bot: RLIM, 20 V/div,
mid-2: VDD-COM, 20 V/div,	time = 10 ms/div

Figure 5-18. RLIM: VIN=24 V, $I_{VDD-VEE}$=100 mA



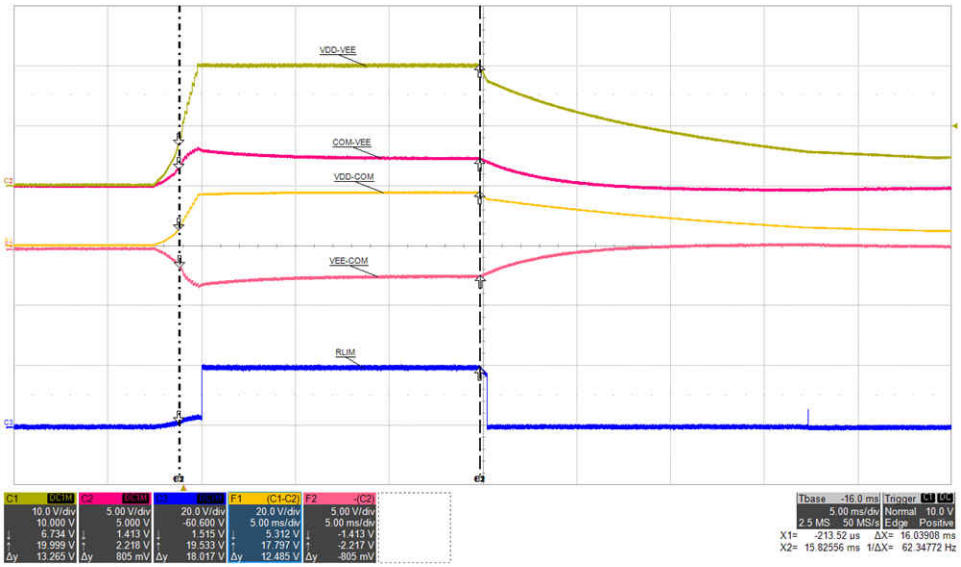
top: VDD-VEE, 20 V/div,	mid-1: COM-VEE, 5 V/div,	mid-2: VDD-COM, 20 V/div,
mid-3: VEE-COM, 5 V/div,	bot: RLIM, 20 V/div,	Zoom: RLIM, 5 V/div,
time = 10 ms/div,	time_zoom = 20 µs/div	

Figure 5-19. RLIM: VIN=24 V, $I_{VDD-VEE}$ = 100 mA

5.9 Fault Protection

5.9.1 Output UVLO

Figure 5-20 shows the effect of mismatched bias loading at startup where the load on VEE-COM is greater than the load on VDD-COM. A fixed resistive load of 340-Ω (73 mW) is applied to VEE-COM while VDD-COM is left unloaded. VDD-VEE is regulating at 20-V, as expected but VDD-COM is measuring 17.8 V (target value is 15 V) and VEE-COM is measuring 2.2 V (target value is 5 V). Since VDD-COM is not directly monitored by feedback, over-voltage protection (OVP) is not triggered even though the measured voltage is 18% above the target value. Also, since VEE-COM is overloaded, the regulated voltage is only reaching 2.2 V which is 56% below the targeted set value of 5-V, therefore, VEE-COM UVLO is triggered. RLIM is internally switched to VDD (20 V) and is attempting to overcome the imbalance by sourcing current into the capacitor midpoint, COM, connection. FBVDD and FBVEE must both be between 90%-110% of their target set value before 16-ms, which is thw maximum allowable soft-start time as defined by the internal watch-dog-timer. The 16-ms, watch-dog-timer UVLO fault protection is enabled to protect the UCC14240-Q1 from output short-circuit or soft overload conditions. Once the UVLO fault is triggered, RLIM is internally switched to VEE, helping to discharge the outputs. When activated, as illustrated in Figure 5-20, the outputs are latched off into a protected sate. EN or VIN must be recycled to clear the UVLO fault and attempt to restart the module.

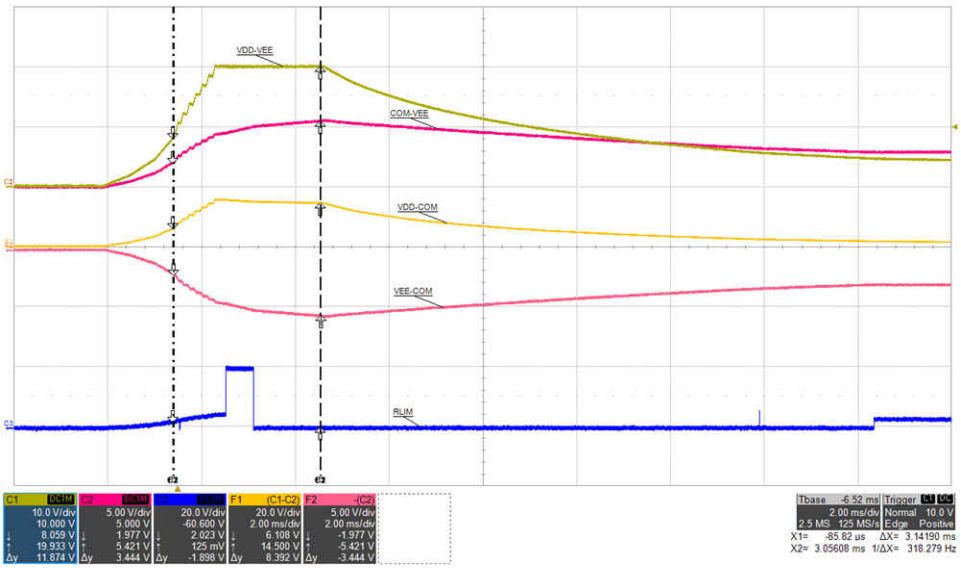


top: VDD-VEE, 10 V/div,	mid3: VEE-COM, 5 V/div,
mid1: COM-VEE, 5 V/div,	bot: RLIM, 20 V/div,
mid2: VDD-COM, 20 V/div,	time = 5 ms/div

Figure 5-20. Output UVLO, PVDD=0 mW, PVEE = 73 mW

5.9.2 Output OVP

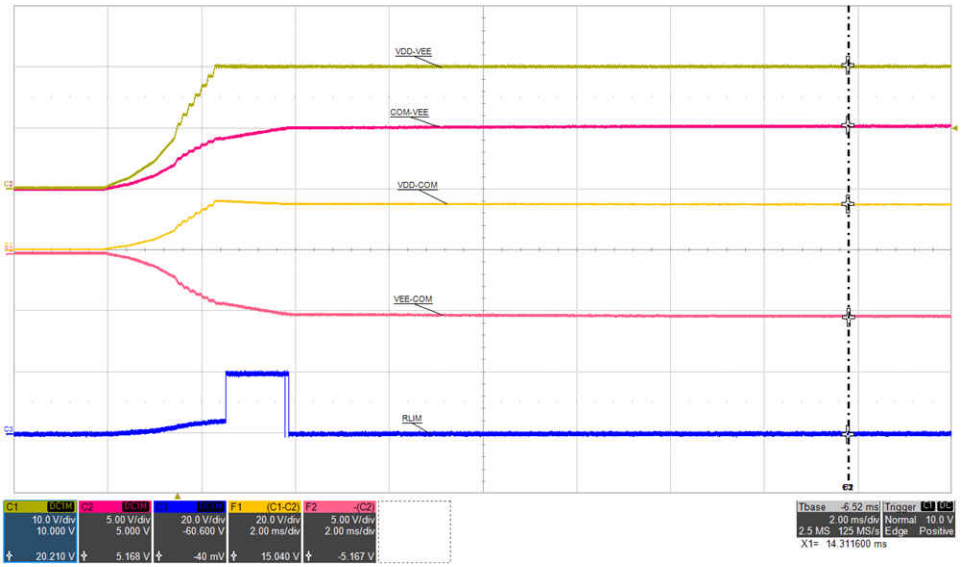
Figure 5-21 shows the effect of mismatched bias loading at startup where the load on VDD-COM is greater than the load on VEE-COM. A fixed resistive load of 910-Ω (247 mW) is applied to VDD-COM while VEE-COM is left unloaded. VDD-VEE is regulating at 20-V, as expected and VDD-COM is measuring 14.5 V (target value is 15 V) but VEE-COM is measuring 5.5 V (target value is 5 V). VEE-COM is directly monitored by FBVEE and has exceeded 110% of the set target value, triggering OVP and instantly latching both outputs off, regardless of the 16-ms watch-dog-timer. When FBVEE has detected the regulated voltage exceeding the set target value, RLIM is internally switched to VEE, sinking current from the capacitor midpoint, COM connection. When activated, as illustrated in Figure 5-21, the outputs are latched off into a protected sate. EN or VIN must be recycled to clear the OVP fault and attempt to restart the module.



top: VDD-VEE, 10 V/div,	mid3: VEE-COM, 5 V/div,
mid1: COM-VEE, 5 V/div,	bot: RLIM, 20 V/div,
mid2: VDD-COM, 20 V/div,	time = 2 ms/div

Figure 5-21. VEE OVP, VIN=24 V, PVDD=247 mW, PVEE = 0 mW

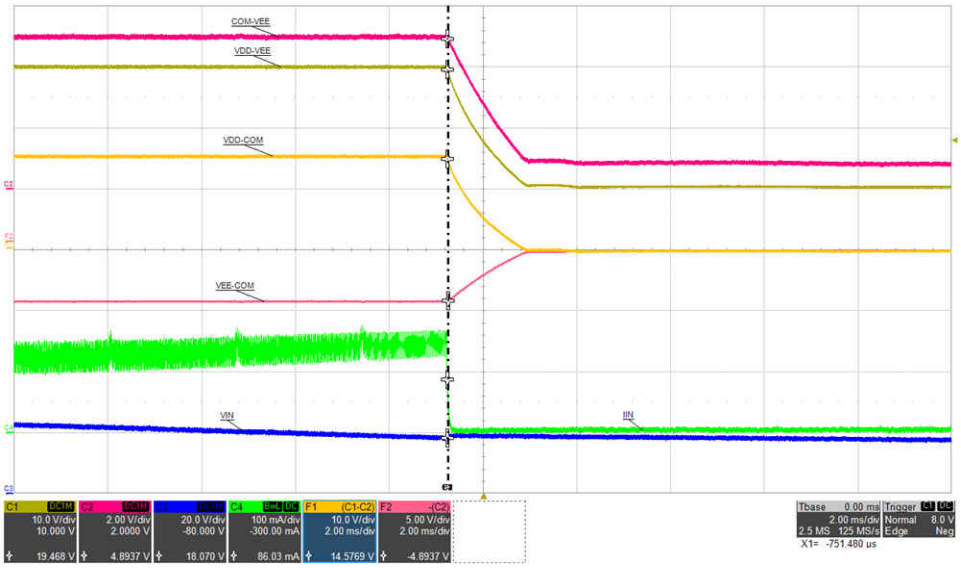
Figure 5-22 shows the same fixed resistive load of 910-Ω (247 mW) applied to VDD-COM as Figure 5-21 but the load on VEE-COM has been increased from 0-mW to 53-mW. Once both outputs are regulating, RLIM is internally connected and held to VEE, sinking current from COM, attempting to compensate for the additional load imbalance present during steady state operation.



top: VDD-VEE, 10 V/div,	mid3: VEE-COM, 5 V/div,
mid1: COM-VEE, 5 V/div,	bot: RLIM, 20 V/div),
mid2: VDD-COM, 20 V/div,	time = 2 ms/div

Figure 5-22. Normal Start, VIN=24 V, PVDD=247 mW, PVEE = 53 mW

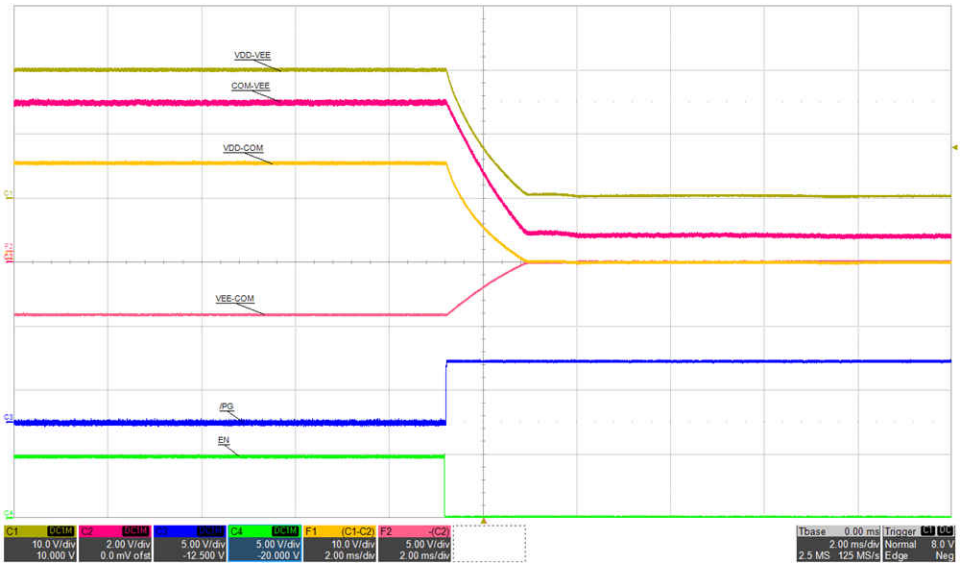
5.10 Shutdown



Note

top: COM-VEE, 2 V/div,	mid-1: VDD-VEE, 10 V/div,	mid-2: VDD-COM, 10 V/div,
mid-3: VEE-COM, 5 V/div,	mid-4: IIN, 100 mA/div,	bot: VIN, 20 V/div),
time = 2 ms/div		

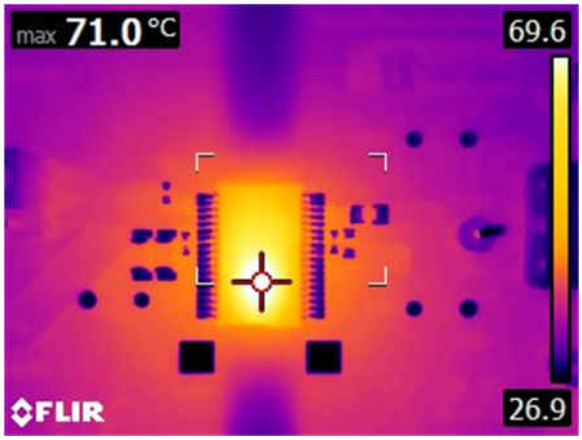
Figure 5-23. Shutdown by VIN Removal: VIN_{OFF}=18 V, $I_{VDD-VEE}$ = 80 mA



top: VDD-VEE, 10 V/div,	mid-1: COM-VEE, 2 V/div,	mid-2: VDD-COM, 10 V/div,
mid-3: VEE-COM, 5 V/div,	mid-4: /PG, 5 V/div,	bot: ENA, 5 V/div,
time = 2 ms/div		

Figure 5-24. Shutdown by EN Low: VIN=24 V, $I_{VDD-VEE}$ = 80 mA

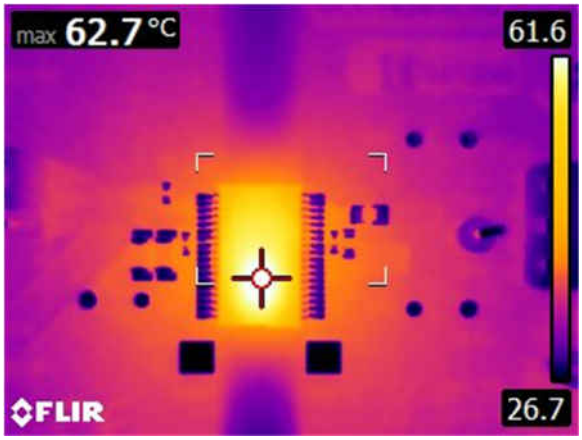
5.11 Thermal Performance



V_{IN} = 24 V	V_{DD} = 19.93 V	I_{VDD} = 100 mA
V_{VEE} = 5 V	I_{VEE} = 10 mA	P_{OUT} = 2.04 W
	T_{RISE} = 46°C (see Equation 1)	

Figure 5-25. Steady State, P_{MAX}=2 W

$$T_{RISE} = 71°C - 25°C = 46°C \quad (1)$$



V_{IN} = 24 V	V_{DD} = 19.95 V	I_{VDD} = 80 mA
V_{VEE} = 5 V	I_{VEE} = 10 mA	P_{OUT} = 1.65 W
	T_{RISE} = 37.7°C (see Equation 2)	

Figure 5-26. Rated Power, P=1.65 W

$$T_{RISE} = 62.7°C - 25°C = 37.7°C \quad (2)$$

6 Assembly and Printed Circuit Board (PCB) Layers

The UCC14240EVM-052 is designed using a four-layer, FR4, PCB. The EVM, PCB demonstrates the important use of ground planes and tented stitching vias for shielding and improving EMI performance. For higher density PCBs such as automotive traction inverters, the PCB can include several additional signal layers but similar design methodology can be applied as best as possible.

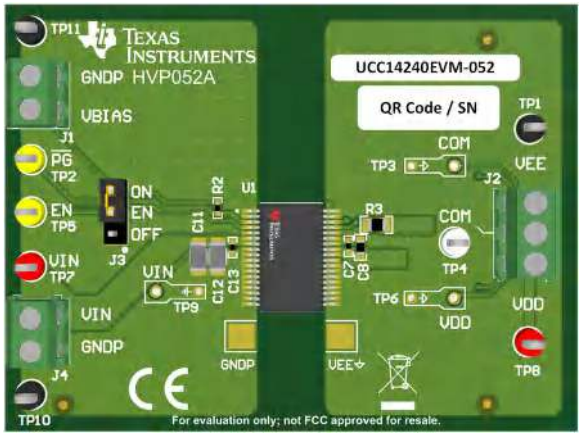


Figure 6-1. UCC14240EVM-052, Fully Assembled 3D Top View

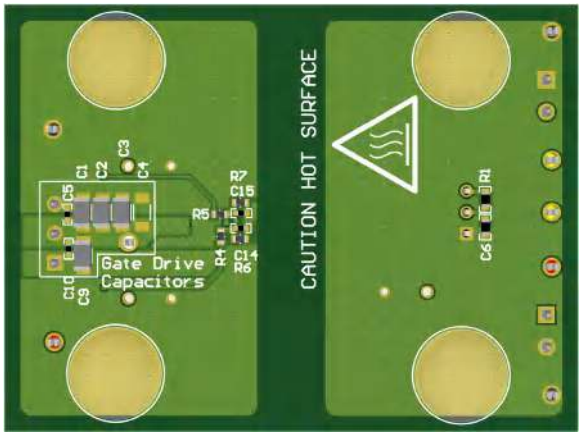


Figure 6-2. UCC14240EVM-052, Fully Assembled 3D Bottom View

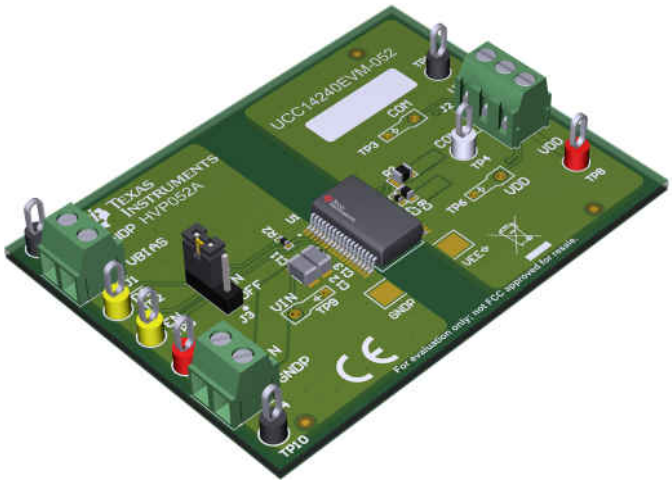


Figure 6-3. UCC14240EVM-052, 3D Angle View

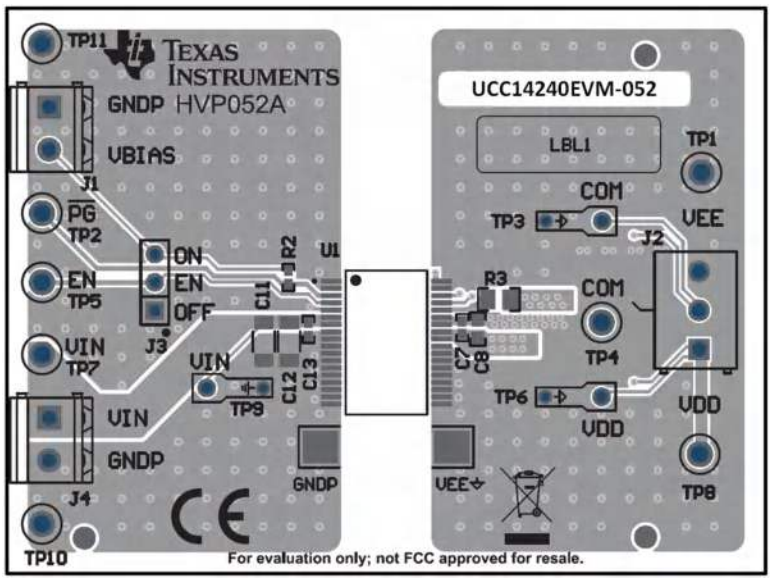


Figure 6-4. UCC14240EVM-052, PCB Top Layer, Assembly

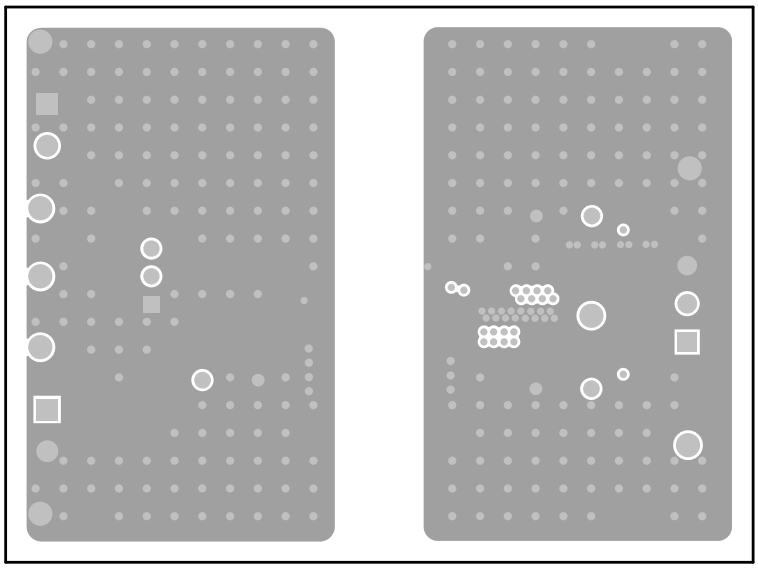


Figure 6-5. UCC14240EVM-052, GND Layer 2 (same as layer 3)

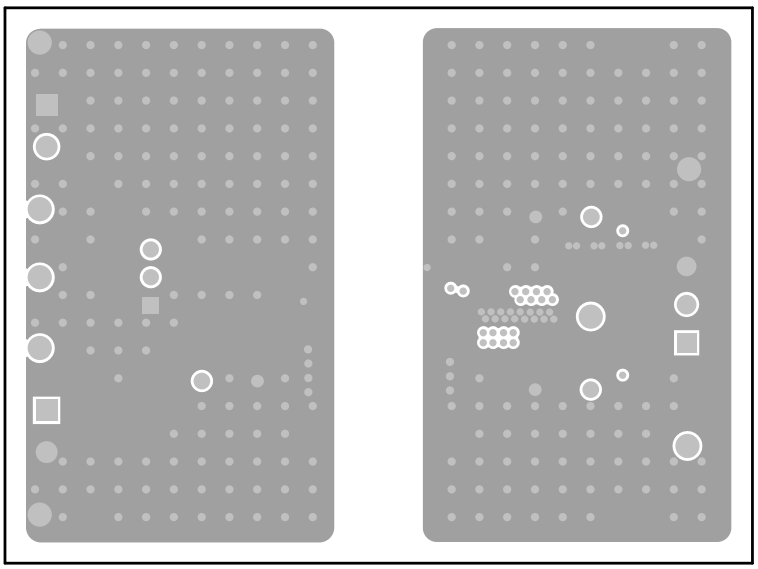


Figure 6-6. UCC14240EVM-052, GND Layer 3 (same as layer 2)

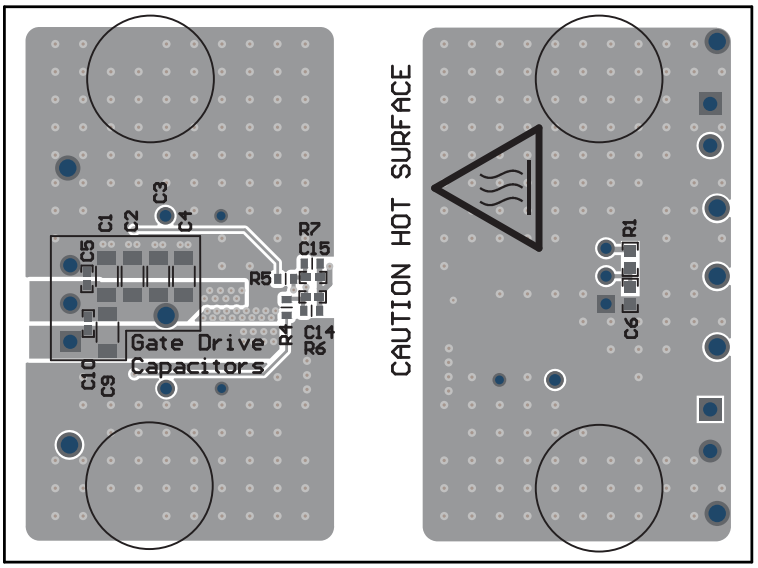


Figure 6-7. UCC14240EVM-052, PCB Bottom Layer, Assembly (mirrored view)

7 Bill of Materials (BOM)

Table 7-1. UCC14240EVM-052 BOM

Ref Des	Qty	Description	Part Number	Mfr
PCB1	1	Printed circuit board	HVP052A	Any
C1, C2, C3, C9, C11, C12	6	Capacitor, ceramic, 35 V, +/- 10%, X7R, 10 µF, AEC-Q200 Grade 1, 1206	CGA5L1X7R1V106K160AC	TDK
C5, C7, C10, C13	4	Capacitor, ceramic, 50 V, +/- 10%, X7R, 0.1 µF, AEC-Q200 Grade 1, 0402	GCM155R71H104KE02D	MuRata
C6	1	Capacitor, ceramic, 50 V, +/- 10%, X7R, 0.1 µF, AEC-Q200 Grade 1, 0603	CGA3E2X7R1H104K080AA	TDK
C8	1	Capacitor, ceramic, 35 V, +/- 10%, X6S, 2.2 µF, 0603	GRT188C8YA225KE13D	Murata
C14, C15	2	Capacitor, ceramic, 50 V, +/- 10%, X7R, 330 pF, AEC-Q200 Grade 1, 0402	CGA2B2X7R1H331K050BA	TDK
H1, H2, H3, H4	4	Bumpon, hemisphere, 0.44 X 0.20, Clear, Adhesive	SJ-5303 (CLEAR)	3M
J1, J4	2	Terminal block, 2x1, 3.81 mm, 24-16 AWG, 10 A, 300 VAC, TH	691214310002	Wurth Elektronik
J2	1	Terminal block, 3.5mm, 3x1, TH	691214110003	Wurth Elektronik
J3	1	Header, 100 mil, 3x1, TH	PEC03SAAN	Sullins
R1	1	Resistor, 1%, 0.1 W, AEC-Q200 Grade 0, 5.11 kΩ, 0603	CRCW06035K11FKEA	Vishay-Dale
R2	1	Resistor, 5%, 0.1 W, AEC-Q200 Grade 0, 100 kΩ, 0402	ERJ-2GEJ104X	Panasonic
R3	1	Resistor, 1%, 0.125 W, AEC-Q200 Grade 0, 1.00 kΩ, 0805	CRCW08051K00FKEA	Vishay-Dale
R4	1	Resistor, 0.1%, 1/10 W, 69.8 kΩ, 0603	ERA-3AEB6982V	Panasonic
R5, R7	2	Resistor, 0.1%, 1/10 W, 49.9 kΩ, 0603	ERA-3AEB4992V	Panasonic
R6	1	Resistor, 0.1%, 1/10 W, 10 kΩ, 0603	ERA-3ARB103V	Panasonic
SH-J1	1	Shunt, 100mil, gold plated, black, 1x2, Shunt	SNT-100-BK-G	Samtec
TP1, TP10, TP11	3	Test Point, multipurpose, black, TH	5011	Keystone
TP2, TP5	2	Test Point, multipurpose, yellow, TH	5014	Keystone
TP4	1	Test Point, multipurpose, white, TH	5012	Keystone
TP7, TP8	2	Test Point, multipurpose, red< TH	5010	Keystone
U1	1	2-W, 24-V VIN, 24-V VOUT, > 3 kVRMS, isolated DC/DC module, SOIC36	UCC14240QDWNQ1	Texas Instruments
U1-alternate	0	2-W, 24-V VIN, 24-V VOUT, > 5 kVRMS, isolated DC/DC module, SOIC36	UCC14241QDWNQ1	Texas Instruments
C4	0	Capacitor, ceramic, 35 V, +/- 10%, X7R, AEC-Q200 Grade 1, 10 µF, 1206	CGA5L1X7R1V106K160AC	TDK

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2022) to Revision B (March 2023)	Page
• Changed text in *Abstract* section	1
• Added *U1 Component Selection* section	3
• Added *U1-alternate* to *Bill of Materials*	30

Changes from Revision * (July 2021) to Revision A (December 2022)	Page
• Initial release	3

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

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8. *Limitations on Damages and Liability:*

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9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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