



# SY58611U

## 3.2Gbps Precision, LVDS 2:1 MUX with Internal Termination and Fail Safe Input

### General Description

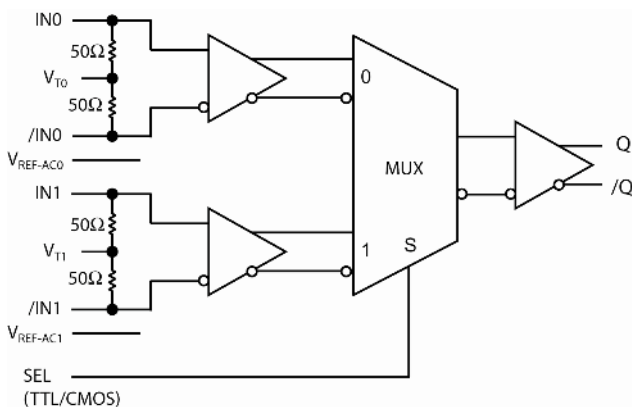
The SY58611U is a 2.5V, high-speed, fully differential LVDS 2:1 MUX capable of processing clocks up to 2.5GHz and data up to 3.2Gbps. SY58611U is optimized to provide a buffered output of the selected input with less than 20ps of skew and less than 10ps<sub>pp</sub> total jitter. Patented MUX Isolation design reduces crosstalk and provides superior signal integrity.

The differential inputs include Micrel's unique, 3-pin input termination architecture that interfaces to LVPECL, LVDS or CML differential signals, (AC- or DC-coupled) as small as 100mV<sub>PK</sub> (200mV<sub>pp</sub>) without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an integrated reference voltage (V<sub>REF-AC</sub>) is provided to bias the V<sub>T</sub> pin. The output is LVDS compatible, with rise/fall times guaranteed to be less than 120ps.

The SY58611U operates from a 2.5V ±5% supply and is guaranteed over the full industrial temperature range (-40°C to +85°C). For applications that require CML or LVPECL output, consider the SY58609U and SY58610U, 2:1 MUX with 400mV and 800mV output swings respectively. The SY58611U is part of Micrel's high-speed, Precision Edge<sup>®</sup> product line.

Datasheets and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

### Functional Block Diagram



United States Patent No. RE44,134

Precision Edge is a registered trademark of Micrel, Inc.



Precision Edge<sup>®</sup>

### Features

- Selects between two sources and provides buffered copy of the selected input signal
- Fail Safe Input
  - Prevents output from oscillating when input is invalid or removed
- Guaranteed AC performance over temperature and voltage:
  - DC-to > 3.2Gbps throughput
  - <420ps typical propagation delay (IN-to-Q)
  - <120ps rise/fall times
- Unique, patented internal termination and VT pin accepts DC- and AC-coupled inputs (CML, PECL, LVDS)
- Unique, patented MUX input isolation design minimizes adjacent channel crosstalk
- Ultra-low jitter design
  - <1ps<sub>RMS</sub> cycle-to-cycle jitter
  - <10ps<sub>pp</sub> total jitter
  - <1ps<sub>RMS</sub> random jitter
  - <10ps<sub>pp</sub> deterministic jitter
- 2.5V ±5% power supply operation
- Industrial temperature range: -40°C to +85°C
- Available in 16-pin (3mm x 3mm) QFN package

### Applications

- All SONET clock distribution
- Fibre Channel clock and data distribution
- Gigabit Ethernet clock or data distribution
- Backplane distribution

### Markets

- DataCom and Telecom
- Storage
- ATE
- Test and Measurement

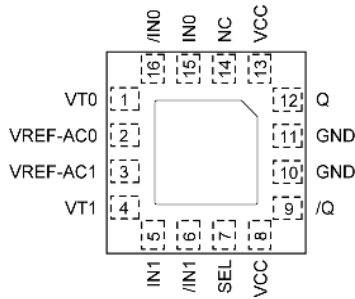
## Ordering Information<sup>(1)</sup>

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58611UMG	QFN-16	Industrial	611U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY58611UMGTR <sup>(2)</sup>	QFN-16	Industrial	611U with Pb-Free bar-line indicator	NiPdAu Pb-Free

**Notes:**

- Contact factory for die availability. Dice are guaranteed at  $T_A = 25^\circ\text{C}$ , DC Electricals only.
- Tape and Reel.

## Pin Configuration



16-Pin QFN

## Truth Table

SEL	Output
0	IN0 Selected
1	IN1 Selected

## Pin Description

Pin Number	Pin Name	Pin Function
1, 4	VT0, VT1	Input Termination Center-Tap: Each side of the differential input pair terminates to the VT pin. This pin provides a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" subsection.
2, 3	VREF-AC0, VREF-AC1	Reference Voltage: These outputs bias to $V_{CC}-1.2\text{V}$ . They are used for AC-coupling inputs IN and /IN. Connect VREF-AC directly to the corresponding VT pin. Bypass with $0.01\mu\text{F}$ low ESR capacitor to VCC. Due to limited drive capability, the VREF-AC pin is only intended to drive its respective VT pin. Maximum sink/source current is $\pm 0.5\text{mA}$ . See "Input Interface Applications" subsection.
5, 6 15, 16	IN1, /IN1 IN0, /IN0	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-Coupled differential signals as small as $100\text{mV}$ ( $200\text{mV}_{PP}$ ). Each pin of the pairs internally terminates with $50\Omega$ to the $V_T$ pin. If the input swing falls below a certain threshold (typical $30\text{mV}$ ), the Fail Safe Input (FSI) feature will guarantee a stable output by latching the output to its last valid state. See "Input Interface Applications" subsection.
7	SEL	Single-Ended Input: This single-ended TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a $25\text{k}\Omega$ pull-up resistor and will default to logic HIGH state if left open. The input-switching threshold is $V_{CC}/2$ .
8, 13	VCC	Positive Power Supply: Bypass with $0.1\mu\text{F}/0.01\mu\text{F}$ low ESR capacitors as close to the $V_{CC}$ pins as possible.
9, 12	/Q, Q	LVDS Differential Output Pair: Differential buffered output copy of the selected input signal. The output swing is typically $325\text{mV}$ . Normally terminated $100_\Omega$ across the output (Q and /Q). See "LVDS Output Interface Applications" subsection.
10, 11	GND, Exposed pad	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
14	NC	No connect.

### Absolute Maximum Ratings<sup>(1)</sup>

Supply Voltage ( $V_{CC}$ ) ..... -0.5V to +4.0V  
 Input Voltage ( $V_{IN}$ ) ..... -0.5V to  $V_{CC}$   
 LVDS Output Current ( $I_{OUT}$ ) .....  $\pm 10$ mA  
 Input Current  
     Source or Sink Current on (IN, /IN).....  $\pm 50$ mA  
 Current ( $V_{REF}$ )  
     Source or sink current on  $V_{REF-AC}$  <sup>(4)</sup> .....  $\pm 0.5$ mA  
 Maximum operating Junction Temperature ..... 125°C  
 Lead Temperature (soldering, 20sec.) ..... 260°C  
 Storage Temperature ( $T_s$ ) ..... -65°C to +150°C

### Operating Ratings<sup>(2)</sup>

Supply Voltage ( $V_{CC}$ ) ..... +2.375V to +2.635V  
 Ambient Temperature ( $T_A$ ) ..... -40°C to +85°C  
 Package Thermal Resistance<sup>(3)</sup>  
 QFN  
     Still-air ( $\theta_{JA}$ ) ..... 60°C/W  
     Junction-to-Board ( $\psi_{JB}$ )..... 33°C/W

### DC Electrical Characteristics<sup>(5)</sup>

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{CC}$	Power Supply Voltage Range		2.375	2.5	2.625	V
$I_{CC}$	Power Supply Current	No load, max. $V_{CC}$		40	60	mA
$R_{IN}$	Input Resistance (IN-to- $V_T$ , /IN-to- $V_T$ )		45	50	55	$\Omega$
$R_{DIFF\_IN}$	Differential Input Resistance (IN-to-/IN)		90	100	110	$\Omega$
$V_{IH}$	Input HIGH Voltage (IN, /IN)		1.2		$V_{CC}$	V
$V_{IL}$	Input LOW Voltage (IN, /IN)		0.2		$V_{IH}-0.1$	V
$V_{IN}$	Input Voltage Swing (IN, /IN)	see Figure 3a, Note 6	0.1		1.0	V
$V_{DIFF\_IN}$	Differential Input Voltage Swing ( IN - /IN )	see Figure 3b	0.2			V
$V_{IN\_FSI}$	Input Voltage Threshold that Triggers FSI			30	100	mV
$V_{REF-AC}$	AC Reference Voltage	$I_{VREF-AC} = \pm 0.5\text{mA}$	$V_{CC}-1.3$		$V_{CC}-1.0$	V
$V_{T\_IN}$	Voltage from Input to $V_T$				1.28	V

**Notes:**

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.  $\psi_{JB}$  and  $\theta_{JA}$  values are determined for a 4-layer board in still-air number, unless otherwise stated.
4. Due to the limited drive capability, use for input of the same package only.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6.  $V_{IN}$  (max) is specified when  $V_T$  is floating.

## LVDS Output DC Electrical Characteristics<sup>(7)</sup>

$V_{CC} = +2.5V \pm 5\%$ ,  $R_L = 100\Omega$  across the output pair;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OUT}$	Output Voltage Swing (Q, /Q)	See Figure 3a	250	325		mV
$V_{DIFF\_OUT}$	Differential Output Voltage Swing  Q-/Q	See Figure 3b	500	650		mV
$V_{OCM}$	Output Common Mode Voltage (Q, /Q)	See Figure 5b	1.125	1.20	1.275	V
$\Delta V_{OCM}$	Change in Common Mode Voltage (Q, /Q)	See Figure 5b	-50		50	mV

## LVTTL/CMOS DC Electrical Characteristics<sup>(7)</sup>

$V_{CC} = 2.5V \pm 5\%$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IH}$	Input HIGH Voltage		2.0			V
$V_{IL}$	Input LOW Voltage				0.8	V
$I_{IH}$	Input HIGH Current		-125		30	$\mu A$
$I_{IL}$	Input LOW Current		-300			$\mu A$

### Notes:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

## AC Electrical Characteristics<sup>(8)</sup>

$V_{CC} = +2.5V \pm 5\%$ ,  $R_L = 100\Omega$  across the output pair; Input  $t_r/t_f \leq 300ps$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$f_{MAX}$	Maximum Frequency	NRZ Data	3.2			Gbps
		$V_{OUT} > 200mV$ Clock	2.5	3		GHz
$t_{PD}$	Propagation Delay IN-to-Q	$V_{IN}: 100mV-200mV$	190	330	470	ps
		$V_{IN}: > 200mV$	150	280	420	ps
	SEL-to-Q		150		450	ps
$t_{Skew}$	Input-to-Input Skew	Note 9, 10		5	20	ps
	Part-to-Part Skew	Note 11			150	ps
$t_{Jitter}$	Data Random Jitter	Note 12			1	ps <sub>RMS</sub>
	Deterministic Jitter	Note 13			10	ps <sub>PP</sub>
	Clock Cycle-to-Cycle Jitter	Note 14			1	ps <sub>RMS</sub>
	Total Jitter	Note 15			10	ps <sub>PP</sub>
$t_r, t_f$	Output Rise/Fall Times (20% to 80%)	At full output swing.	40	80	120	ps
	Duty Cycle	Differential I/O	47		53	%

### Notes:

8. High-frequency AC-parameters are guaranteed by design and characterization.
9. Input-to-Input skew is the time difference between the two inputs and one output, under identical input transitions.
10. Input-to-Input Skew is included in IN-to-Q propagation delay.
11. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature, same transition edge, and no skew at the edges at the respective inputs.
12. Random jitter is measured with a K28.7 pattern, measured at  $\leq f_{MAX}$ .
13. Deterministic jitter is measured at 2.5Gbps with both K28.5 and  $2^{23}-1$  PRBS pattern.
14. Cycle-to-cycle jitter definition: the variation period between adjacent cycles over a random sample of adjacent cycle pairs.  $t_{JITTER\_CC} = T_n - T_{n+1}$ , where T is the time between rising edges of the output signal.
15. Total jitter definition: with an ideal clock input frequency of  $\leq f_{MAX}$  (device), no more than one output edge in  $10^{12}$  output edges will deviate by more than the specified peak-to-peak jitter value.

## Functional Description

### Fail-Safe Input (FSI)

The input includes a special fail-safe circuit to sense the amplitude of the input signal and to latch the output when there is no input signal present, or when the amplitude of the input signal drops sufficiently below  $100\text{mV}_{\text{PK}}$  ( $200\text{mV}_{\text{PP}}$ ), typically  $30\text{mV}_{\text{PK}}$ . Refer to Figure 1b.

### Input Clock Failure Case

If the input clock fails to a floating, static, or extremely low signal swing such that the voltage swing across the input pair is significantly less than  $100\text{mV}$ , FSI

function will eliminate a metastable condition and latch the output to the last valid state. No ringing and no undetermined state will occur at the output under these conditions. The output recovers to normal operation once the input signal returns to a valid state with a typical swing greater than  $30\text{mV}$ .

Note that the FSI function will not prevent duty cycle distortion in case of a slowly deteriorating (but still toggling) input signal. Due to the FSI function, the propagation delay will depend on rise and fall time of the input signal and on its amplitude. Refer to "Typical Operating Characteristics" for detailed information.

## Timing Diagrams

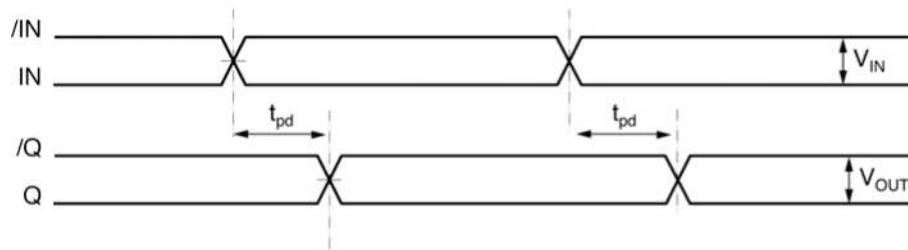


Figure 1a. Propagation Delay

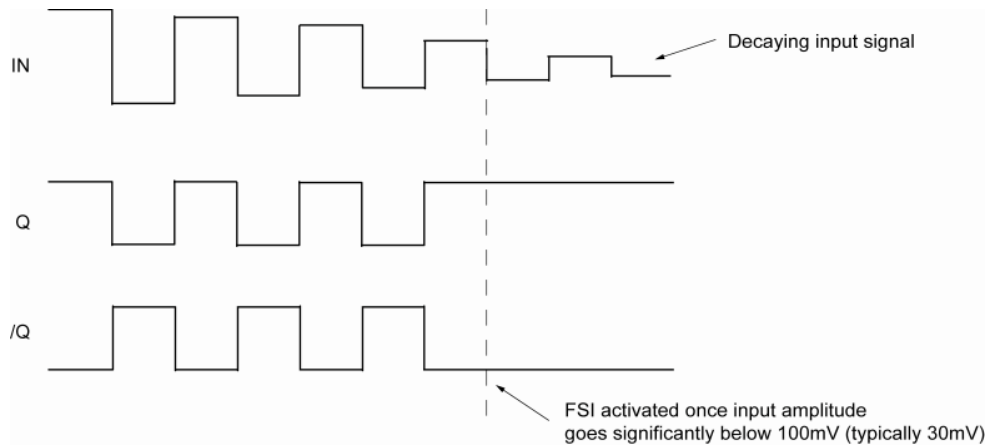


Figure 1b. Fail-Safe Feature

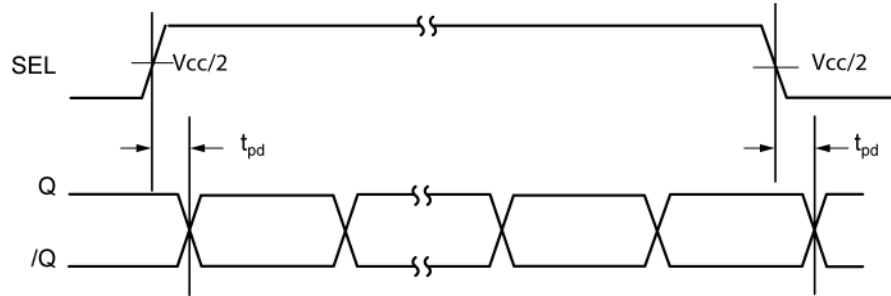


Figure 1c. SEL-to-Q Delay

### Input Stage

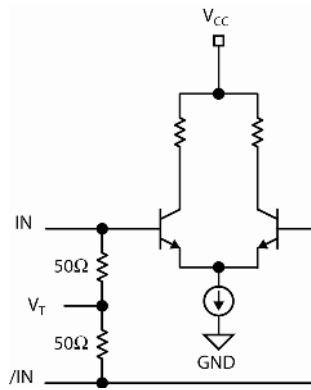


Figure 2. Simplified Differential Input Buffer

### Single-Ended and Differential Swings

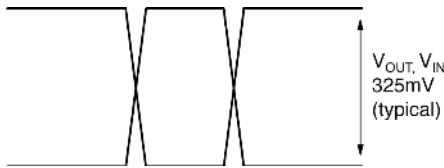


Figure 3a. Single-Ended Swing

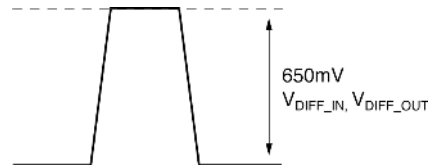
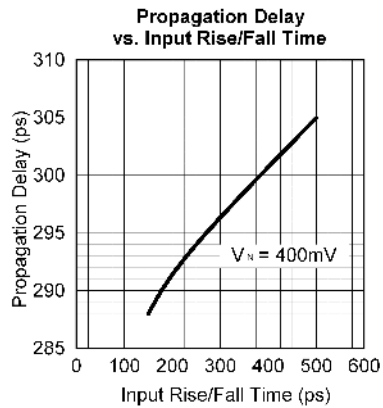
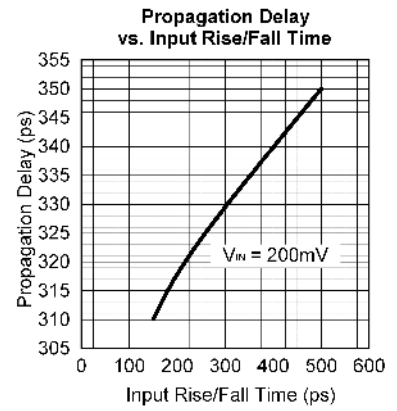
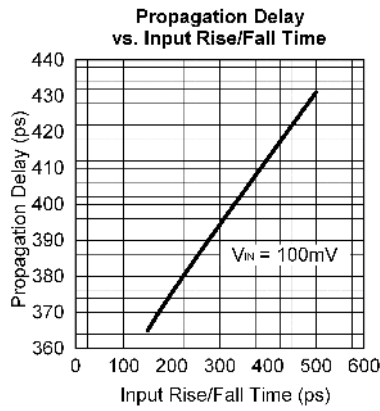
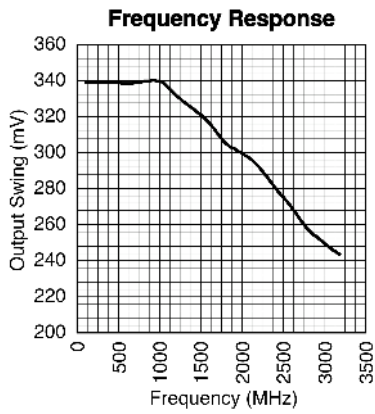


Figure 3b. Differential Swing

## Typical Characteristics

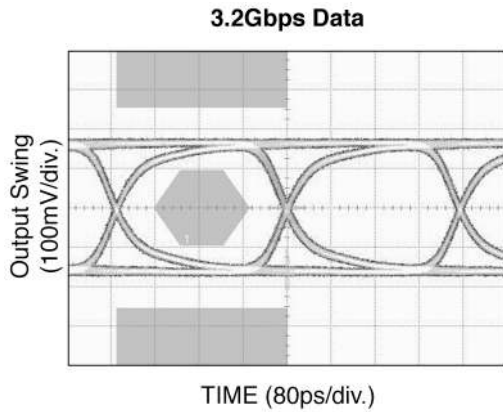
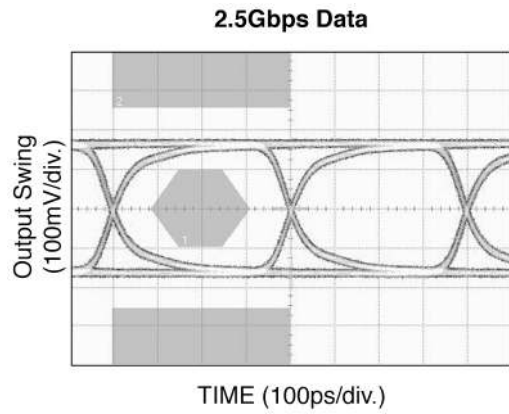
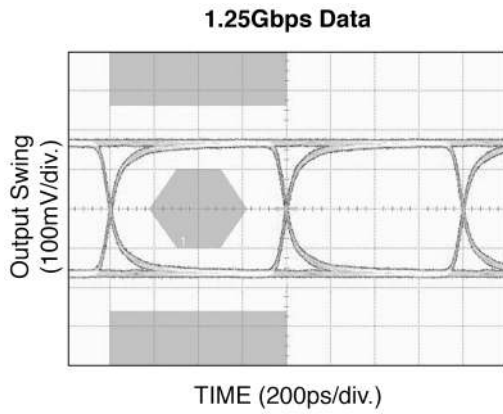
$V_{CC} = 2.5V$ ,  $GND = 0V$ ,  $V_{IN} = 100mV$ ,  $R_L = 100\Omega$  across the output pair,  $T_A = 25^\circ C$ , unless otherwise stated.





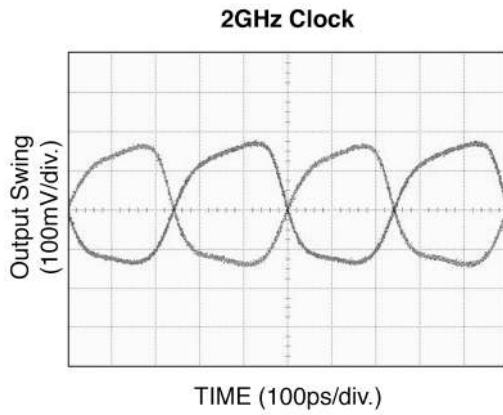
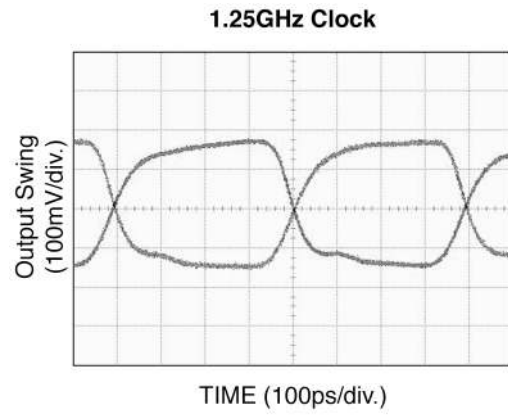
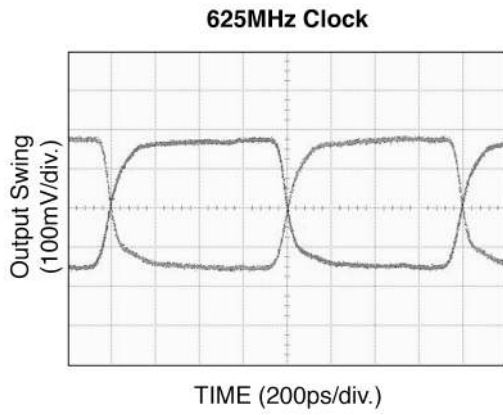
### Functional Characteristics

$V_{CC} = 2.5V$ ,  $GND = 0V$ ,  $V_{IN} = 325mV$ ,  $R_L = 100\Omega$  across the output pair,  $T_A = 25^\circ C$ , unless otherwise stated.

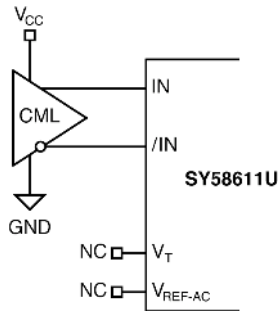


**Functional Characteristics** (continued)

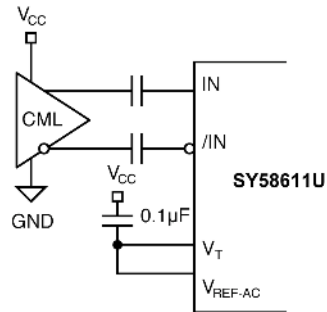
$V_{CC} = 2.5V$ ,  $GND = 0V$ ,  $V_{IN} = 325mV$ ,  $R_L = 100\Omega$  across the output pair,  $T_A = 25^\circ C$ , unless otherwise stated.



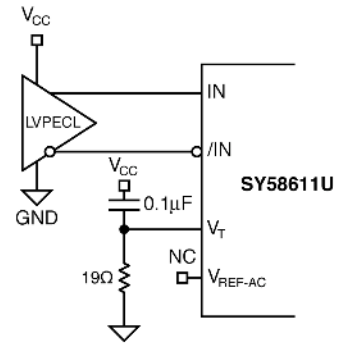
## Input Interface Applications



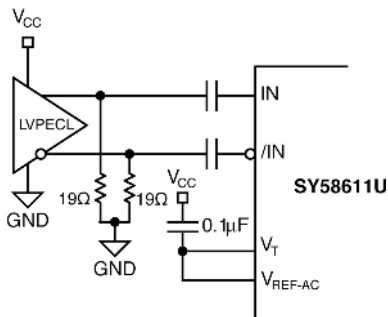
**Figure 4a. CML Interface (DC-Coupled)**  
Option: May connect  $V_T$  to  $V_{CC}$



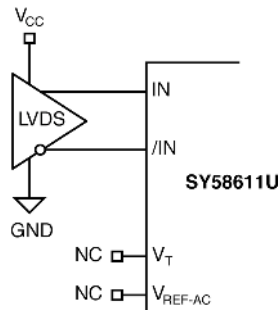
**Figure 4b. CML Interface (AC-Coupled)**



**Figure 4c. LVPECL Interface (DC-Coupled)**



**Figure 4d. LVPECL Interface (AC-Coupled)**



**Figure 4e. LVDS Interface (AC-Coupled)**

## LVDS Output Interface Applications

LVDS specifies a small swing of 325mV typical, on a nominal 1.2V common mode above ground. The common mode voltage has tight limits to permit large variations in the ground between and LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is kept to a minimum, to keep EMI low.

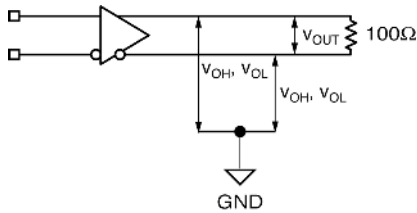


Figure 5a. LVDS Differential Measurement

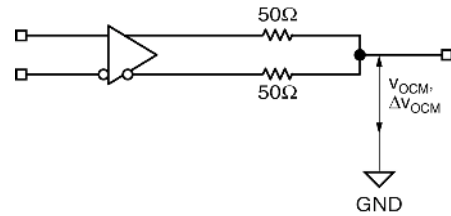
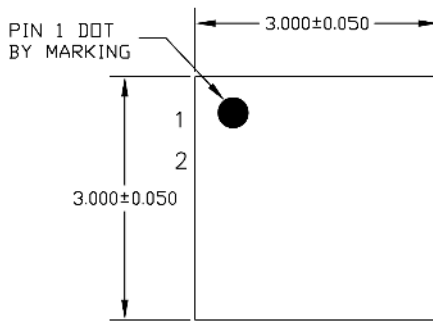


Figure 5b. LVDS Common Mode Measurement

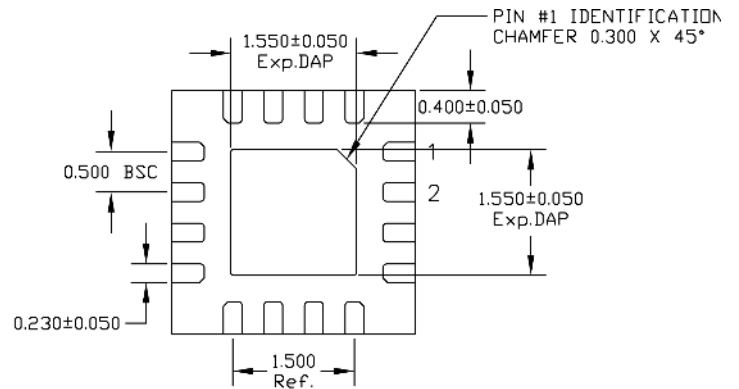
## Related Products and Support Documentation

Part Number	Function	Data Sheet Link
SY58609U	4.25Gbps Precision, CML 2:1 MUX with Internal Termination and Fail Safe Input	<a href="http://www.micrel.com/_PDF/HBW/sy58609u.pdf">http://www.micrel.com/_PDF/HBW/sy58609u.pdf</a>
SY58610U	3.2Gbps Precision, LVPECL 2:1 MUX with Internal Termination and Fail Safe Input	<a href="http://www.micrel.com/_PDF/HBW/sy58610u.pdf">http://www.micrel.com/_PDF/HBW/sy58610u.pdf</a>
HBW Solutions	New Products and Termination Application Notes	<a href="http://www.micrel.com/page.do?page=/product-info/as/HBWsolutions.shtml">http://www.micrel.com/page.do?page=/product-info/as/HBWsolutions.shtml</a>

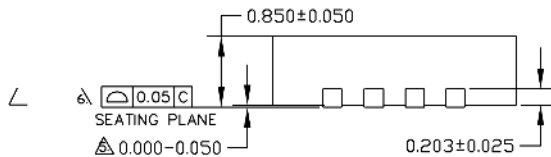
**Package Information**



TOP VIEW



BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
  2. MAX. PACKAGE WARPAGE IS 0.05 mm.
  3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
  4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
- ⚠ APPLIED ONLY FOR TERMINALS.  
 ⚠ APPLIED FOR EXPOSED PAD AND TERMINALS.

**16-Pin (3mm x 3mm) QFN**

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