

# 54LS/74LS256

011117

## DUAL 4-BIT ADDRESSABLE LATCH

**DESCRIPTION** — The '256 is a dual 4-bit addressable latch with common control inputs; these include two Address inputs ( $A_0$ ,  $A_1$ ), an active LOW Enable input ( $\bar{E}$ ) and an active LOW Clear input ( $\bar{CL}$ ). Each latch has a Data input ( $D$ ) and four outputs ( $Q_0$  —  $Q_3$ ).

When the Enable ( $\bar{E}$ ) is HIGH and the Clear input ( $\bar{CL}$ ) is LOW, all outputs ( $Q_0$  —  $Q_3$ ) are LOW. Dual 4-channel demultiplexing occurs when the  $\bar{CL}$  and  $\bar{E}$  are both LOW. When  $\bar{CL}$  is HIGH and  $\bar{E}$  is LOW, the selected output ( $Q_0$  —  $Q_3$ ), determined by the Address inputs, follows  $D$ . When the  $\bar{E}$  goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ( $\bar{E}$  = LOW,  $\bar{CL}$  = HIGH), changing more than one bit of the Address ( $A_0$ ,  $A_1$ ) could impose a transient wrong address. Therefore, this should be done only while in the memory mode ( $\bar{E}$  =  $\bar{CL}$  = HIGH).

- SERIAL-TO-PARALLEL CAPABILITY
- OUTPUT FROM EACH STORAGE BIT AVAILABLE
- RANDOM (ADDRESSABLE) DATA ENTRY
- EASILY EXPANDABLE
- ACTIVE LOW COMMON CLEAR

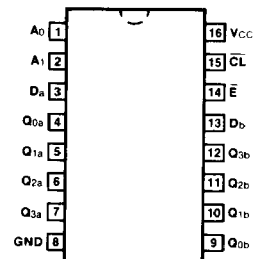
**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$ , $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$ , $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	74LS256PC		9B
Ceramic DIP (D)	A	74LS256DC	54LS256DM	6B
Flatpak (F)	A	74LS256FC	54LS256FM	4L

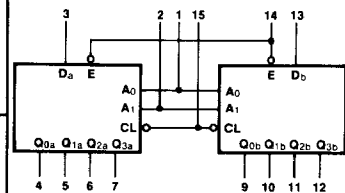
**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$A_0$ , $A_1$	Common Address Inputs	0.5/0.25
$D_a$ , $D_b$	Data Inputs	0.5/0.25
$\bar{E}$	Common Enable Input (Active LOW)	1.0/0.5
$\bar{CL}$	Conditional Clear Input (Active LOW)	0.5/0.25
$Q_{0a}$ — $Q_{3a}$	Side A Latch Outputs	10/5.0 (2.5)
$Q_{0b}$ — $Q_{3b}$	Side B Latch Outputs	10/5.0 (2.5)

### CONNECTION DIAGRAM PINOUT A



### LOGIC SYMBOL



$V_{CC}$  = Pin 16  
GND = Pin 8

**TRUTH TABLE**

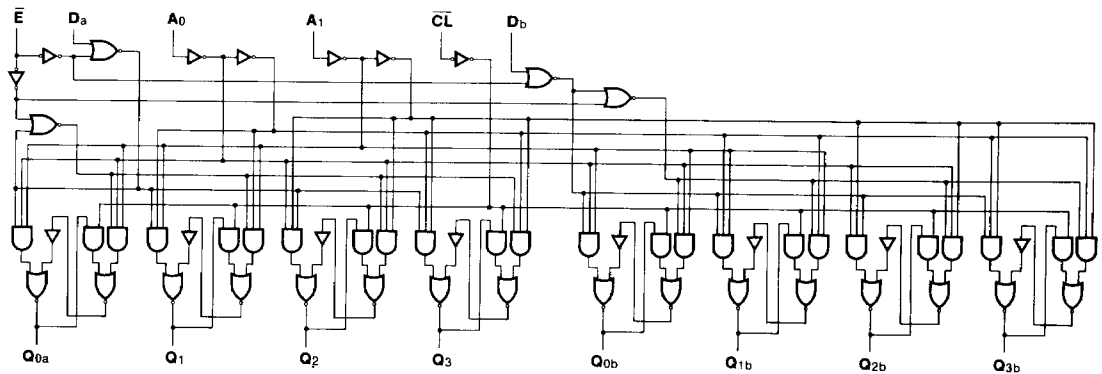
INPUTS				OUTPUTS				MODE
$\overline{CL}$	$\overline{E}$	A <sub>0</sub>	A <sub>1</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	
L	H	X	X	L	L	L	L	Clear
L	L	L	L	D	L	L	L	Demultiplex
L	L	H	L	L	D	L	L	
L	L	L	H	L	L	D	L	
L	L	H	H	L	L	L	D	
H	H	X	X	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Memory
H	L	L	L	D	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Addressable Latch
H	L	H	L	Q <sub>t-1</sub>	D	Q <sub>t-1</sub>	Q <sub>t-1</sub>	
H	L	L	H	Q <sub>t-1</sub>	Q <sub>t-1</sub>	D	Q <sub>t-1</sub>	
H	L	H	H	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	D	

t-1 = Bit time before address change or rising edge of E  
 H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial

**MODE SELECTION**

$\overline{E}$	$\overline{CL}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 4-Channel Demultiplexers
H	L	Clear

**LOGIC DIAGRAM**



**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I <sub>CC</sub>	Power Supply Current		25	mA	V <sub>CC</sub> = Max

**AC CHARACTERISTICS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		C <sub>L</sub> = 15 pF			
		Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay E̅ to Q <sub>n</sub>		27 24	ns	Figs. 3-1, 3-9
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D <sub>n</sub> to Q <sub>n</sub>		30 20	ns	Figs. 3-1, 3-5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> to Q <sub>n</sub>		30 20	ns	Figs. 3-1, 3-20
t <sub>PHL</sub>	Propagation Delay CL to Q <sub>n</sub>		18	ns	Figs. 3-1, 3-16

**AC OPERATING REQUIREMENTS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25° C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t <sub>s</sub> (H)	Setup Time HIGH D <sub>n</sub> to E̅	20		ns	Fig. 3-13
t <sub>h</sub> (H)	Hold Time HIGH D <sub>n</sub> to E̅	0		ns	Fig. 3-13
t <sub>s</sub> (L)	Setup Time LOW D <sub>n</sub> to E̅	15		ns	Fig. 3-13
t <sub>h</sub> (L)	Hold Time LOW D <sub>n</sub> to E̅	0		ns	Fig. 3-13
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time HIGH or LOW, A <sub>n</sub> to E̅	0		ns	Fig. 3-21
t <sub>w</sub> (L)	E̅ Pulse Width LOW	17		ns	Fig. 3-21