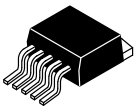
CAT6243

1 Amp Adjustable CMOS LDO Voltage Regulator

ON Semiconductor®

www.onsemi.com

WDFN−6
3 x 3 mm
CASE 511AP



DPAK−5
TO−252
CASE 369AE

Description

The CAT6243 is a low dropout CMOS voltage regulator providing up to 1000 mA of output current with fast response to load current and line voltage changes. CAT6243 offers a user adjustable output voltage from 0.8 V to 5.0 V and its low quiescent current make CAT6243 ideal for energy conscious designs. CAT6243 is available in a DPAK−5 5−lead packages and in a space saving 3 mm x 3 mm WDFN−6 package with a power pad for heat sinking to the PCB.

Features

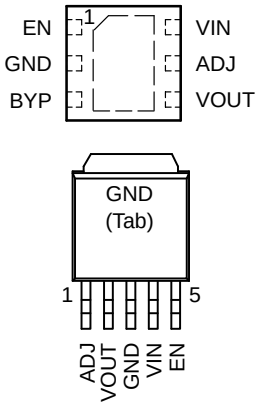
- Guaranteed 1000 mA Continuous Output Current
- V_{OUT}: 0.8 V to 5.0 V
- Dropout Voltage of 350 mV Typical at 1000 mA
- ±2.0% Output Voltage Accuracy at Room Temperature
- No−load Ground Current of 70 μA Typical
- Full−load Ground Current of 140 μA Typical
- “Zero” Current Shutdown Mode
- Under Voltage Lockout
- Stable with Ceramic Output Capacitors
- Current Limit and Thermal Protection
- 4 and 5 Lead DPAK−5 and 3 mm x 3 mm WDFN−6 Power Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- DSP Core and I/O Voltages
- FPGAs, ASICs
- PDAs, Mobile Phones, GPS
- Camcorders and Cameras
- Hard Disk Drives

PIN CONNECTIONS

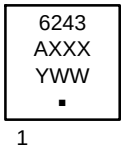
(Top Views)



ORDERING INFORMATION

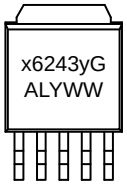
See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

MARKING DIAGRAMS



6243	= Specific Device Code
A	= Assembly Location
XXX	= Last Three Digits of Assembly Lot Number
Y	= Production Year
WW	= Production Week (Two Digits)
▪	= Pb−Free Package

*Pb−Free indicator, “G” or microdot “▪”, may or may not be present.



x	= P (CAT)
6243	= Device Code
y	= Output Voltage W = Adjustable
G	= Pb−Free Package
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week

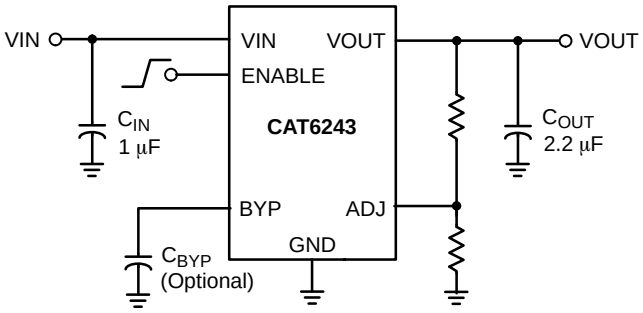


Figure 1. Application Schematic

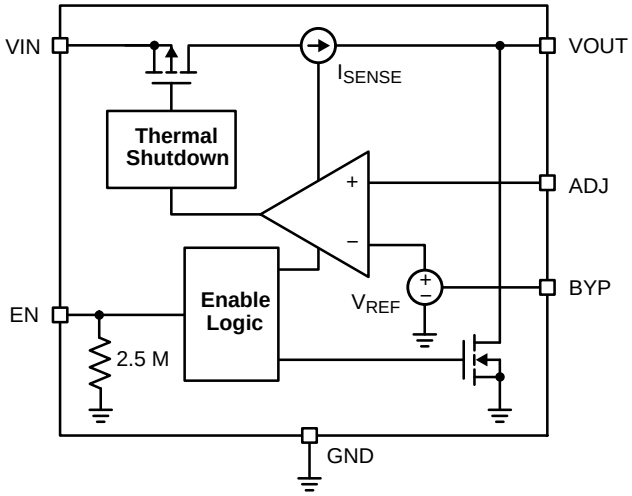


Figure 2. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin # WDFN−6	Pin # DPAK−5−5	Pin Name	Description
1	5	EN	The Enable Input. An active HIGH input, turning ON the LDO. This input should be tied to V_{IN} if the LDO is not intended to be shut off during normal operation. A pull−down 2.5 MΩ resistor maintains the circuit in the OFF state if the pin is left open.
2, PAD	3, TAB	GND	Power Supply Ground; Device Substrate. The center pad is internally connected to Ground and as such can cause short circuits to signal traces running beneath the IC. This pad is intended for heat sinking the IC to the PCB and is typically connected to the PCB ground plane.
3	NC	BYP	Bypass input. Placing a capacitor of 100 pF to 470 pF between BYP and ground reduces noise on V_{OUT}. This capacitor is optional and it increases the turn−on time.
4	2	V_{OUT}	Regulated Output Voltage. A protection block eliminates any current flow from output to input if $V_{OUT} > V_{IN}$.
5	1	ADJ	Output Voltage Adjust Input. This input ties to the common point of a resistor divider which determines the regulator's output voltage. See Applications section for details on selecting resistor values.
6	4	V_{IN}	Positive Power Supply Input. Supplies power for V_{OUT} as well as the regulator's internal circuitry.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range (Note 1)	V_{IN}	−0.3 to 6.0	V
Output Voltage Range	V_{OUT}	−0.3 to 6.0	V
Enable Input Range	EN	−0.3 to 5.5 V or (V_{IN} + 0.3), whichever is lower	V
Adjust Input Range	ADJ	−0.3 to 5.5 V	V
Bypass Input Range	BYP	−0.3 to 5.5 V or (V_{IN} + 0.3), whichever is lower	V
Power Dissipation	PD	Internally Limited	mW
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2	kV
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating range.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, WDFN6, 3x3 mm			°C/W
Thermal Resistance, Junction−to−Air: 1 in^2/1 oz. copper (Note 4)	$R_{\theta JA}$	55	
Thermal Reference, Junction−to−Case (Note 4)	$R_{\psi JL}$	10	
Thermal Characteristics, DPAK−5			°C/W
Thermal Resistance, Junction−to−Air: 1 in^2/1 oz. copper (Note 4)	$R_{\theta JA}$	60	
Thermal Reference, Junction−to−Tab (Note 4)	$R_{\psi JT}$	4.3	

4. Values based on copper area of 650 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

Table 4. OPERATING RANGES (Note 5)

Rating		Symbol	Min	Max	Unit
Input Voltage (Note 6)	CAT6243−ADJ CAT6243DC	V_{IN}	1.8 1.8	5.0 5.5	V
Output Current		I_{OUT}	0.1	1000	mA
Output Voltage		V_{OUT}	0.8	5.0	V
Ambient Temperature		T_A	−40	85	°C

5. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating range.
6. Minimum V_{IN_MIN} = 1.8 V or (V_{OUT} + V_{DO}), whichever is higher.

Table 5. ELECTRICAL CHARACTERISTICS (V_{IN} = (V_{OUT} + 1 V) or V_{IN_MIN}, whichever is higher, C_{IN} = 1 μF, C_{OUT} = 2.2 μF, for typical values T_A = 25°C, for **Bold** values T_A = −40°C to 85°C; unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INPUT / OUTPUT						
V_{OUT}	Output Voltage Range CAT6243−ADJ CAT6243DC		**0.8** **0.8**		**4.5** **5.0**	V
$V_{OUT-ACC}$	Output Voltage Accuracy CAT6243−ADJ CAT6243DC CAT6243DC	Initial accuracy, I_{OUT} = 1 mA	 **−2** −2 **−3**		 **+2** +2 **+3**	%
V_{ADJ}	Voltage at ADJ input		**0.784**	**0.8**	**0.816**	V
TC_{OUT}	Output Voltage Temp. Coefficient CAT6243−ADJ CAT6243DC			 **25** **50**		ppm/°C
I_{OUT}	Output Current		0.0001	1		A
V_{R-LINE}	Line Regulation	V_{IN} = V_{OUT} + 1.0 V to $V_{IN(max)}$, I_{OUT} = 10 mA	−0.2	±0.05	0.2	%/V
		V_{IN} = V_{OUT} + 1.0 V to $V_{IN(max)}$, I_{OUT} = 10 mA	**−0.35**		**0.35**	
V_{R-LOAD}	Load Regulation	I_{OUT} = 100 μA to 1000 mA		1.5	2	%
		I_{OUT} = 100 μA to 1000 mA			**3**	
V_{DO}	V_{OUT} = 1.2 V	I_{OUT} = 300 mA T_A = 25°C			600	mV
	V_{OUT} = 2.5 V CAT6243−ADJ CAT6243DC				110 130	
	V_{OUT} = 3.3 V				85	
	V_{OUT} = 1.2 V CAT6243−ADJ CAT6243DC	I_{OUT} = 1 A T_A = 25°C			625 650	
	V_{OUT} = 2.5 V CAT6243−ADJ CAT6243DC				350 400	
	V_{OUT} = 3.3 V				275	
I_{ADJ}	ADJ Input Current				100	nA
I_{GND}	Ground Current	I_{OUT} = 0 μA		70		μA
		I_{OUT} = 0 μA			**100**	
		I_{OUT} = 1000 mA		140	200	
		I_{OUT} = 1000 mA			**250**	
I_{GND-SD}	Shutdown Ground Current CAT6243−ADJ CAT6243DC	V_{EN} < 0.4 V			 **2** **5**	μA
ISC	Output short circuit current limit	V_{OUT} = 0 V		900		mA
PSRR AND NOISE						
PSRR	Power Supply Rejection Ratio CAT6243	f = 1 kHz, BYP = 470 pF, I_{OUT} = 10 mA		54		dB
		f = 20 kHz, BYP = 470 pF, I_{OUT} = 10 mA		42		
e_N	Output Noise Voltage for 1.8 V output	BW = 10 Hz to 100 kHz BYP = 470 pF, I_{OUT} = 10 mA		45		μVrms
UVLO, R_{OUT} AND ESR						
V_{UVLO}	Under voltage lockout threshold			1.65	**1.75**	V
R_{OUT-SH}	ON resistance of Discharge Transistor			150		Ω
ESR	C_{OUT} equivalent series resistance		5		500	mΩ

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

Table 5. ELECTRICAL CHARACTERISTICS (V_{IN} = (V_{OUT} + 1 V) or V_{IN_MIN}, whichever is higher, C_{IN} = 1 μF, C_{OUT} = 2.2 μF, for typical values T_A = 25°C, for **Bold** values T_A = −40°C to 85°C; unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ENABLE INPUT						
V_{HI}	Logic High Level	V_{IN} = 1.8 to 5.5 V	**1.6**			V
V_{LO}	Logic Low Level	V_{IN} = 1.8 to 5.5 V			**0.4**	V
I_{EN}	Enable Input Current	V_{EN} = 0.4 V		0.15	**1**	μA
		V_{EN} = V_{IN} = 2.5 V		1	**3**	
R_{EN}	Enable pull−down resistor			2.5		MΩ
TIMING						
T_{ON}	Turn−On Time	C_{BYP} = 0 pF		230		μs
		C_{BYP} = 470 pF		1600		
THERMAL PROTECTION						
T_{SD}	Thermal Shutdown			145		°C
T_{HYS}	Thermal Hysteresis			10		°C

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

TYPICAL CHARACTERISTICS

(shown for V_{OUT} = 2.5 V, V_{IN} = 3.5 V, I_{OUT} = 1 mA, C_{IN} = 1 μF, C_{OUT} = 4.7 μF, C_{BYP} = 0, and T_A = 25°C unless otherwise specified.)

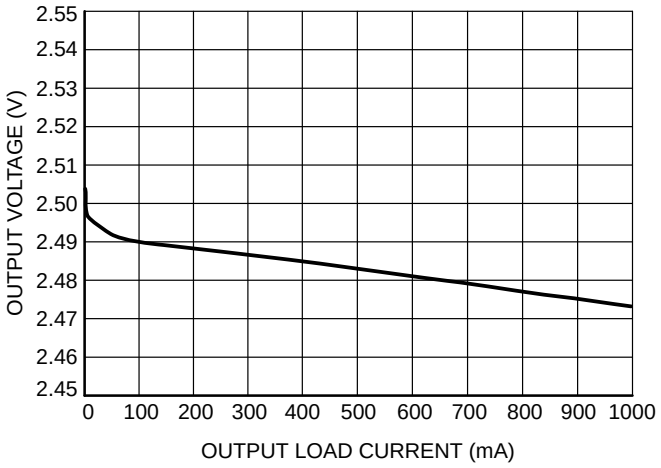


Figure 3. Output Voltage vs. Load Current

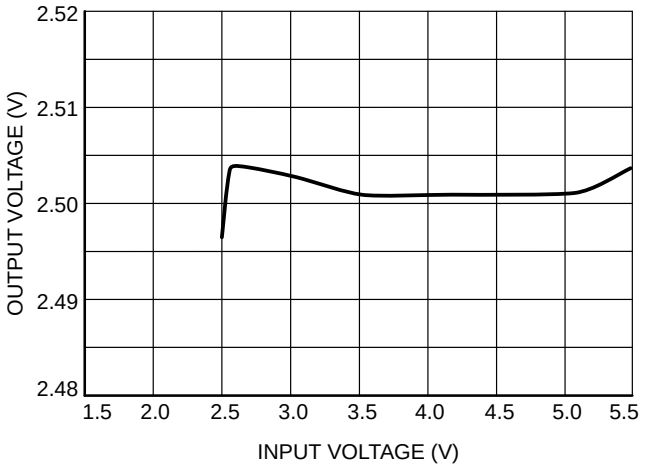


Figure 4. Output Voltage vs. Input Voltage

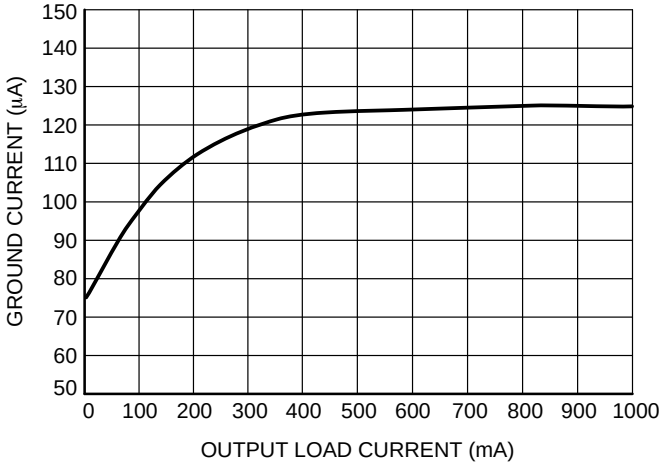


Figure 5. Ground Current vs. Load Current

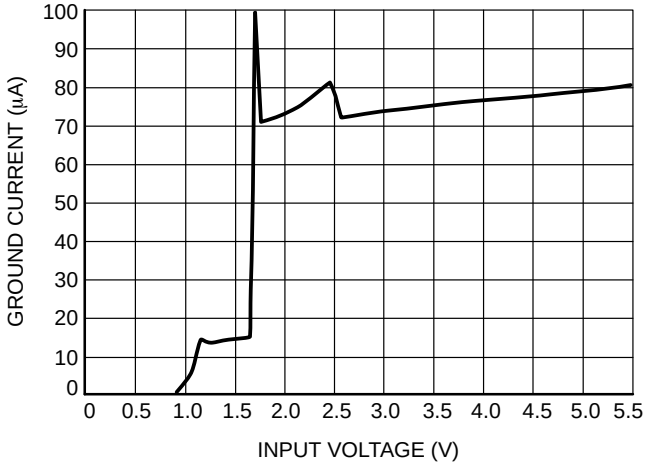


Figure 6. Ground Current vs. Input Voltage

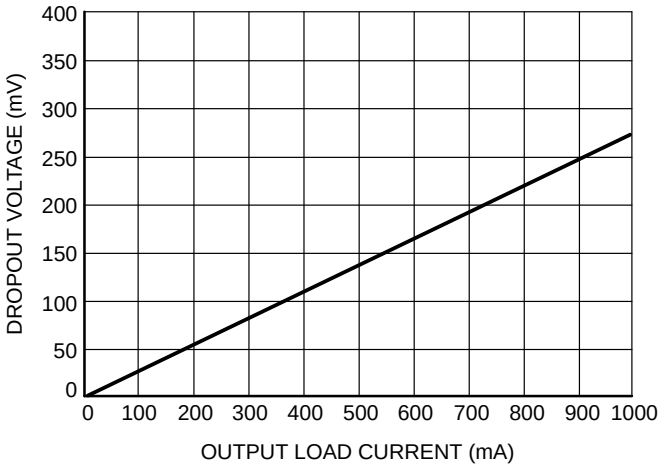


Figure 7. Dropout Voltage vs. Load Current

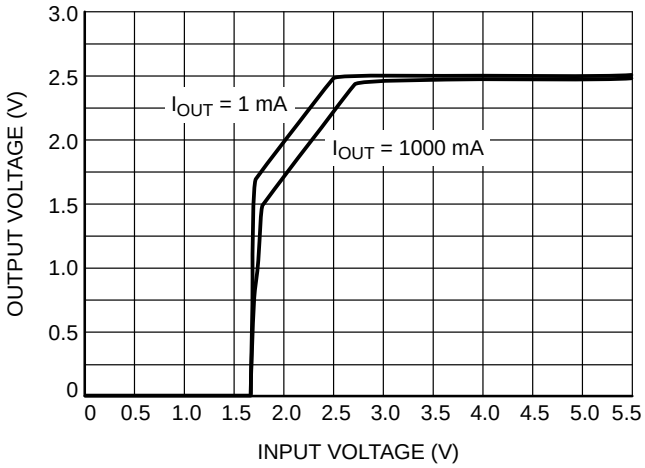


Figure 8. Dropout Characteristics

TYPICAL CHARACTERISTICS

(shown for V_{OUT} = 2.5 V, V_{IN} = 3.5 V, I_{OUT} = 1 mA, C_{IN} = 1 μF, C_{OUT} = 4.7 μF, C_{BYP} = 0, and T_A = 25°C unless otherwise specified.)

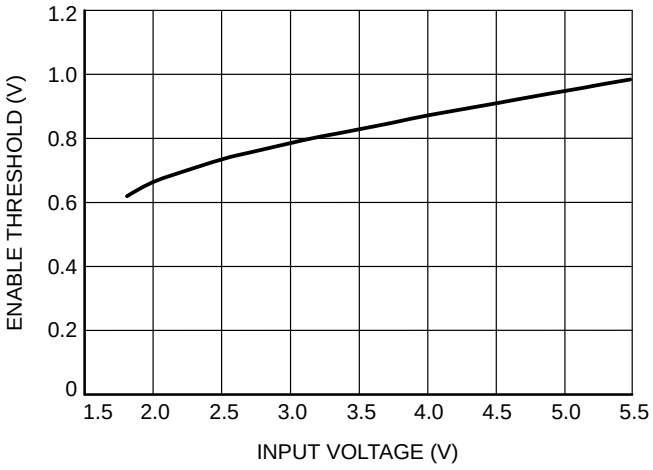


Figure 9. Rising Enable Threshold vs. Supply Voltage

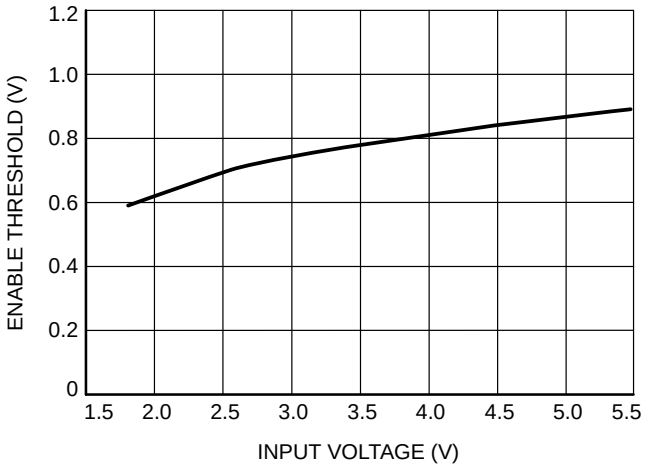


Figure 10. Falling Enable Threshold vs. Supply Voltage

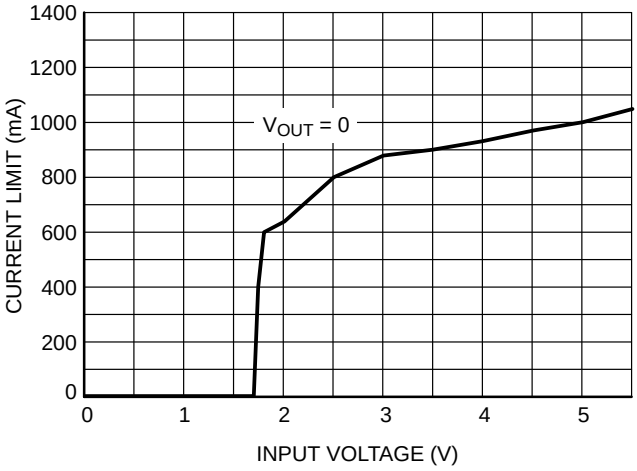


Figure 11. Current Limit on Output vs. Supply Voltage

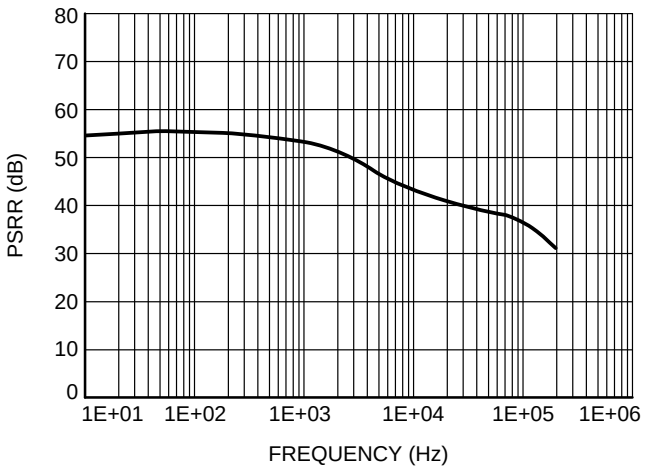


Figure 12. PSRR @ 10 mA

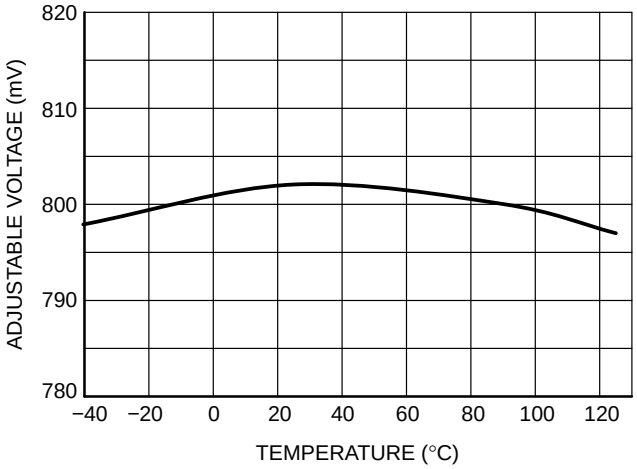


Figure 13. Adjustable Voltage vs. Temperature

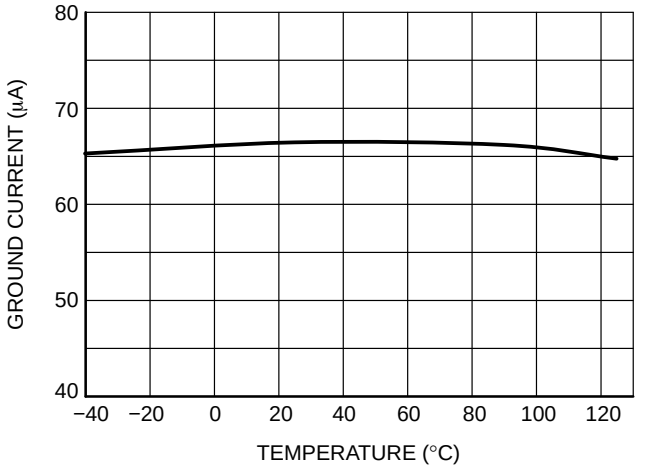


Figure 14. Ground Current vs. Temperature

TRANSIENT CHARACTERISTICS

(shown for V_{OUT} = 2.0 V, V_{IN} = 3.0 V, I_{OUT} = 1 mA, C_{IN} = 1 μF, C_{OUT} = 4.7 μF, C_{BYP} = 0, and T_A = 25°C unless otherwise specified.)

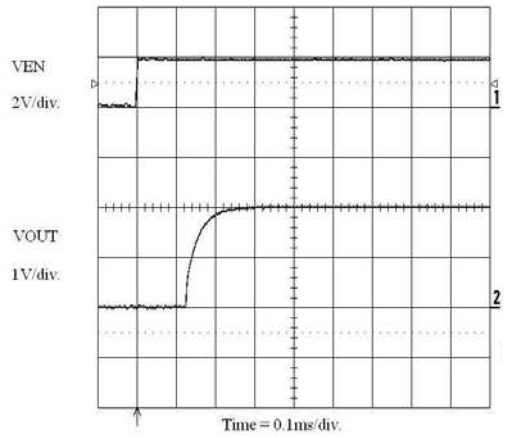


Figure 15. Enable Turn−On (1 mA Load)

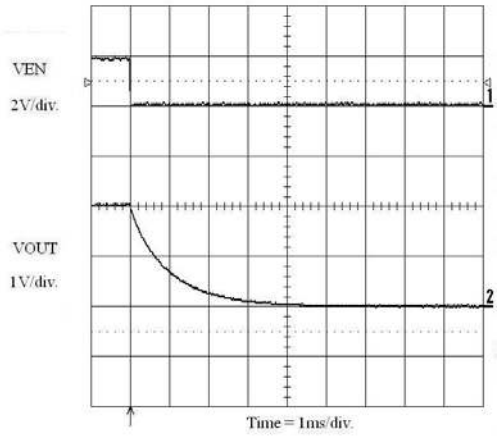


Figure 16. Enable Turn−Off (1 mA Load)

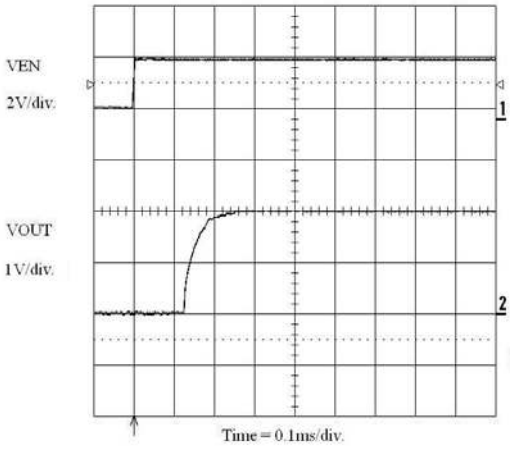


Figure 17. Enable Turn−On (1000 mA Load)

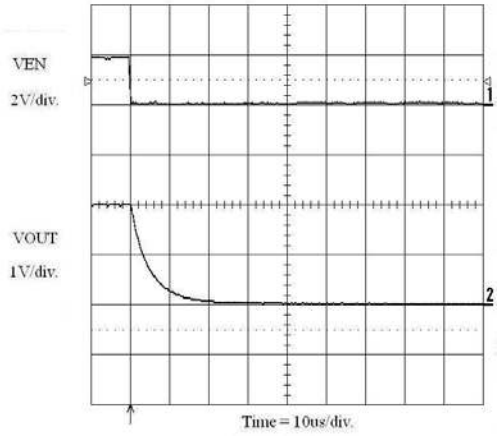


Figure 18. Enable Turn−Off (1000 mA Load)

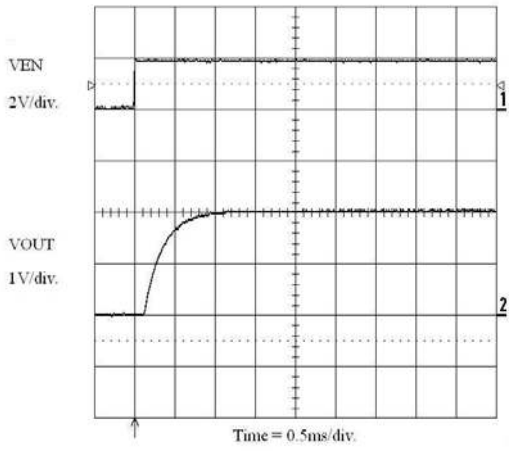


Figure 19. Enable Turn−On (1 mA Load)
CBYP = 470 pF

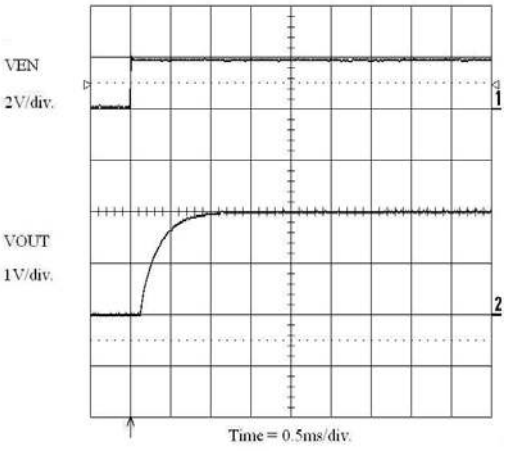


Figure 20. Enable Turn−On (1000 mA Load)
CBYP = 470 pF

TRANSIENT CHARACTERISTICS

(shown for V_{OUT} = 2.0 V, V_{IN} = 3.0 V, I_{OUT} = 1 mA, C_{IN} = 1 μF, C_{OUT} = 4.7 μF, C_{BYP} = 0, and T_A = 25°C unless otherwise specified.)

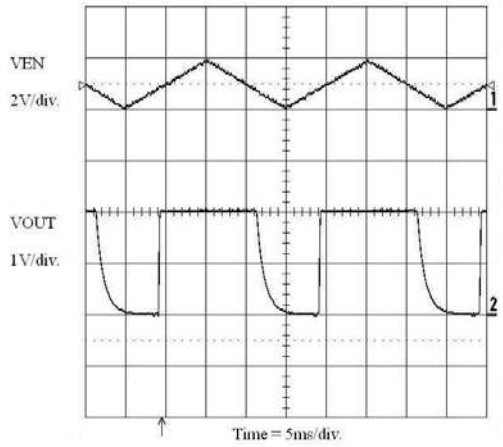


Figure 21. Slow Enable Operation (1 mA Load)

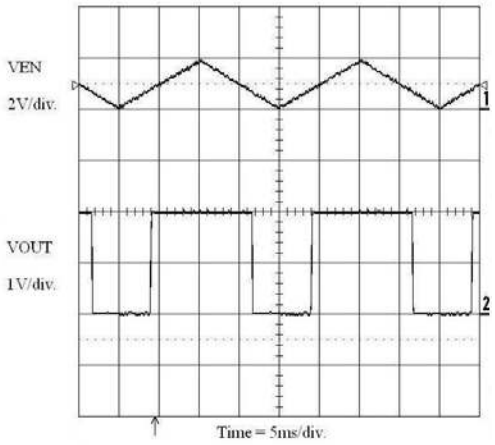


Figure 22. Slow Enable Operation (1000 mA Load)

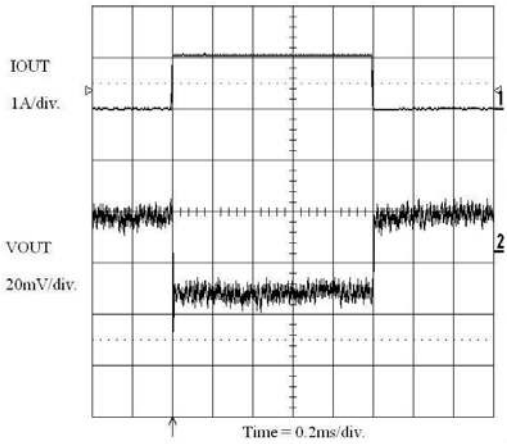


Figure 23. Load Transient Response (1 mA to 1000 mA)

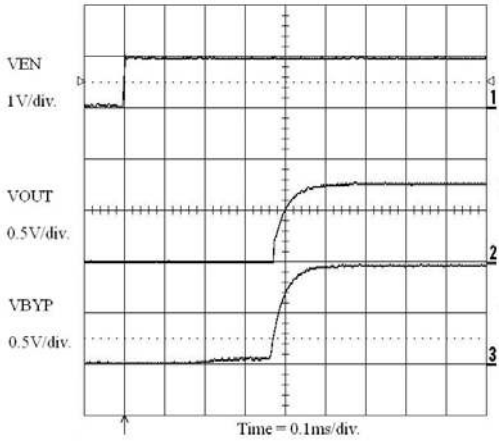


Figure 24. Enable Turn−On (1 mA Load) (V_{OUT} = 0.8 V and V_{IN} = 1.8 V)

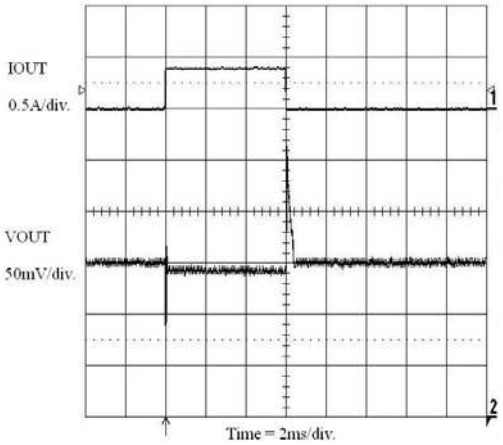


Figure 25. Load Transient Response (1 mA to 400 mA) (V_{OUT} = 0.8 V and V_{IN} = 1.8 V)

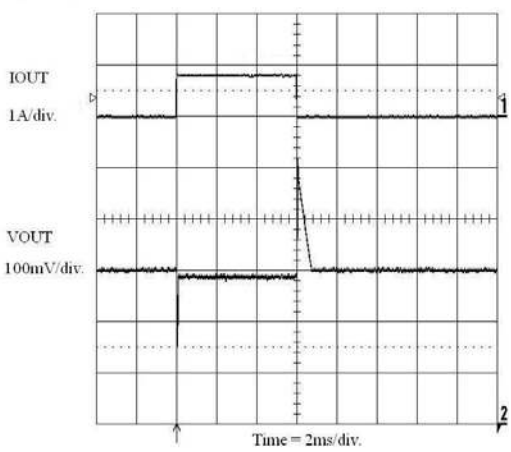


Figure 26. Load Transient Response (1 mA to 800 mA) (V_{OUT} = 0.8 V and V_{IN} = 1.8 V)

PIN FUNCTIONS

V_{IN}

Positive Power Input. Power is supplied to the device through the V_{IN} pin. A bypass capacitor is required on this pin if the device is more than six inches away from the main input filter capacitor. In general it is advisable to include a small bypass capacitor adjacent to the regulator. In battery−powered circuits this is particularly important because the output impedance of a battery rises with frequency, so a bypass capacitor in the range of 1 μF to 10 μF is recommended.

GND

Ground. The negative voltage of the input power source. The center pad on the back of the package is also electrically ground. This pad is used for cooling the device by making connection to the buried ground plane through solder filled vias or by contact with a topside copper surface exposed to free flowing air.

ENABLE

ENABLE is an active high logic input which controls the regulator's the output state. If ENABLE < 0.4 V the regulator is shutdown and V_{OUT} = 0 V. If ENABLE > 1.6 V the regulator is active and supplying power to the load.

If the regulator is intended to operate continuously and won't be shut down from time to time ENABLE should be tied to V_{IN}.

BYP

The Bypass Capacitor input is used to decrease output voltage noise by placing a capacitor between BYP and ground. The recommended range of capacitance is from 100 pF to 470 pF. Values larger than this will provide no additional improvement and will further extend CAT6243's startup time.

A bypass capacitor is not required for operation and BYP may be left open or floating if no capacitor is used but DO NOT ground BYP as this will interfere with the error amplifier's functioning.

ADJ

ADJ = Adjust and is the voltage control input. ADJ connects to the center point of a resistor divider which determines the CAT6243's output voltage. See Applications Section for resistor selection guidelines.

V_{OUT}

V_{OUT} is the regulator's output and supplies power to the load. V_{OUT} can be shut off via the ENABLE input. All CAT6243 members are designed to block reverse current, meaning anytime V_{OUT} becomes greater than V_{IN} the pass FET will be shut off so there is no reverse current flow from output to input. CAT6243 is also equipped with an output discharge transistor that is turned ON anytime ENABLE is at a logic Low. This transistor ensures V_{OUT} discharges to 0 V when the regulator is shutdown. This is especially important when powering digital circuitry because if V_{OUT} fails to reach 0 V their POR (power−ON reset) circuitry may not trigger and scrambled data or unpredictable operations may result.

A minimum output capacitor of 2.2 μF should be placed between V_{OUT} and GND to insure stable operation. Increasing the size of C_{OUT}, up to 22 μF, will improve transient response to large changes in load current.

APPLICATIONS INFORMATION

Input Decoupling (C_{IN})

A ceramic or tantalum 1 μF capacitor is recommended and should be connected close to the CAT6243's package. Higher capacitance and lower ESR will improve the overall line and load transient response.

Output Decoupling (C_{OUT})

The minimum output decoupling value is 2.2 μF and can be augmented to fulfill stringent load transient requirements. The regulator works with ceramic chip capacitors. Larger values, up to 22 μF, improve noise rejection and load regulation transient response. The CAT6243 is a highly stable regulator and performs well over a wide range capacitor Equivalent Series Resistances (ESR).

No−Load Regulation Considerations

The CAT6243 adjustable regulator will operate properly under conditions where the only load current is through the resistor divider that sets the output voltage. However, in the case where the CAT6243 is configured to provide a 0.8 V output, there is no resistor divider and the ADJ pin is connected to V_{OUT}. If the part is enabled under no−load conditions, leakage current through the pass transistor at junction temperatures above 85°C can approach several microamperes, especially as junction temperature approaches 150°C. If this leakage current is not directed into a load, the output voltage will rise above nominal until a load is applied. For this reason it is recommended that a minimum load of 100 μA be present at all times. Normally the voltage setting resistor divider will serve this function but if no divider is used (V_{OUT} = 0.8 V) then an external load of 8 KΩ should be provided.

Output Voltage Adjust

The output voltage can be adjusted from 0.8 V to 5.0 V using resistors between the output and the ADJ input. The output voltage and resistors are chosen using Equation 1 and Equation 2.

$$V_{OUT} = 0.8\left(1 + \frac{R_1}{R_2}\right) + \left(I_{ADJ} \times R_1\right) \quad \text{(eq. 1)}$$

$$R_2 \cong \frac{0.8\ V}{I_{DIV}} \quad \text{(eq. 2)}$$

$$R_1 \cong R_2\left(\frac{V_{OUT}}{0.8\ V} - 1\right) \quad \text{(eq. 3)}$$

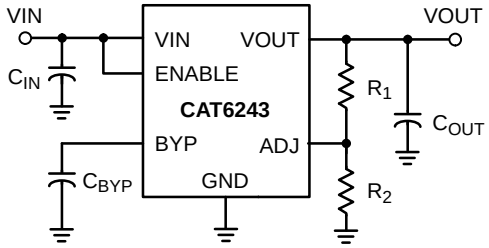


Figure 27. Adjustable Output Resistor Divider

Input bias current, I_{ADJ}, for all practical designs can be ignored (I_{ADJ} = 0). Considering that the lowest recommended I_{OUT} value is 100 μA, then, when there is no load on V_{OUT}, I_{DIV} must be 100 μA to keep CAT6243 in regulation. This then sets R2's value using Equation 2 to 8 KΩ, which minimizes output noise. Use Equation 3 to find the required value for R1. If needed, lower values for I_{DIV} can be considered, but not lower than 10 μA. The price will be worse values for both load regulation and TC_{OUT}.

Thermal Considerations

As power in the CAT6243 increases, it may become necessary to provide thermal relief. The maximum power dissipation supported by this device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the CAT6243 has good thermal conductivity through the PCB, the junction temperature will be relatively low even with high power applications. The maximum dissipation the CAT6243 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \quad \text{(eq. 4)}$$

Since T_J is not recommended to exceed 125°C, then with CAT6243 soldered to 645 mm^2 (1 sq inch), 1 oz copper area, FR4 PCB material can dissipate in excess of 1 W when the ambient temperature (T_A) is 25°C. Note that this assumes the pad in the center of the package is soldered to the dissipating copper foil. See Figure below for $R_{\theta JA}$ versus PCB area for heat dissipating areas smaller than 645 mm^2. Power dissipation can be calculated from the following equations:

$$P_D \approx V_{IN}(I_{GND} + I_{OUT}) + I_{OUT}(V_{IN} - V_{OUT}) \quad \text{(eq. 5)}$$

or

$$V_{IN(MAX)} \approx \frac{P_{D(MAX)} + (V_{OUT} \times I_{OUT})}{I_{OUT} + I_{GND}} \quad \text{(eq. 6)}$$

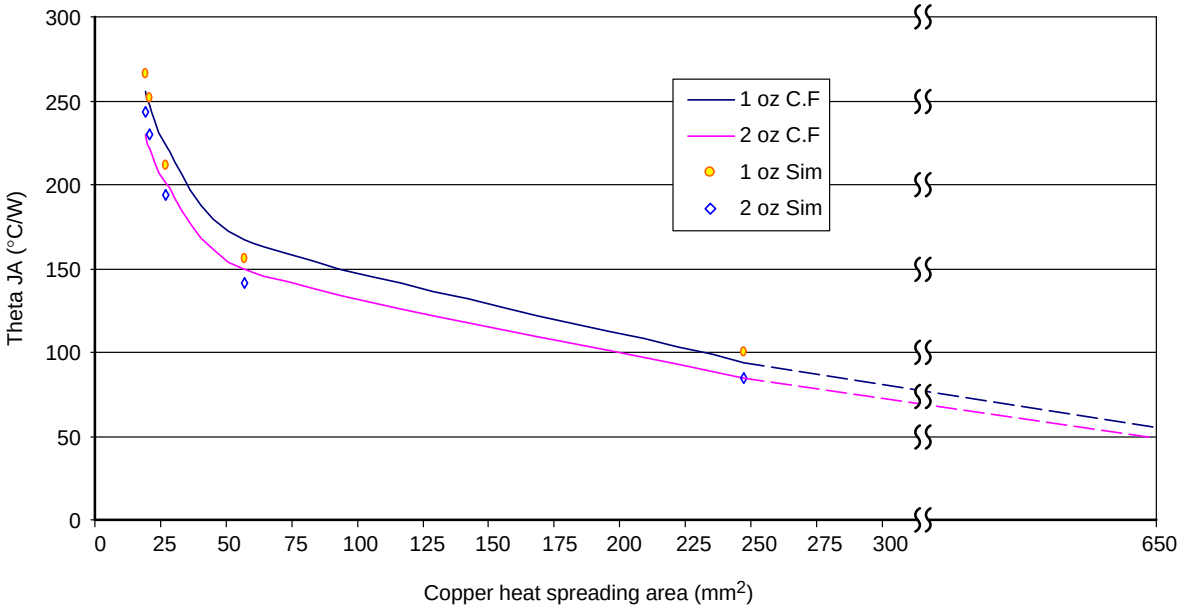


Figure 28. Thermal Resistance vs. PCB Copper Area for 3 mm x 3 mm WDFN Package

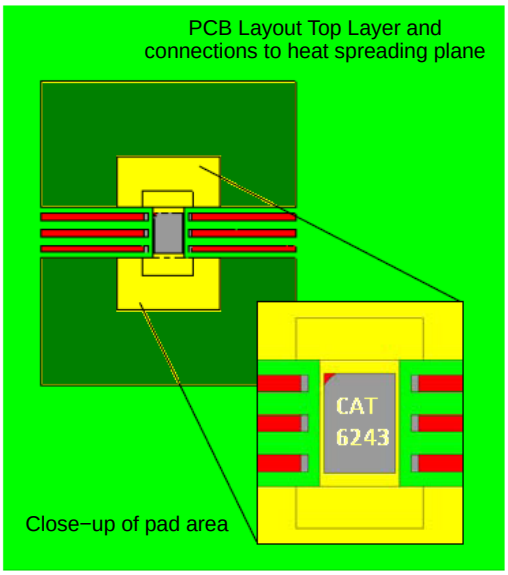


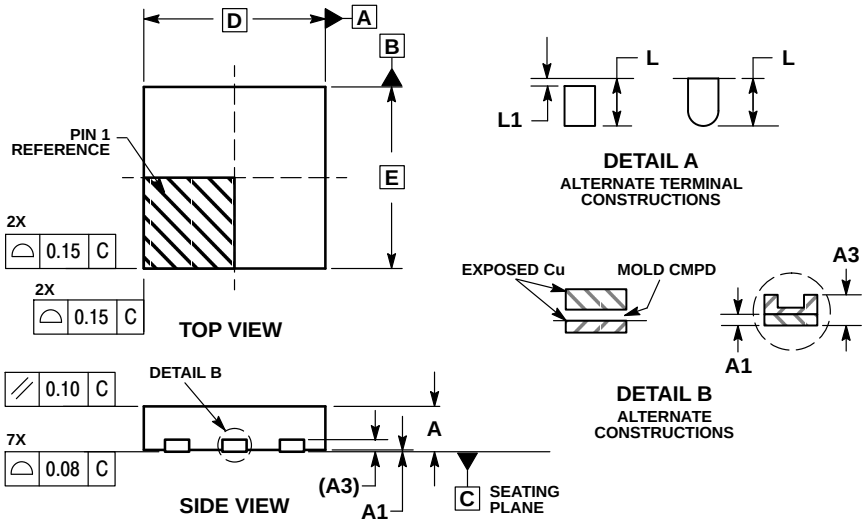
Figure 29. Topside Copper Foil Pattern for Heat Dissipation

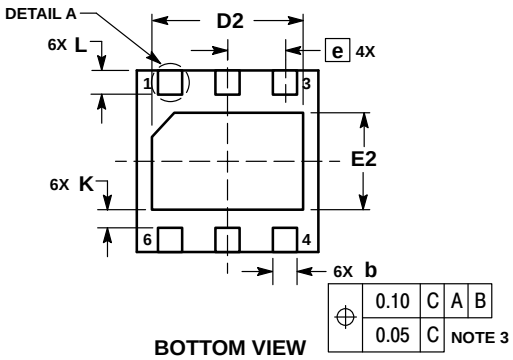
Design Hints

V_{IN} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high due to narrow trace width or long length, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the input and output capacitors, as close as possible to the CAT6243, and keep traces between power source and load as short as possible.

PACKAGE DIMENSIONS

WDFN6 3x3, 0.95P
CASE 511AP
ISSUE O

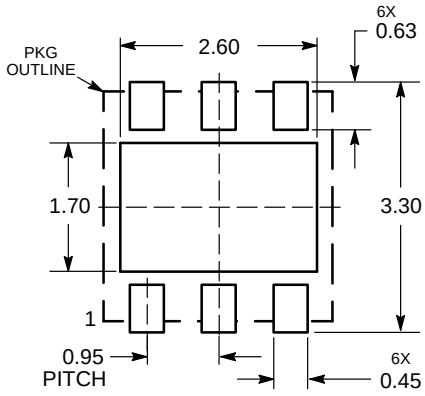




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMESNION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.35	0.45
D	3.00 BSC	
D2	2.40	2.60
E	3.00 BSC	
E2	1.50	1.70
e	0.95 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15

SOLDERING FOOTPRINT*

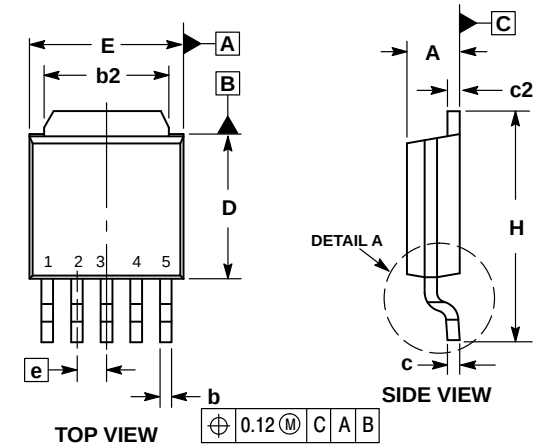


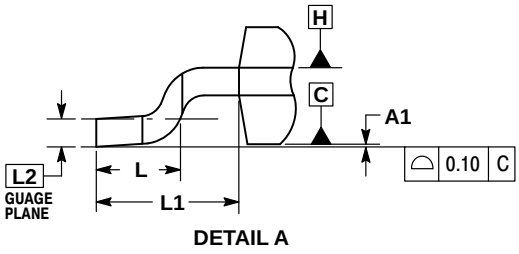
DIMENSIONS: MILLIMETERS

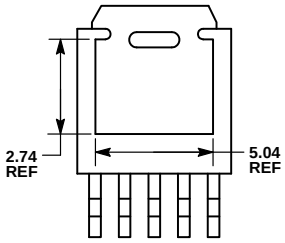
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

DPAK−5 (TO−252, 5 LEAD)
CASE 369AE
ISSUE A



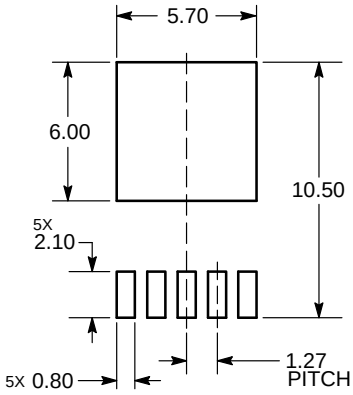




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL, WITHIN DIMENSIONS SHOWN.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

	MILLIMETERS	
DIM	MIN	MAX
A	2.10	2.50
A1	0.00	0.13
b	0.40	0.60
b2	5.14	5.54
c	0.40	0.60
c2	0.40	0.60
D	5.40	6.30
D1	4.80	5.10
E	6.35	6.80
E1	4.75	5.05
e	1.27 BSC	
H	9.50	10.20
L	1.39	1.78
L1	2.50	2.90
L2	0.51 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 6. ORDERING INFORMATION (Notes 8 − 11)

Device	Output Voltage	Package	Shipping
CAT6243−ADJMT5T3	Adjustable	WDFN−6, 3 mm x 3 mm (Pb−Free)	3,000 / Tape & Reel
CAT6243DCADJ−RKG	Adjustable	DPAK 5 5−Lead (Pb−Free)	2,500 / Tape & Reel

8. The standard lead finish is Matte−Tin.
9. For additional package and temperature options, contact your nearest ON Semiconductor Sales office.
10. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
11. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative