SPECIFICATIONS

CUSTOMER : _____

MODEL NO. : GFOC2002C-WG

VERSION : D

DATE : 2023.01.16

CERTIFICATION : ROHS

Customer Sign	Approved By	Prepared By	Prepared By
	GIFAR 2023.01.16 Sidney	GIFAR 2023.01.16 Roger	GIFAR 2023.01.16 Hazel

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Revision Record

Data(y/m/d)	Ver.	Description	page
2011.12.13	A	Specification released	
2013.09.26	B	將 IC pad 的 Pin Definition 改成 FPC 16pin 的. 將 Block Diagram 繪成實際 16pin 的接腳(SPI/I2C)	5、6
2017.08.14	C	修改公司抬頭、格式統一	
2023.01.16	D	1. 更新公司抬頭認證圖示 2. 1.2 Weight 更正 3. 1.5 Block Diagram(MCU Interface 增加表格細部說明) 4. 4.6 Self-Defined CGRAM 更新	4、6、17

Contents

1. Basic Specifications

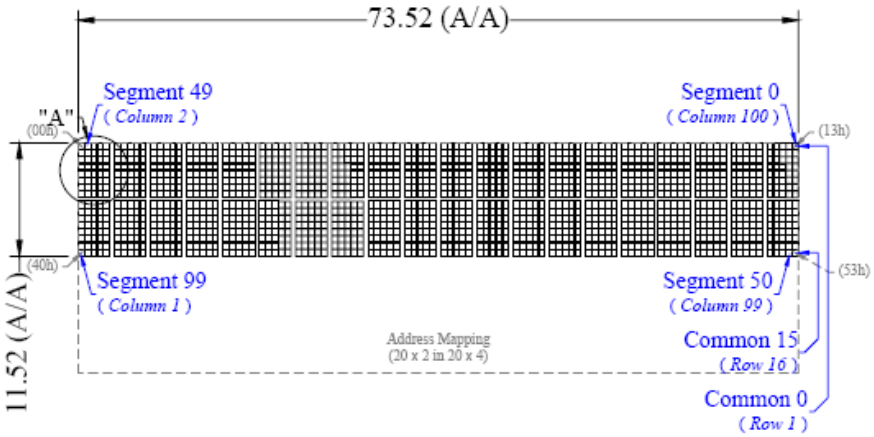
1.1 Display Specifications

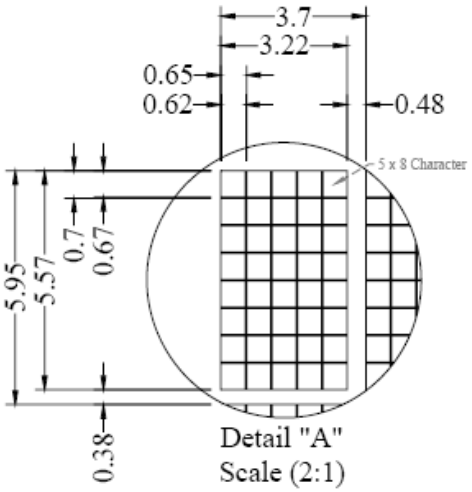
1) Display Mode : Passive Matrix
2) Display Color : Monochrome (White)
3) Drive Duty : 1/16 Duty

1.2 Mechanical Specifications

1) Outline Drawing : According to the annexed outline drawing
2) Number of Characters : 20 Characters (5 x 8) x 2 Lines
3) Module Size : 184.50 x 19.28 x 2.00 (mm)
4) Panel Size : 84.50 x 19.28 x 2.00 (mm) including “Anti-Glare Polarizer”
5) Active Area : 73.52 x 11.52 (mm)
6) Character Pitch : 3.70 x 5.95 (mm)
7) Character Size : 3.22 x 5.57 (mm)
8) Pixel Pitch : 0.65 x 0.70 (mm)
9) Pixel Size : 0.62 x 0.67 (mm)
10) Weight : 7.12 (g)

1.3 Active Area / Address Mapping & Character Construction





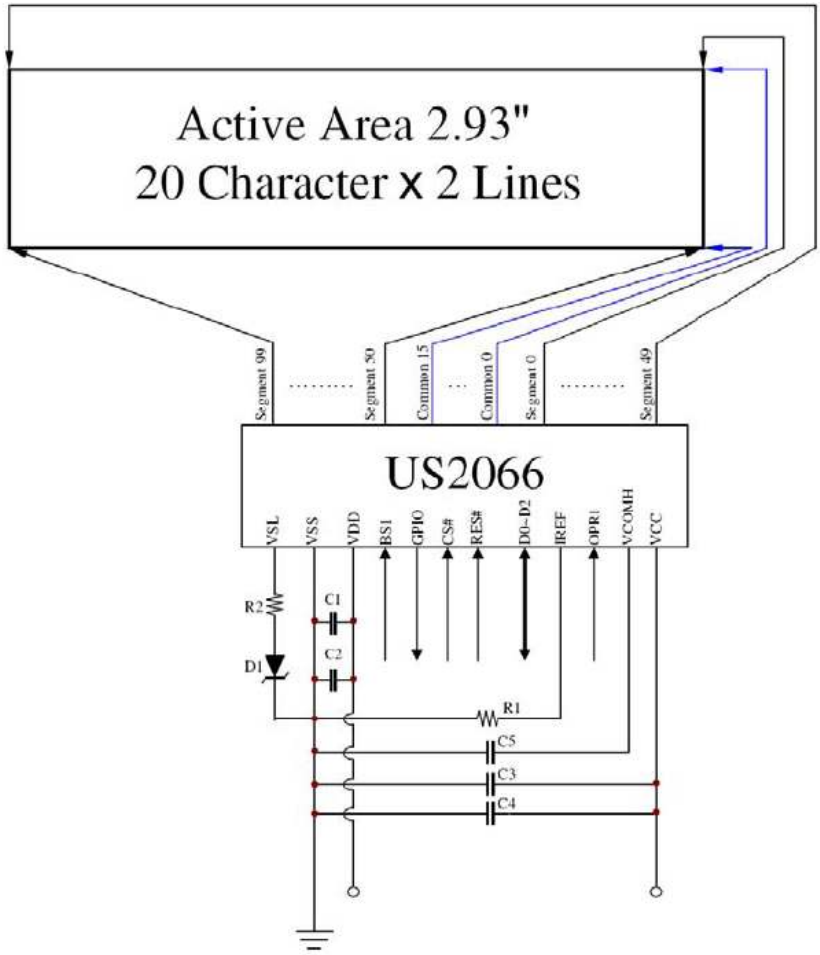
Address Mapping

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Line 1	00h	01h	02h	03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh	10h	11h	12h	13h
Line 2	40h	41h	42h	43h	44h	45h	46h	47h	48h	49h	4Ah	4Bh	4Ch	4Dh	4Eh	4Fh	50h	51h	52h	53h

1.4 Pin Definition

Pin Number	Symbol	I/O	Function
Power Supply			
4	VDD	P	**Power Supply for Logic Circuit** This is a voltage supply pin. It should match with the MCU interface voltage level and must be connected to external source
3	VSS	P	**Ground of OEL System** This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.
15	VCC	P	**Power Supply for OEL Panel** This is the most positive voltage supply pin of the chip. It must be connected to external source.
Driver			
12	IREF	I	**Current Reference for Brightness Adjustment** This pin is segment current reference pin. A resistor should be connected between this pin and V_{SS}. Set the current at 15μA.
14	VCOMH	P	**Voltage Output High Level for COM Signal** This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V_{SS}.
2	VSL	P	**Voltage Output Low Level for SEG Signal** This is segment voltage reference pin. When external V_{SL} is not used, this pin should be left open. When external V_{SL} is used, this pin should connect with resistor and diode to ground.
External IC Communication			
6	GPIO	I/O	**General Purpose Input/Output** This pin could be left open individually or have signal inputted/outputted. It is able to use as the external DC/DC converter circuit enabled/disabled control or other applications.
Configuration			
13	OPR1	I	**Character ROM/RAM Management** These pins are used to manage the character number of character generator. See the following table & Section 4.6: CGROM / CGRAM / OPR1 248 / 8 / 0 256 / 0 / 1 It can still be programmable and defined by extended command.
Interface			
5	BS1	I	**Communicating Protocol Selection** These pins are MCU interface selection input. See the following table: BS1 I^2C / 1 SPI / 0
8	RES#	I	**Power Reset for Controller and Driver** This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.
7	CS#	I	**Chip Select** This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.
9~11	D0~D2	I/O	**Host Data Input/Output Bus** These pins are to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I^2C mode is selected, D2, D1 should be tired together and serve as SDA_{OUT}, SDA_{IN} in application and D0 is the serial clock input, SCL.
Reserve			
1, 16	N.C. (GND)	-	**Reserved Pin (Supporting Pin)** The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.

1.5 Block Diagram

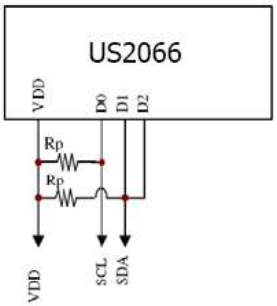


C1, C3 :0.1μF
C2, :4.7μF
C4 :10μF
C5 :4.7μF / 25V Tantalum Capacitor
R1 :470kΩ, R1 = (Voltage at IREF - VSS) / IREF
R2 :50Ω, 1/4W
D1 :≤1.4V, 0.5W

MCU Interface Selection : Base on BS1 connection
Pins connected to MCU interface : CS#, RES#, and D0~D2

BS1	Interface	Data Bus			Control Signal	
		D2	D1	D0	CS#	RES#
1	I^2C	SDA_{OUT}	SDA_{IN}	SCL	**0**	RES#
0	Serial	SOD	SID	SCLK	CS#	RES#

Note:
a. " 0 " is connected to V_{SS}.
b. " 1 " is connected to V_{DD}.
c. D/C# is internal connected to Vss. When I^2C mode is selected, SA0 is equal to "0".
d. When I^2C mode is selected, SDA and SCL should connect the pull up resistor to V_{DD} . Showed as the figure.



2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	VDD	-0.3	6	V	1, 2
Supply Voltage for Display	VCC	0	15	V	1, 2
Operating Temperature	TOP	-40	85	°C	3
Storage Temperature	TSTG	-40	90	°C	3
Life Time (120 cd/m2)		30,000	-	hour	4
Life Time (100 cd/m2)		50,000	-	hour	4

Note 1: All the above voltages are on the basis of “VSS = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. “Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: VCC = 12.0V, Ta = 25°C, 50% Checkerboard.
Software configuration follows Section 4.4 Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note 4	100	120	-	cd/m^2
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.25 0.27	0.29 0.31	0.33 0.35	
Dark Room Contrast	CR		-	>10,000:1	-	
View Angle			-	Free	-	degree

* Optical measurement taken at VDD = 2.8V, VCC = 12.0V.
Software configuration follows Section 4.4 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	VDD		2.4	2.8	3.6	V
Supply Voltage for Display	VCC	Note 5	11.5	12.0	12.5	V
High Level Input	VIH	IOUT = 100μA, 3.3MHz	0.8×VDD	-	VDD	V
Low Level Input	VIL	IOUT = 100μA, 3.3MHz	0	-	0.2×VDD	V
High Level Output	VOH	IOUT = 100μA, 3.3MHz	0.9×VDD	-	VDD	V
Low Level Output	VOL	IOUT = 100μA, 3.3MHz	0	-	0.1×VDD	V
Operating Current for VDD	IDD		-	180	300	μA
Operating Current for VCC	ICC	Note 6	-	15.0	18.0	mA
		Note 7	-	23.7	28.6	mA
		Note 8	-	45.5	55.0	mA
Sleep Mode Current for VDD	IDD, SLEEP		-	1	10	μA
Sleep Mode Current for VCC	ICC, SLEEP		-	2	10	μA

Note 5: Brightness (Lbr) and Supply Voltage for Display (VCC) are subject to the change of the panel characteristics and the customer's request.
Note 6: VDD = 2.8V, VCC = 12.0V, 30% Display Area Turn on.
Note 7: VDD = 2.8V, VCC = 12.0V, 50% Display Area Turn on.
Note 8: VDD = 2.8V, VCC = 12.0V, 100% Display Area Turn on.

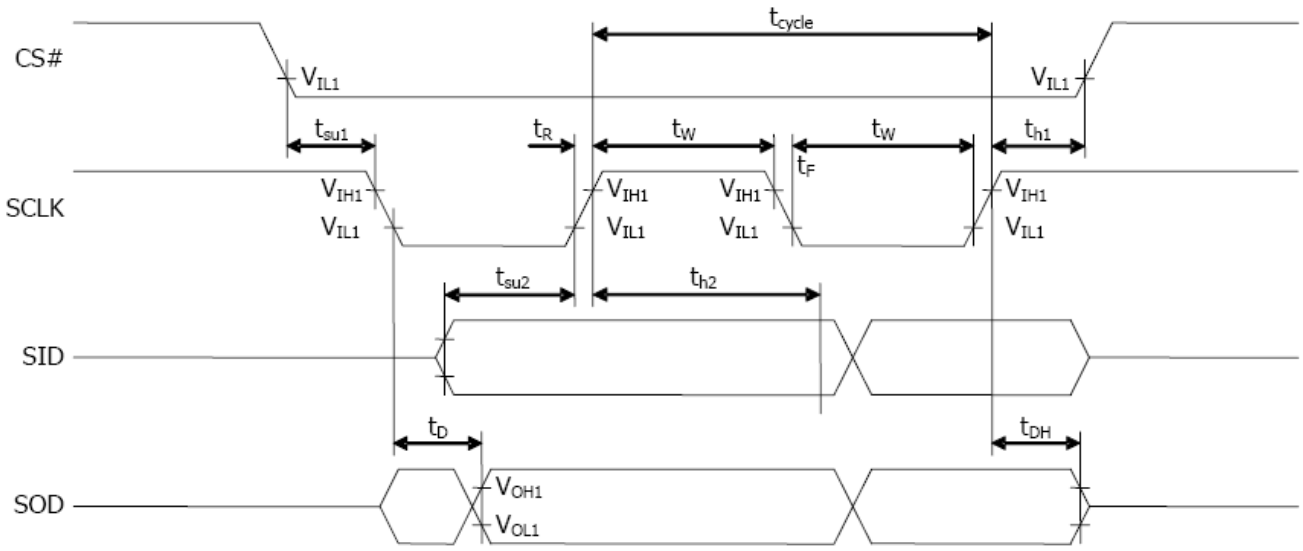
* Software configuration follows Section 4.4 Initialization.

3.3 AC Characteristics

3.3.1 Serial Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
tcycle	Serial Clock Cycle Time	1	20	ns
tsu1	Chip Select Setup Time	60	-	ns
th1	Chip Select Hold Time	20	-	ns
tsu2	Serial Input Data Setup Time	200	-	ns
th2	Serial Input Data Hold Time	20	-	ns
tD	Serial Output Data Delay Time	200	-	ns
tDH	Serial Output Data Hold Time	10	-	ns
tW	Serial Clock Width (Low, High)	400	-	ns
tR	Serial Clock Rise Time	-	15	ns
tF	Serial Clock Fall Time	-	15	ns

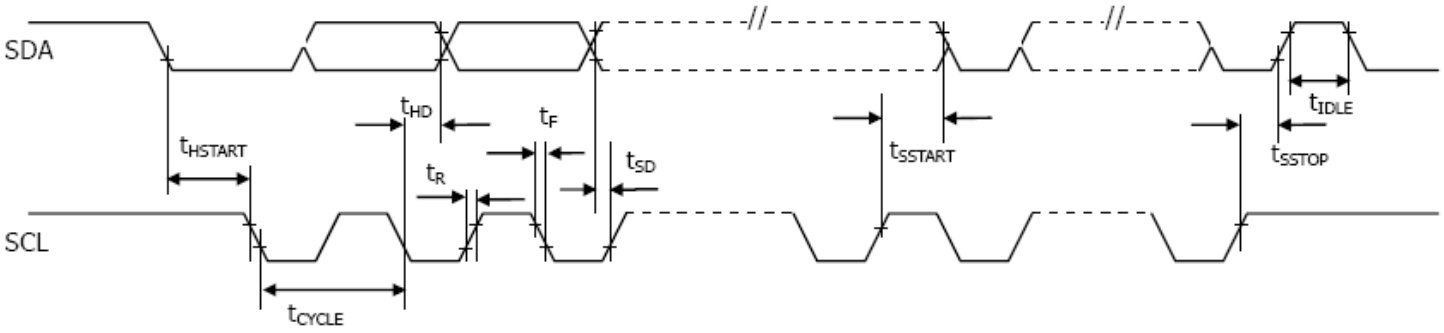
* (VDDIO - VSS = 2.4V to 3.6V , Ta = 25°C)



3.3.2 I²C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	us
t_{HSTART}	Start Condition Hold Time	0.6	-	us
t_{HD}	Data Hold Time (for "SDA$_{OUT}$" Pin)	5	-	ns
	Data Hold Time (for "SDA$_{IN}$" Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	us
t_{SSTOP}	Stop Condition Setup Time	0.6	-	us
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	us

* (VDDIO - VSS = 2.4V to 3.6V / 4.4V to 5.5V, Ta = 25°C)



4. Functional Specification

4.1. Commands

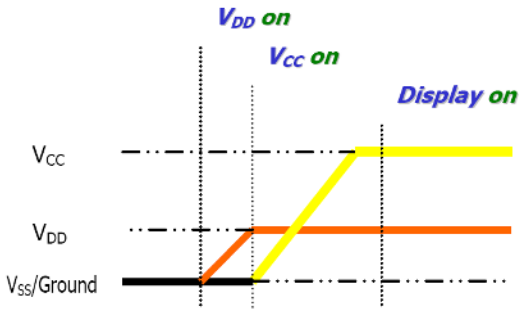
Refer to the Technical Manual for the US2066

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

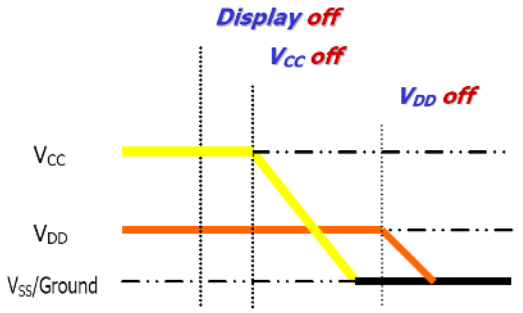
4.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note 9:

1) Since an ESD protection circuit is connected between VDD and VCC inside the driver IC, VCC becomes lower than VDD whenever VDD is ON and VCC is OFF.
2) VCC should be kept float (disable) when it is OFF.
3) Power Pins (VDD, VCC) can never be pulled to ground under any circumstance.
4) VDD should not be power down before VCC power down.

4.3 Reset Circuit

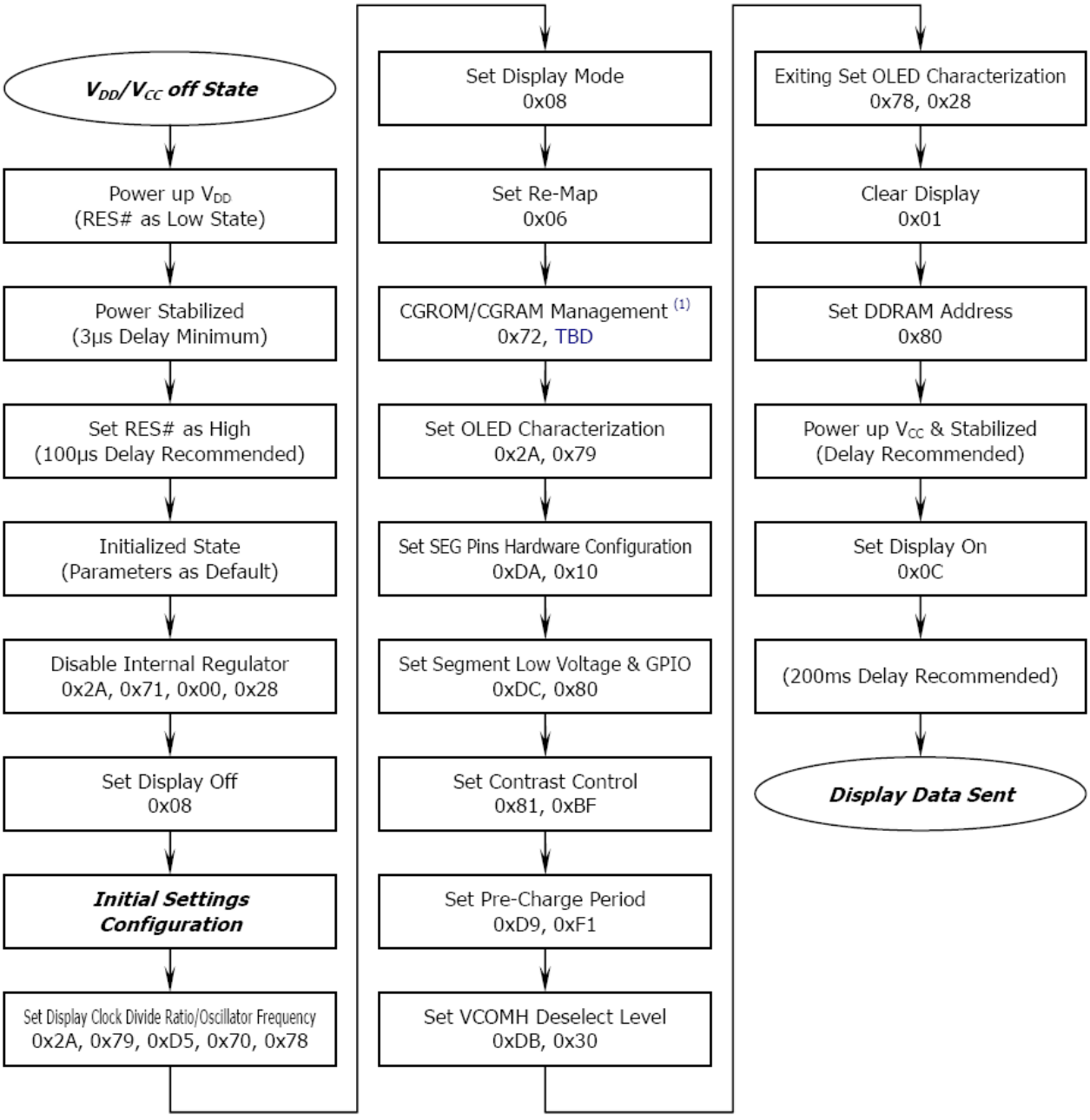
When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 5×8 Character Mode
3. Display start position is set at display RAM address 0
4. CGRAM address counter is set at 0
5. Cursor is OFF
6. Blink is OFF
7. Contrast control register is set at 7Fh
8. OLED command set is disabled

4.4 Actual Application Example

Command usage and explanation of an actual example

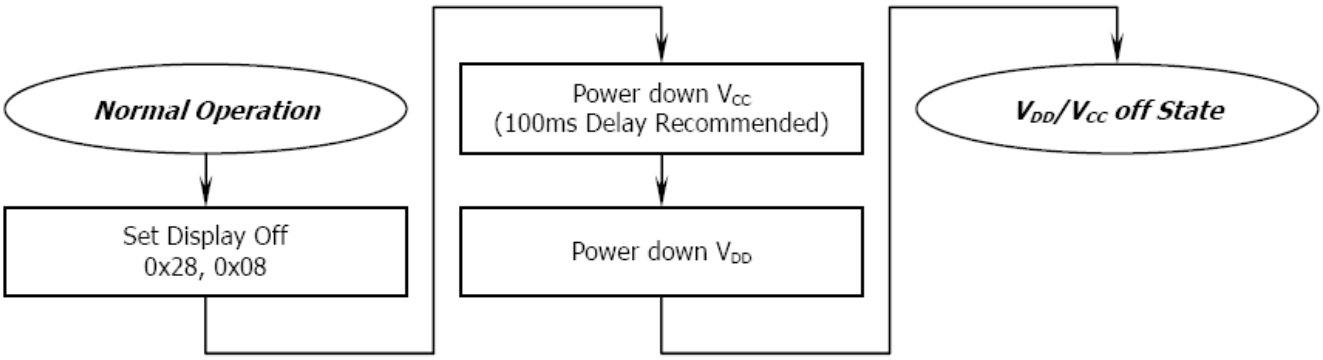
<Power up Sequence>



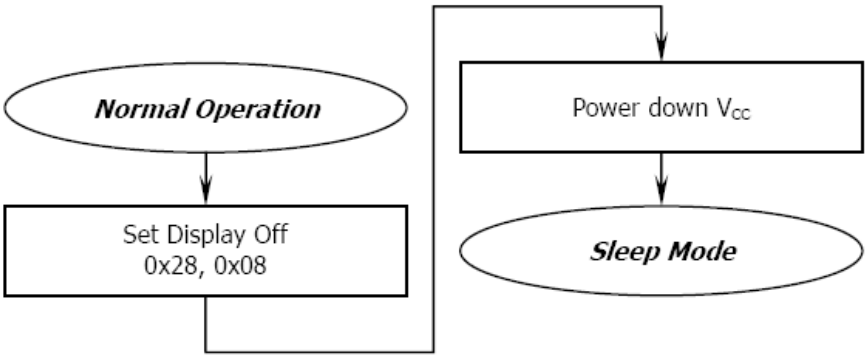
(1) This command could be programmable or defined by pin configuration. The written value of the parameter should depend on the selection from Section 4.5 & 4.6

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

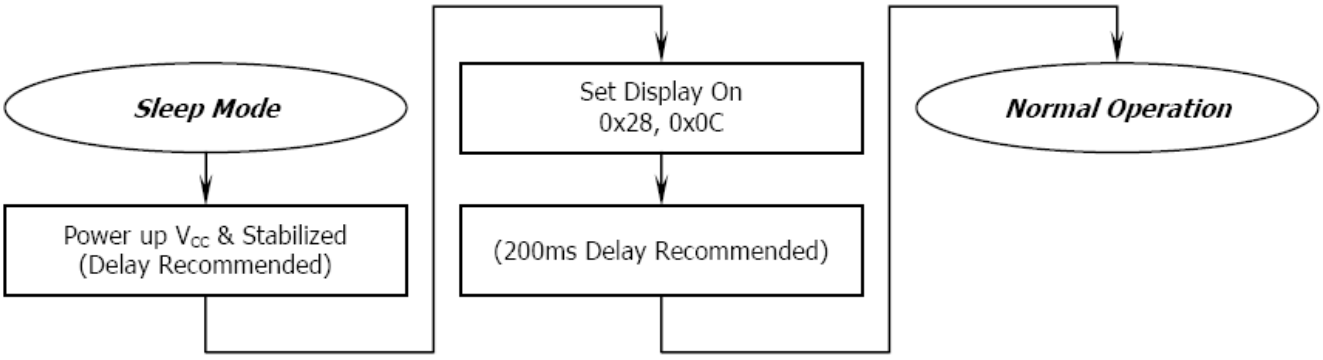
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



4.5 Built-in CGROM (Character Generator ROM)

ROM A (ROM[1:0] = [0:0])

Language: English, Irish, Spanish, Dutch (2), Danish, Norwegian, Swedish, Finnish, Czech (7), Slovene, Hungarian (2), Turkish (1)

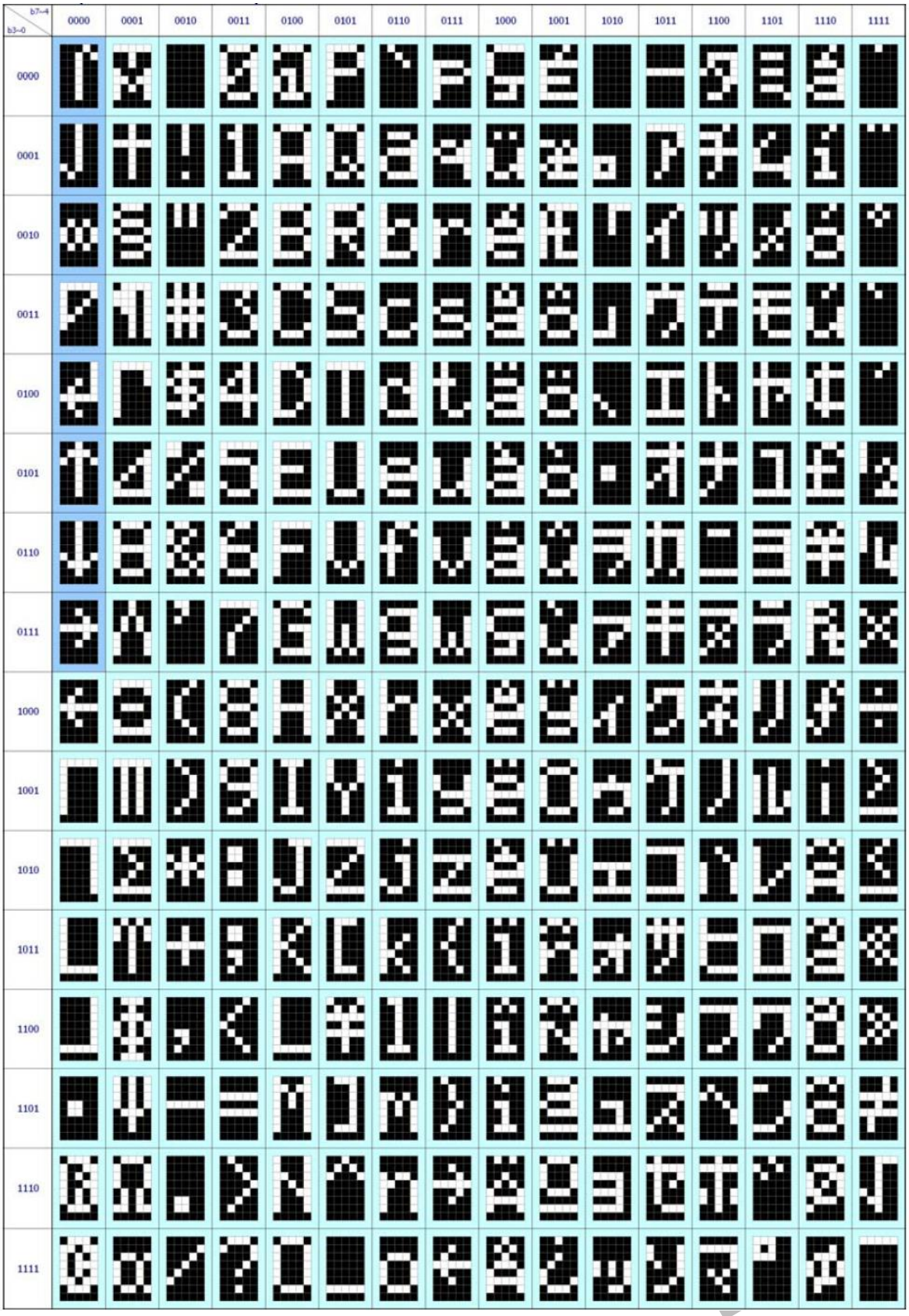
The number in the parentheses is showing how many letters might be needed to build and define additionally at CGRAM. The darker background is showing the maximum addresses (00h~07h) those could be allocated by OPR[1:0] setting.

ROM B (ROM [1:0] = [0:1])

Language: English, Irish, Portuguese, Spanish, French (1), Italian, German, Dutch (2), Icelandic, Danish, Norwegian, Swedish, Polish (8), Czech (8), Hungarian (2), Romanian (5), Turkish, Vietnamese (6), Russian (Small Letters)

The number in the parentheses is showing how many letters might be needed to build and define additionally at CGRAM. The darker background is showing the maximum addresses (00h~07h) those could be allocated by OPR[1:0] setting.

ROM C (ROM[1:0] = [1:0])

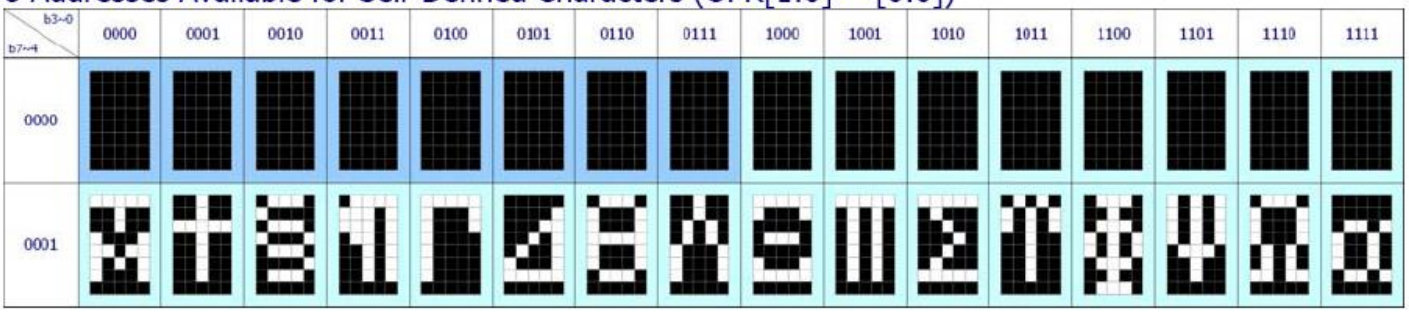


Language: English, Dutch (2), Japanese, Greek (Small Letters)

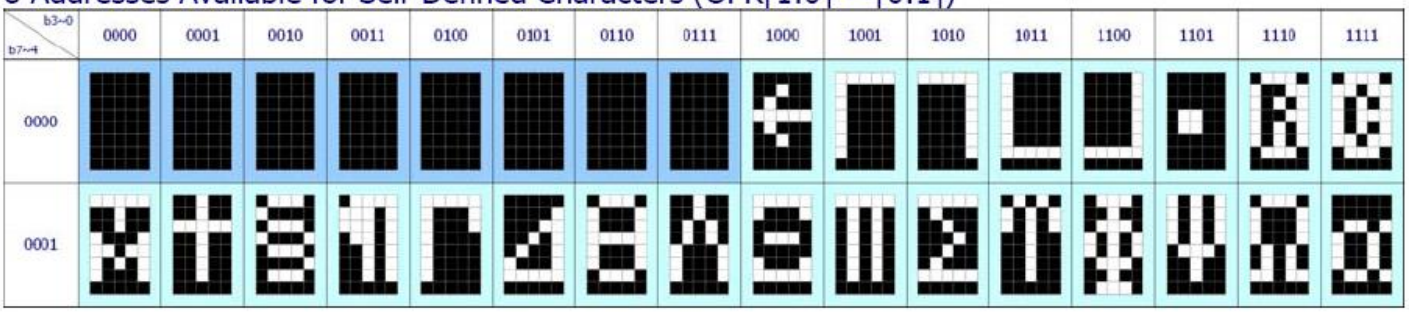
The number in the parentheses is showing how many letters might be needed to build and define additionally at CGRAM. The darker background is showing the maximum addresses (00h~07h) those could be allocated by OPR[1:0] setting.

4.6 Self-Defined CGRAM (Character Generator RAM)

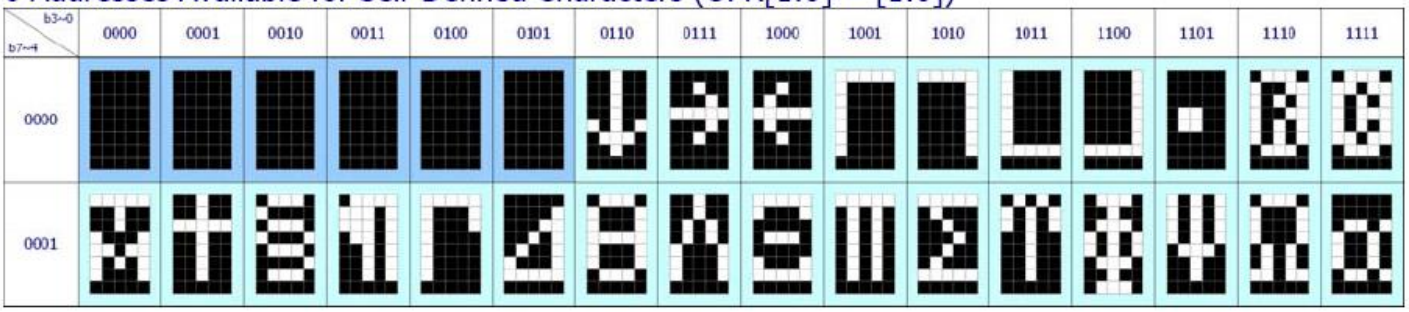
8 Addresses Available for Self-Defined Characters (OPR[1:0] = [0:0])



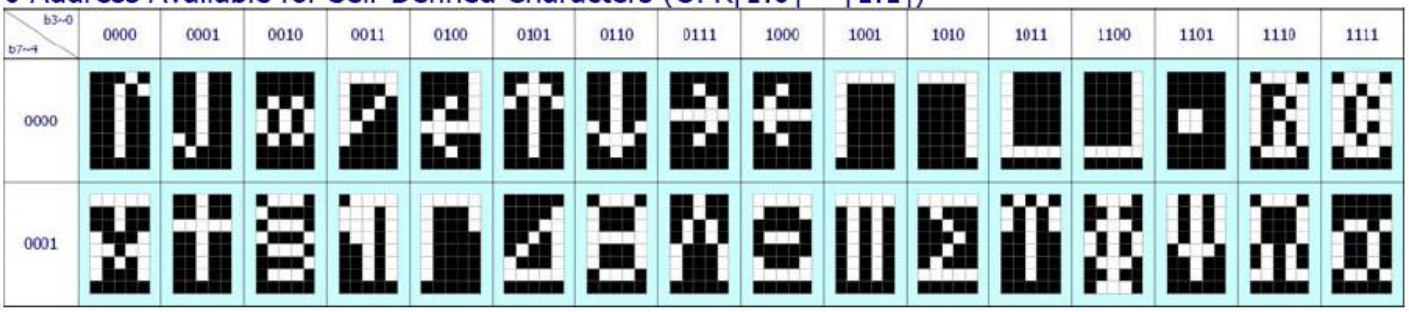
8 Addresses Available for Self-Defined Characters (OPR[1:0] = [0:1])



6 Addresses Available for Self-Defined Characters (OPR[1:0] = [1:0])



0 Address Available for Self-Defined Characters (OPR[1:0] = [1:1])



5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	85°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C,240 hrs	
High Temperature Storage	90°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 240 hrs	
Thermal Shock	-40°C ⇔ 85°C, 100 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

6. Outgoing Quality Control Specifications

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15 %RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50 cm
Distance between the Panel & Eyes of the Inspector:	≥ 30 cm

Finger glove (or finger cover) must be worn by the inspector.

Inspection table or jig must be anti-electrostatic.

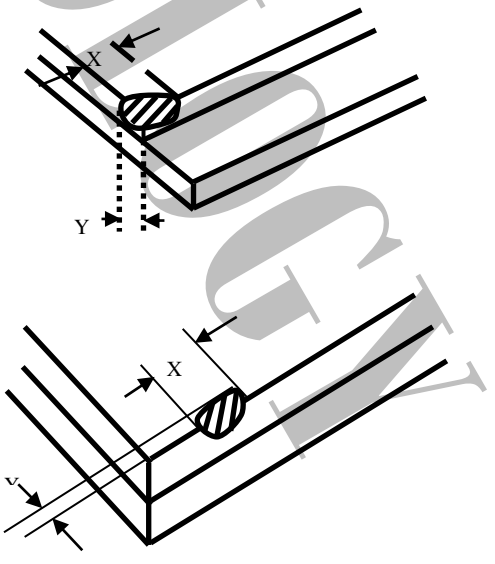
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

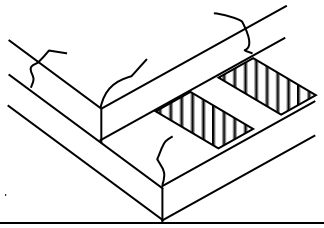
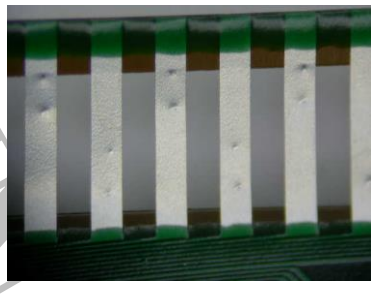
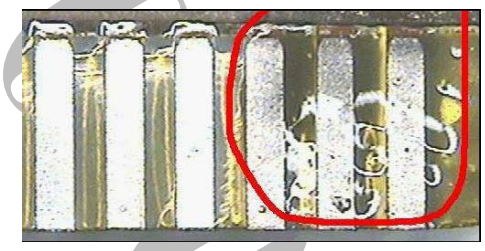
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

6.3.1 Cosmetic Check (Display Off) in Non-Active Area

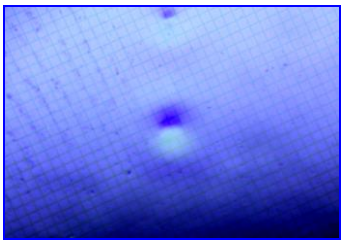
Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Cupper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

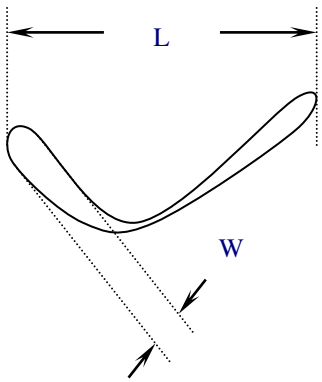
6.3.2 Cosmetic Check (Display Off) in Active Area

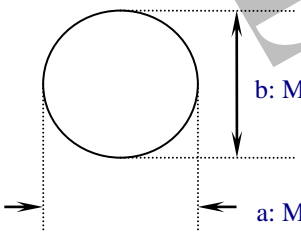
It is recommended to execute in clear room environment (class 10k) if actual in necessary.

Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	$W \le 0.1$ Ignore $W > 0.1, L \le 2$ $n \le 1$ $L > 2$ $n = 0$
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	$\Phi \le 0.1$ Ignore $0.1 < \Phi \le 0.25$ $n \le 1$ $0.25 < \Phi$ $n = 0$
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	$\Phi \le 0.5$ ➔ Ignore if no Influence on Display $0.5 < \Phi$ $n = 0$ 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

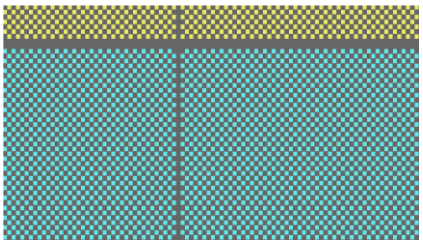
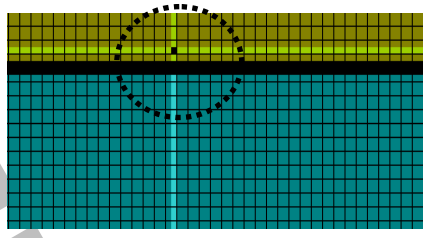
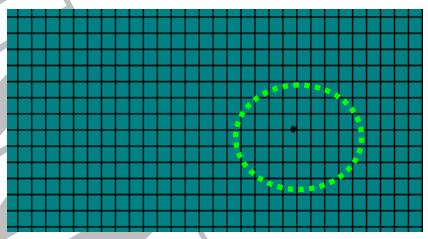
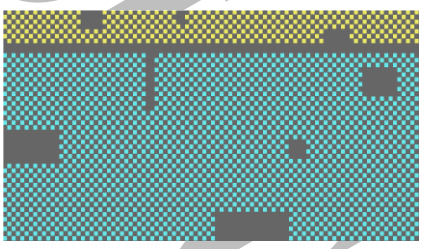
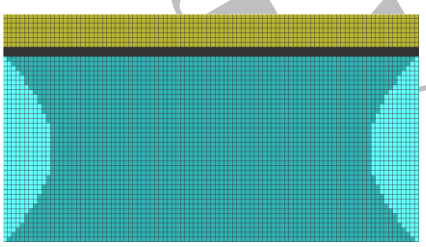
* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): $\Phi = (a + b) / 2$

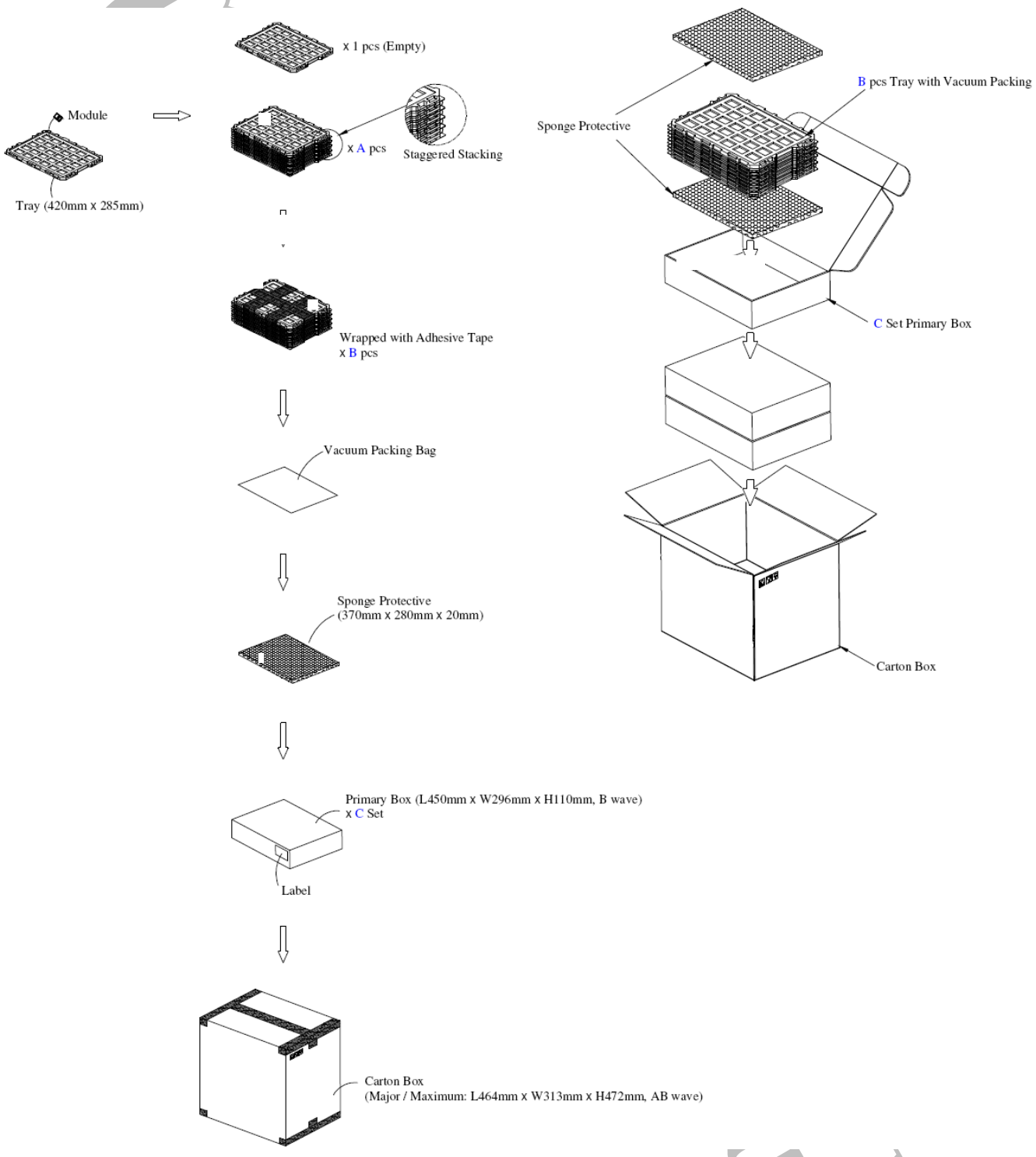




6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

7. Package Specifications



Item		Quantity
Module		280 per Primary Box
Holding Trays	(A)	20 per Primary Box
Total Trays	(B)	21 per Primary Box (Including 1 Empty Tray)
Primary Box	(C)	1~4 per Carton (4 as Major / Maximum)

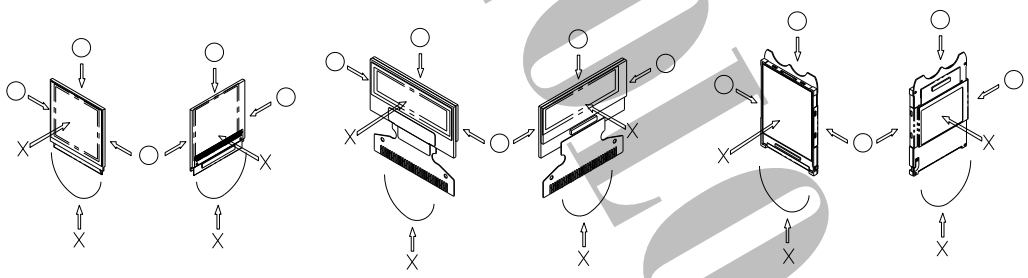
8. Precautions When Using These OEL Display Modules

8.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy. Also, pay attention that the following liquid and solvent may spoil the polarizer:

   * Water
   * Ketone
   * Aromatic Solvents
6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OEL display

module. Be careful since static electricity may be generated when exfoliating the protective film.

11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

8.2 Storage Precautions

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Univision Technology Inc.)

   At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.

2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

8.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: US2066

   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

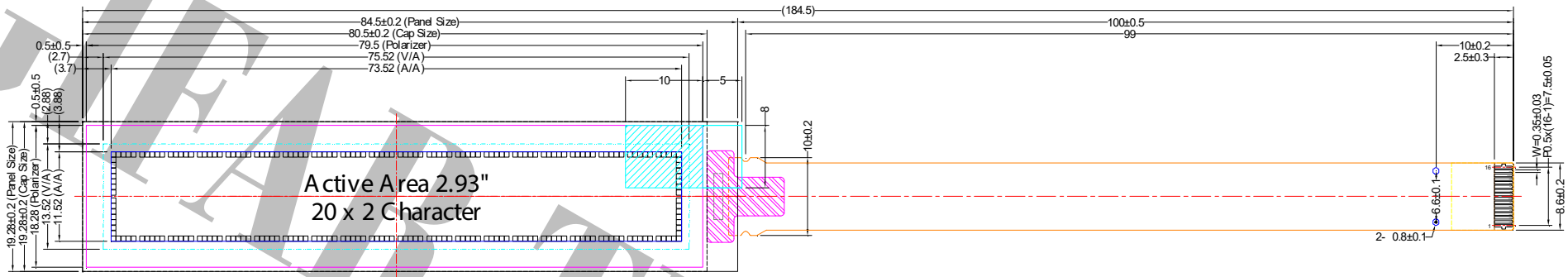
8.4 Precautions when disposing of the OEL display modules

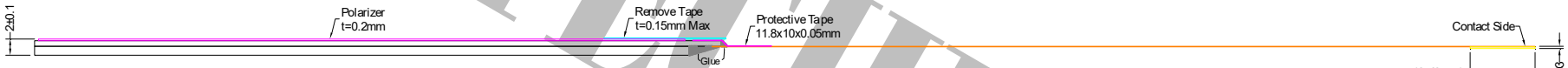
1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

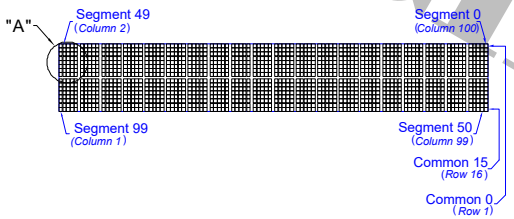
8.5 Other Precautions

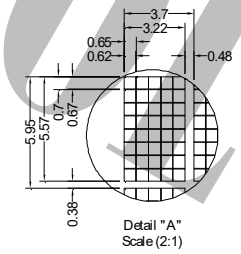
1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
   Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the COF
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

RoHS









Pin	Symbol
1	N.C. (GND)
2	VSL
3	VSS
4	VDD
5	BS1
6	GPIO
7	CS#
8	RES#
9	D0
10	D1
11	D2
12	IREF
13	OPR1
14	VCOMH
15	VCC
16	N.C. (GND)

Notes:

1. Color: White
2. Driver IC: US2066
3. FPC Number: UT-0166-P02
4. Applicable Connector: Superior Tech FPSA-I16T2SX-E
5. Interface: SPI, I2C
6. General Tolerance: ±0.30
7. The total thickness (2.10 Max) is without polarizer protective film & remove tape.
   The actual assembled total thickness with above materials should be 2.35 Max.

日期	版本	修改內容

晶 發 科 技 股 份 有 限 公 司
GI FAR TECHNOLOGY CO., LTD

DATE	2023.01.16	REV	X0		
UNIT : mm SCALE : 1/1 SHEET : 1/1	Product :	GFOC2002C-WG			
	DRAWN :	Hazel	CHECKED :	Sidney	PAGE : 1/1