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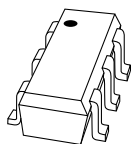
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Kind regards,

Team Nexperia



PMGD780SN

Dual N-channel μ TrenchMOS standard level FET

Rev. 02 — 19 April 2010

Product data sheet

1. Product profile

1.1 General description

Dual N-channel enhancement mode field-effect transistor in a small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package using TrenchMOS technology.

1.2 Features and benefits

- Surface-mounted package
- Standard level threshold voltage
- Low on-state resistance
- Footprint 40 % smaller than SOT23
- Fast switching
- Dual device

1.3 Applications

- Driver circuits
- Switching in portable appliances

1.4 Quick reference data

- $V_{DS} \leq 60$ V
- $I_D \leq 0.49$ A
- $P_{tot} \leq 0.41$ W
- $R_{DS(on)} \leq 920$ m Ω

2. Pinning information

Table 1. Pinning - SOT363 (SC-88), simplified outline and symbol

Pin	Description	Simplified outline	Graphic symbol
1	source1 (S1)	<p>SOT363 (SC-88)</p>	<p>msd901</p>
2	gate1 (G1)		
3	drain2 (D2)		
4	source2 (S2)		
5	gate2 (G2)		
6	drain1 (D1)		

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PMGD780SN	SC-88	plastic surface-mounted package; 6 leads	SOT363

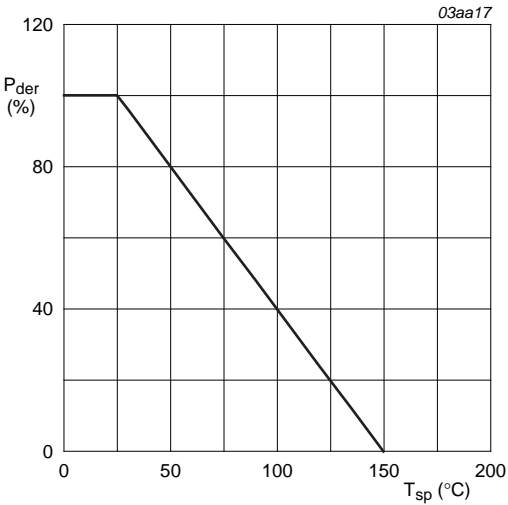
4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

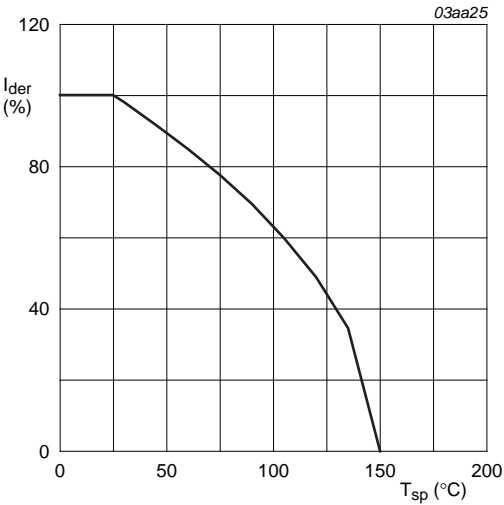
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ }^{\circ}\text{C} \leq T_j \leq 150\text{ }^{\circ}\text{C}$	-	60	V
V_{DGR}	drain-gate voltage	$25\text{ }^{\circ}\text{C} \leq T_j \leq 150\text{ }^{\circ}\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	60	V
V_{GS}	gate-source voltage		-	± 20	V
I_D	drain current	$T_{sp} = 25\text{ }^{\circ}\text{C}$; $V_{GS} = 10\text{ V}$; Figure 2 and 3	[1] -	0.49	A
		$T_{sp} = 100\text{ }^{\circ}\text{C}$; $V_{GS} = 10\text{ V}$; Figure 2	[1] -	0.31	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ }^{\circ}\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	[1] -	0.99	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ }^{\circ}\text{C}$; Figure 1	-	0.41	W
T_{stg}	storage temperature		-55	+150	$^{\circ}\text{C}$
T_j	junction temperature		-55	+150	$^{\circ}\text{C}$
Source-drain diode					
I_S	source current	$T_{sp} = 25\text{ }^{\circ}\text{C}$	[1] -	0.34	A
I_{SM}	peak source current	$T_{sp} = 25\text{ }^{\circ}\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	[1] -	0.69	A

[1] Single device conducting.



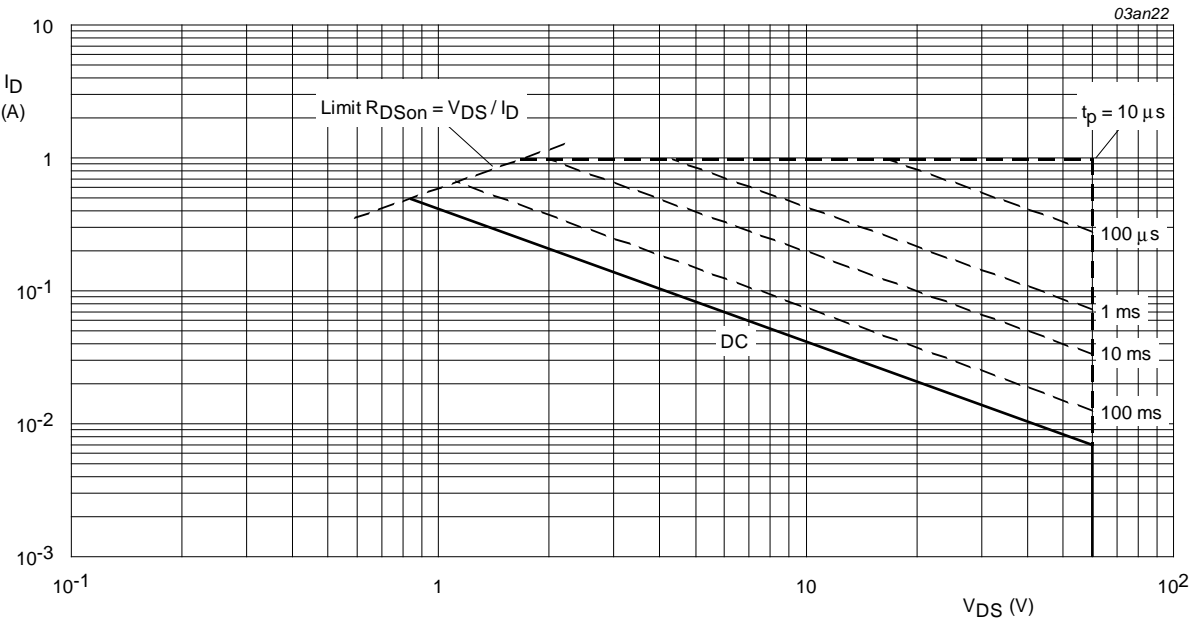
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



T_{sp} = 25 °C; I_{DM} is single pulse; V_{GS} = 10 V

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	300	K/W

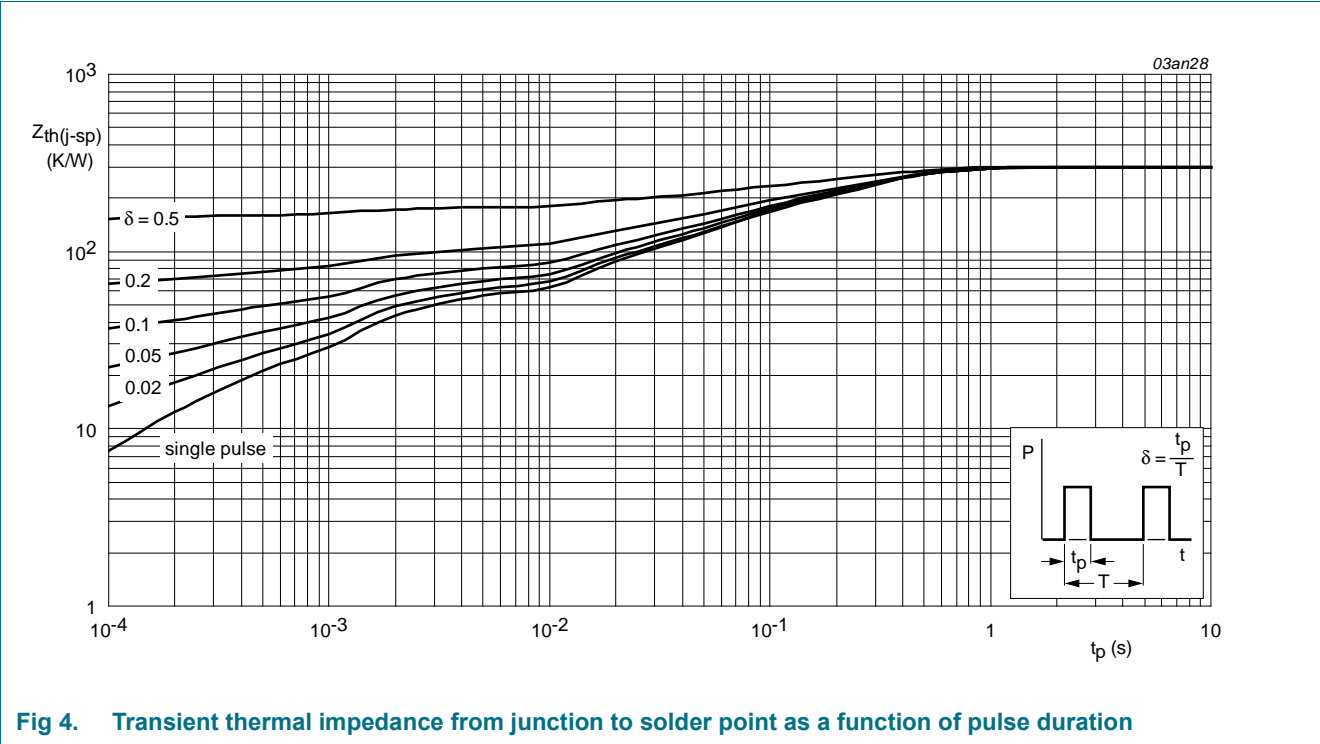


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 5. Characteristics

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V				
		T _j = 25 °C	60	-	-	V
		T _j = −55 °C	55	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 0.25 mA; V _{DS} = V _{GS} ; Figure 9				
		T _j = 25 °C	1	2	2.5	V
		T _j = 150 °C	0.6	–	–	V
		T _j = −55 °C	–	–	3.5	V
I _{DSS}	drain leakage current	V _{DS} = 60 V; V _{GS} = 0 V				
		T _j = 25 °C	-	0.05	1	μA
		T _j = 150 °C	-	-	100	μA
I _{GSS}	gate leakage current	V _{GS} = ±20 V; V _{DS} = 0 V	-	10	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 0.3 A; Figure 7 and 8				
		T _j = 25 °C	-	780	920	mΩ
		T _j = 150 °C	-	1445	1700	mΩ
		V _{GS} = 4.5 V; I _D = 0.075 A; Figure 7 and 8	-	1100	1400	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 1 A; V _{DD} = 30 V; V _{GS} = 10 V; Figure 13	-	1.05	-	nC
Q _{GS}	gate-source charge		-	0.2	-	nC
Q _{GD}	gate-drain charge		-	0.22	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 30 V; f = 1 MHz; Figure 11	-	23	-	pF
C _{oss}	output capacitance		-	5	-	pF
C _{rss}	reverse transfer capacitance		-	3.5	-	pF
t _{d(on)}	turn-on delay time	V _{DD} = 30 V; R _L = 30 Ω; V _{GS} = 10 V; R _G = 6 Ω	-	2	-	ns
t _r	rise time		-	4	-	ns
t _{d(off)}	turn-off delay time		-	5	-	ns
t _f	fall time		-	2.2	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 0.3 A; V _{GS} = 0 V; Figure 12	-	0.83	1.2	V

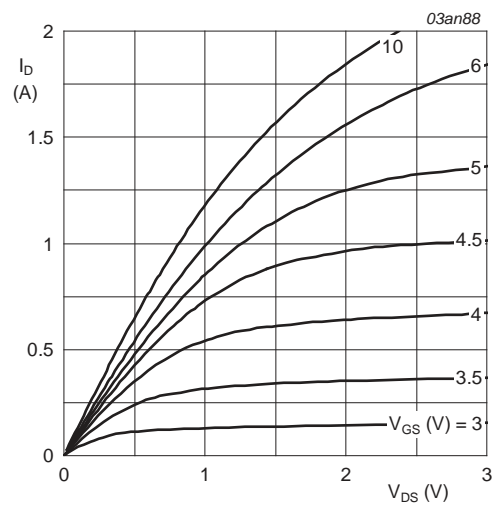


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

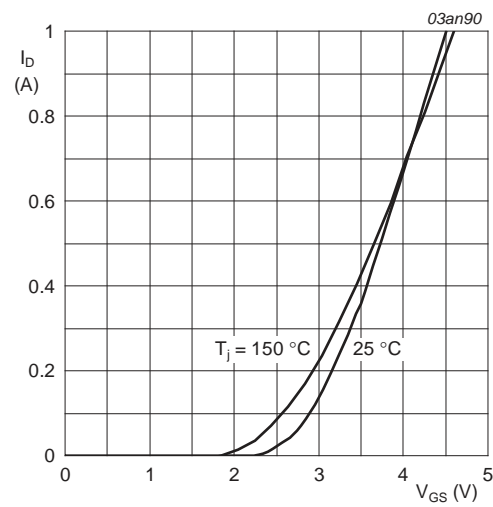


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

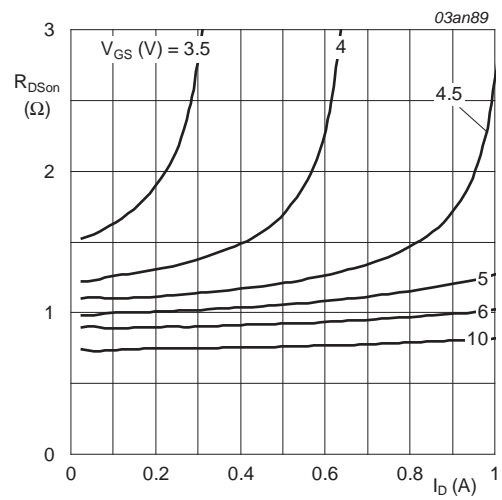


Fig 7. Drain-source on-state resistance as a function of drain current; typical values

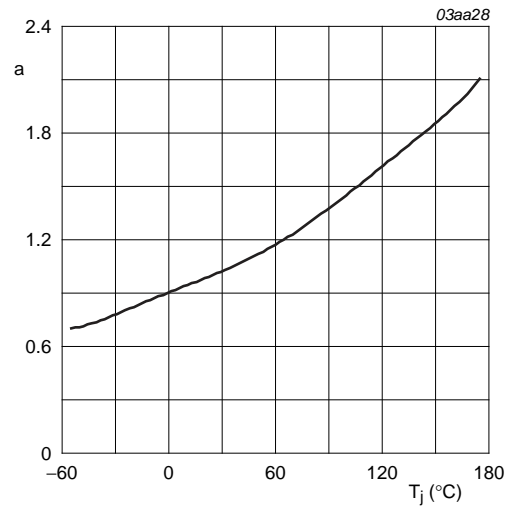
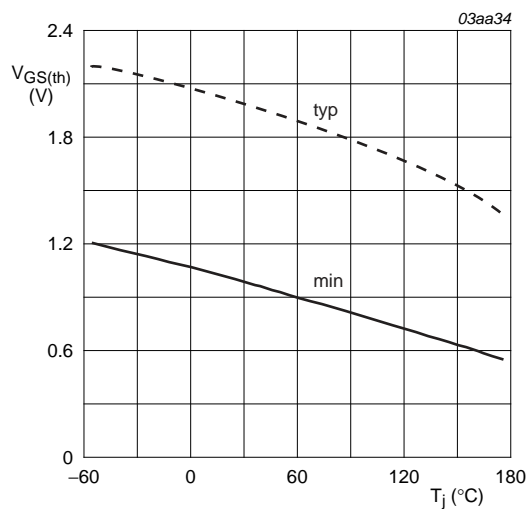
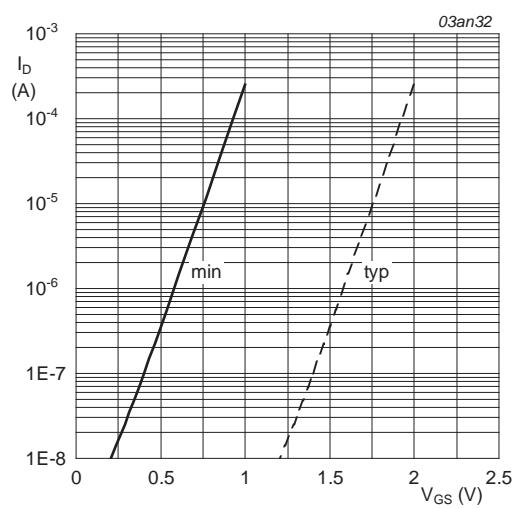


Fig 8. Normalized drain-source on-state resistance as a function of junction temperature



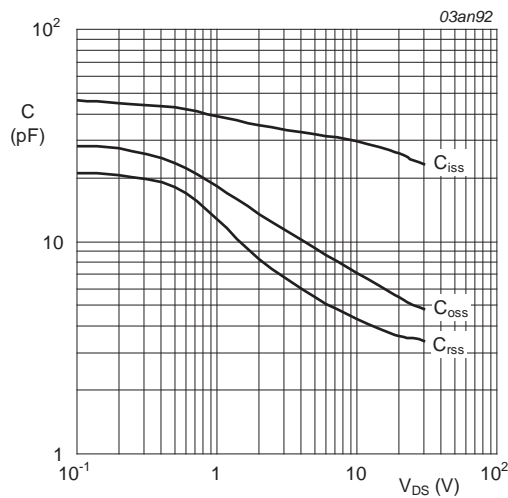
$I_D = 0.25 \text{ mA}$; $V_{DS} = V_{GS}$

Fig. 9. Gate-source threshold voltage as a function of junction temperature



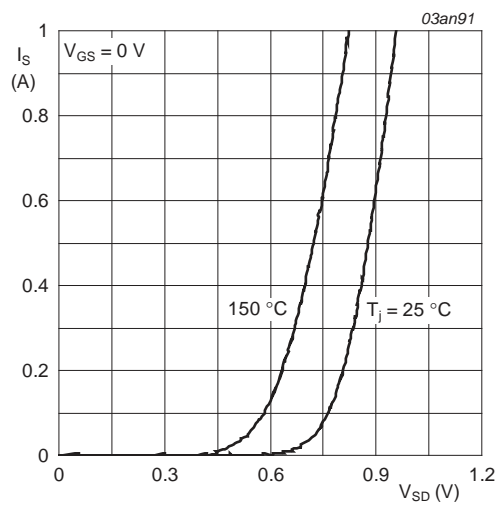
$T_j = 25 \text{ }^\circ\text{C}$; $V_{DS} = 5 \text{ V}$

Fig. 10. Sub-threshold drain current as a function of gate-source voltage



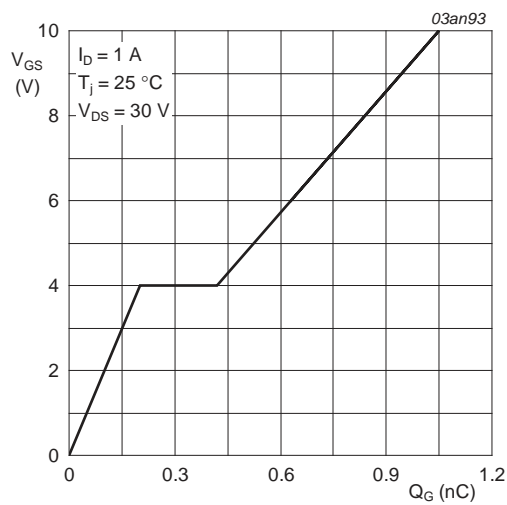
$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig. 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_J = 25\text{ °C}$ and 150 °C ; $V_{GS} = 0\text{ V}$

Fig 12. Source current as a function of source-drain voltage; typical values



$I_D = 1\text{ A}$; $V_{DD} = 30\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values

7. Package outline

Plastic surface-mounted package; 6 leads

SOT363

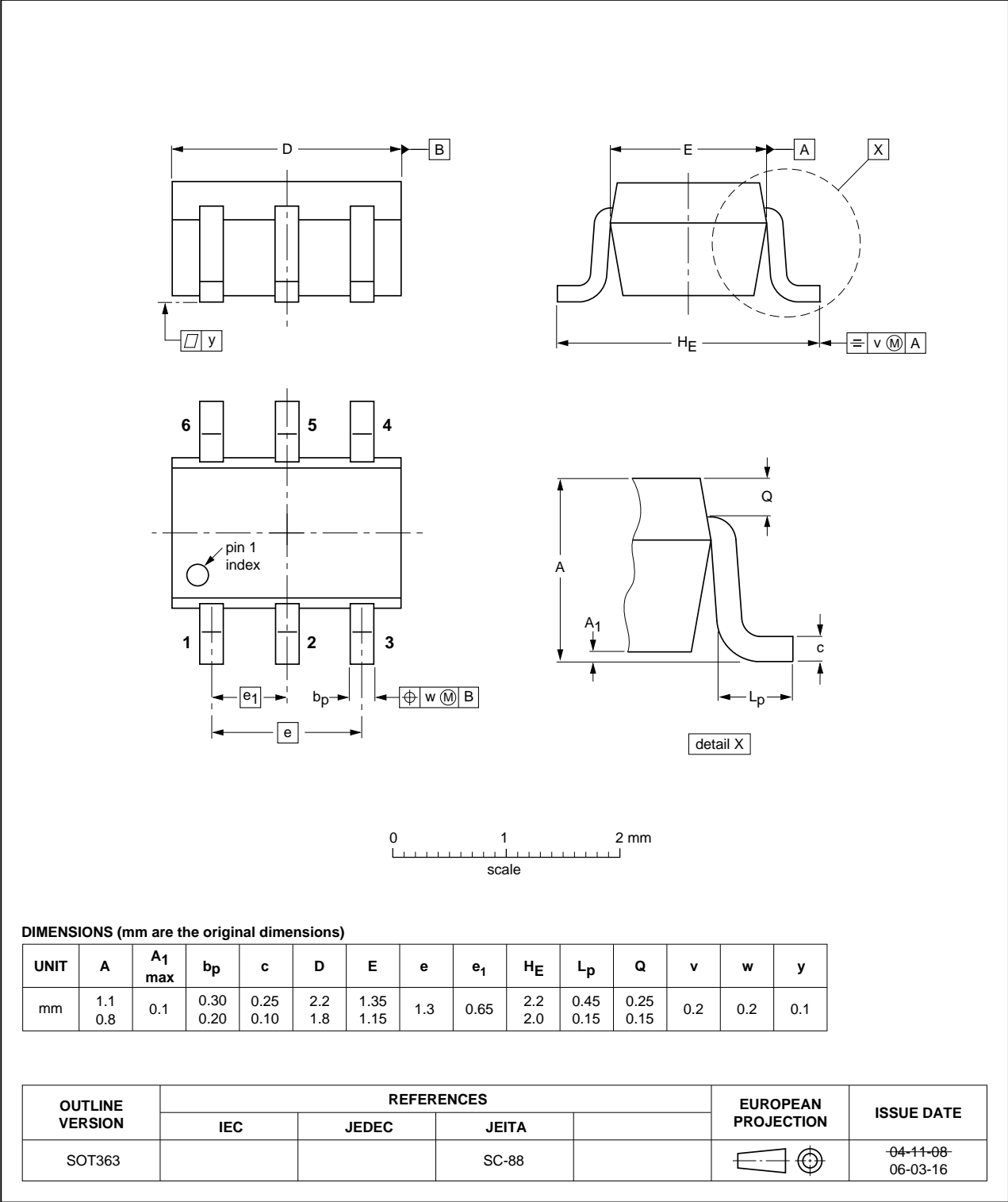
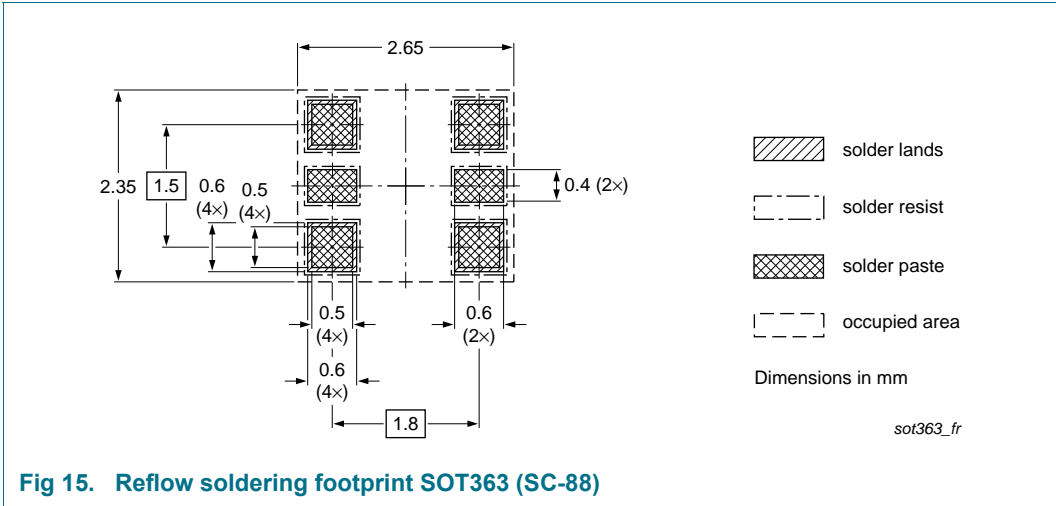


Fig 14. Package outline SOT363 (SC-88)

8. Soldering



9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMGD780SN_2	20100419	Product data sheet	-	PMGD780SN_1
Modifications:	<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.• Table 5 “Characteristics”: added $V_{GS(th)}$ maximum value at condition $T_j = 25\text{ }^{\circ}\text{C}$• Section 10 “Legal information”: updated			
PMGD780SN_1	20040211	Product data	-	-

10. Legal information

10.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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