PI3WVR12612

HDMI 2.0, DisplayPort 1.2 Video Switch

Features

- 4-lane, 1:2 mux/demux that will support RBR, HBR1, or HBR2
- Data rate: 3.4 Gbps to 6.0 Gbps for high data channels
- 1-channel 1:2 mux/demux for HPD signal
- Differential switch matrix for DP AUX and HDMI DDC
- supports 720 Mbps high-speed DP AUX
- -2.0 dB Insertion Loss for Dx channels @ 3 GHz
- -3 dB Bandwidth for Dx channels: 4.1 GHz
- Return loss for Dx channels @ 3 GHz: -12 dB
- Low Crosstalk for high speed channels: -25 dB@ 6 Gbps
- Low Off Isolation for high speed channels: -24dB@ 6 Gbps
- Low channel-to-channel skew, 35ps max
- Low Bit-to-Bit Skew, 5ps typ (between '+' and '-' bits)
- V_{DD} Operating Range: 3.3V +/-10%
- ESD Tolerance: 2kV HBM
- Packaging (Pb-free & Green):
  -50-ball TFBGA (NEE)
  -52-pin TQFN (ZL52)

Description

Pericom Semiconductor's PI3WVR12612 is a multi-standard video switch with wide voltage range capability. It supports DisplayPort 1.2, HDMI 2.0, and emerging and proprietary standards.

PI3WVR12612 can pass high-speed signals up to 1.2 V peak-to-peak differential with a common-mode voltage from 0 to 3.4V. The wide voltage range allows DC-coupled multi-standard operation. Eliminating AC coupling capacitors saves board space and improves signal integrity for dense PCB designs.

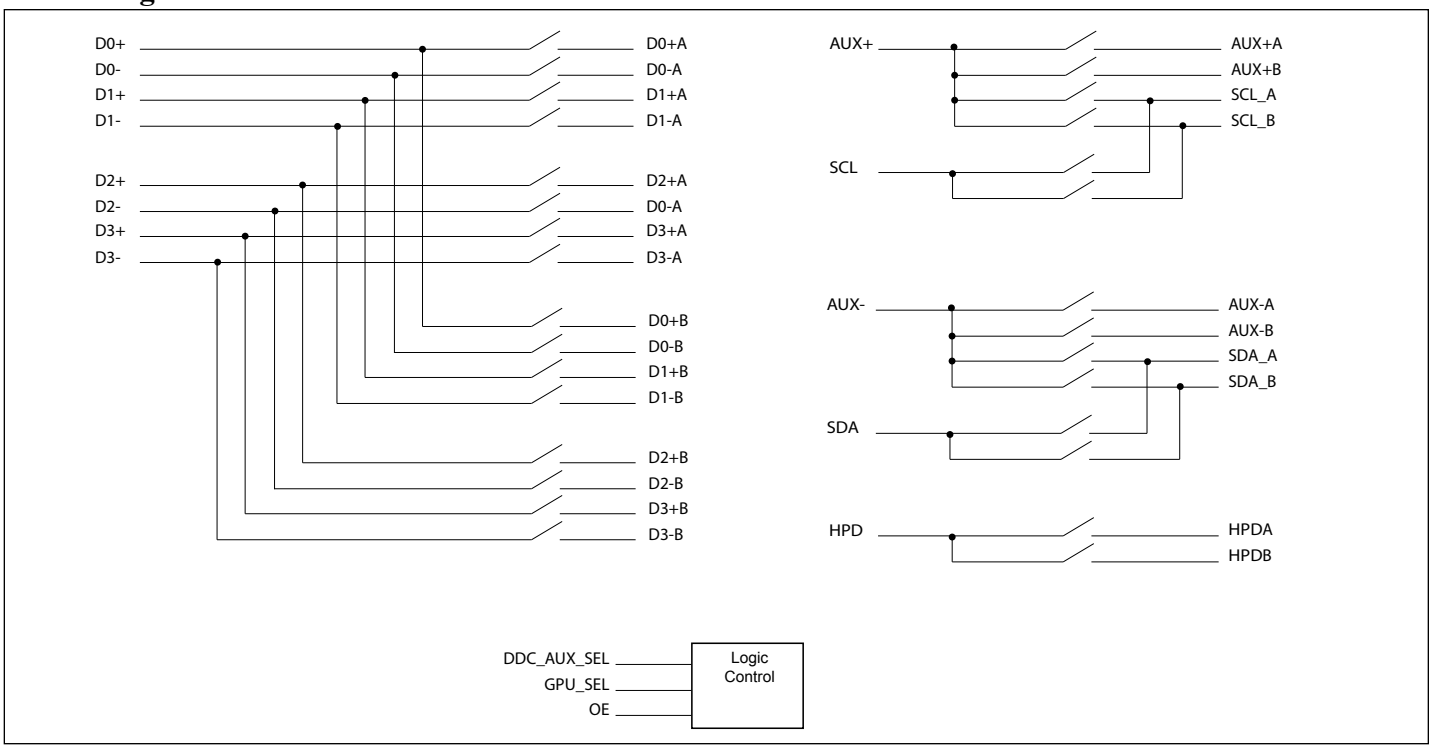
The high speed channels can also pass 0V-3.3V CMOS signals up to 1MHz.

In addition to four high-speed lanes, PI3WVR12612 also switches AUX, DDC, and HPD signals.

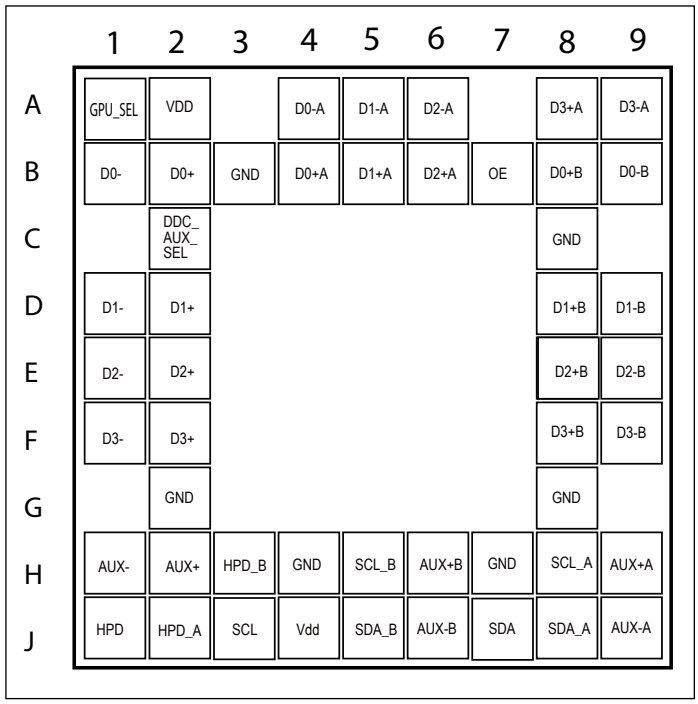
Application

Routing of DisplayPort and HDMI signals with low signal attenuation between source and sink.

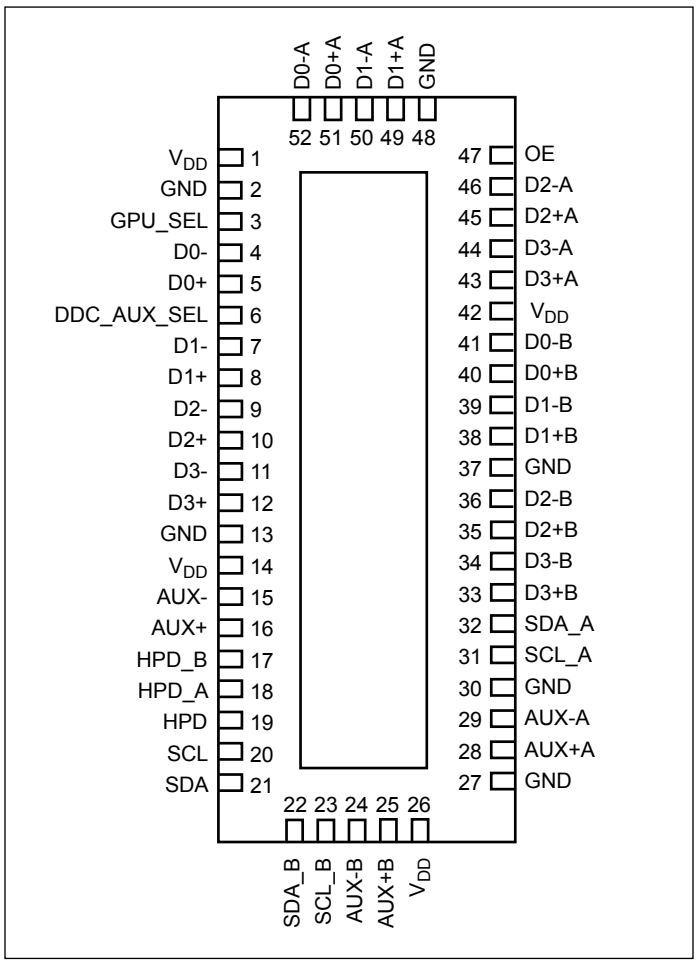
Block Diagram



Pin Assignment (50-Ball TFBGA, NEE)



Pin Assignment (52-Pin TQFN, ZL52)



Truth Table

Control			Switch Function			
OE	**GPU_ SEL**	**DDC_ AUX_ SEL**	**D0-D3**	**AUX**	**HPD**	**DDC**
High	Low	Low	A	AUX A	HPD A	Hi-Z
High	High	Low	B	AUX B	HPD B	Hi-Z
High	Low	High	A	DDC A	HPD A	Hi-Z
High	High	High	B	DDC B	HPD B	Hi-Z
High	Low	Medium	A	AUX A	HPD A	DDC A
High	High	Medium	B	AUX B	HPD B	DDC B
Low	x	x	Hi-Z	Hi-Z	Hi-Z	Hi-Z

➔ Medium level = 1/2 VDD = 1.65V

Pin Description

pin#	pin Name	Signal Type	Description
A1	GPU_SEL	I	switch logic control
B1	D0-	I/O	negative differential signal 0 for COM port
B2	D0+	I/O	positive differential signal 0 for COM port
D1	D1-	I/O	negative differential signal 1 for COM port
D2	D1+	I/O	positive differential signal 1 for COM port
E1	D2-	I/O	negative differential signal 2 for COM port
E2	D2+	I/O	positive differential signal 2 for COM port
F1	D3-	I/O	negative differential signal 3 for COM port
F2	D3+	I/O	positive differential signal 3 for COM port
B3	GND	Ground	Ground
H1	AUX-	I/O	negative differential signal for AUX COM port
H2	AUX+	I/O	posititve differential signal for AUX COM port
J1	HPD	I/O	HPD for COM port
J2	HPD_A	I/O	HPD for port A
H3	HPD_B	I/O	HPD for port B
C8	GND	Ground	Ground
J4	VDD	Pwr	3.3V +/-10% power supply
G2	GND	Ground	Ground
H6	AUX+B	I/O	positive differential signal for AUX, port B
J6	AUX-B	I/O	negative differential signal for AUX, port B
H9	AUX+A	I/O	positive differential signal for AUX, port A
J9	AUX-A	I/O	negative differential signal for AUX, port A
G8	GND	Ground	Ground
F8	D3+B	I/O	positive differential signal 3 for portB
F9	D3-B	I/O	negative differential signal 3 for portB
E8	D2+B	I/O	positive differential signal 2 for portB
E9	D2-B	I/O	negative differential signal 2 for portB
D8	D1+B	I/O	positive differential signal 1 for portB
D9	D1-B	I/O	negative differential signal 1 for portB
B8	D0+B	I/O	positive differential signal 0 for portB
B9	D0-B	I/O	negative differential signal 0 for portB

(Continued)

pin#	pin Name	Signal Type	Description
A8	D3+A	I/O	positive differential signal 3 for port A
A9	D3-A	I/O	negative differential signal 3 for port A
H4	GND	Ground	
B6	D2+A	I/O	positive differential signal 2 for port A
A6	D2-A	I/O	negative differential signal 2 for port A
B5	D1+A	I/O	positive differential signal 1 for port A
A5	D1-A	I/O	negative differential signal 1 for port A
B4	D0+A	I/O	positive differential signal 0 for port A
A4	D0-A	I/O	negative differential signal 0 for port A
A2	VDD	Pwr	Power
C2	DDC_ AUX_SEL	I	switch logic control
H5	SCL_B	I/O	DDC_clock channel for port B
H7	GND	Ground	
H8	SCL_A	I/O	DDC_clock channel for port A
J5	SDA_B	I/O	DDC_data channel for port B
J8	SDA_A	I/O	DDC_data channel for port A
J3	SCL	I/O	DDC_clock channel for COM port
J7	SDA	I/O	DDC_data channel for COM port
B7	OE	I	Output enable. if OE is high, IC is enabled. If OE is low, then IC is power down and all I/Os are hi-z

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +4.2V
DC Input Voltage	–0.5V to V_{DD}
High Speed Data Channel	–0.5V to 3.8V
HPD_x, SDA_x, SCL_x	-0.5V to 5.5V
DC Output Current	120mA
Power Dissipation	0.5W

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics for Switching over Operating Range (T_A = –40°C to +105°C, V_{DD} = 3.3V ±10%)

Parameter	Description	Test Conditions(1)	Min	Typ(2)	Max	Units
V_{IH}	Input HIGH Voltage (OE, GPU_SEL)	Guaranteed HIGH level	1.5			V
V_{IL}	Input LOW Voltage (OE, GPU_SEL)	Guaranteed LOW level			0.75	
V_{IH}	Input HIGH Voltage (DDC_AUX_SEL)	Guaranteed HIGH level	2.65		V_{DD}	
V_{IM}	Input Mid-Level Voltage (DDC_AUX_SEL)	Guaranteed MID level	V_{DD}/2-300mV	V_{DD}/2	V_{DD}/2+300mV	
V_{IL}	Input LOW Voltage (DDC_AUX_SEL)	Guaranteed LOW level	-0.5		0.6	
V_{IK}	Clamp Diode Voltage (HS Channel)	V_{DD} = Max., I_{IN} = –18mA		–1.6V	–1.8	
V_{IK}	Clamp Diode Voltage (Aux, Cntrl)	V_{DD} = Max., I_{IN} = –18mA		–0.7	–1.5	
IIH	Input HIGH Current (All Control Pins)	V_{DD} = Max., V_{IN} = V_{DD}			±5	µA
I_{IL}	Input LOW Current (All Control Pins)	V_{DD} = Max., V_{IN} = GND			±5	
I_{OFF_SB}	I/O leakage when part is off for sideband signals only (DDC, AUX, HPD)	V_{DD} = 0V, V_{INPUT} = 0V to 3.6V			20	
R_{ON_HS}	On resistance between input to output for high speed signals	$V_{INPUT,cm}$ = 0V to 3.4V, $V_{INPUT,diff}$ < $1.2V_{p\text{-}p,diff}$, V_{DD} = 3.0V, I_{INPUT} = 20mA		11		Ohm
R_{ON_AUX}	On resistance between input to output for side-band signals (AUX)	V_{DD} = 3.0V, Vinput = 0 to 3.3V, I_{INPUT} = 20mA		7		Ohm
R_{ON_DDC}	On resistance between input to output for DDC channel	V_{DD} = 3.0V, Vinput = 0V, I_{INPUT} = 20mA		12		Ohm
R_{ON_HPD}	On resistance between input to output for HPD channel	V_{DD} = 3.0V, Vinput = 0 to 3.0V, I_{INPUT} = 20mA		7		Ohm
V_{AUX_SS}	Signal Swing Tolerance in Aux path	V_{DD} = 3.0V	–0.5		5.5	V
V_{HPD_I}	Input voltage on HPD path				5.5	V
V_{HPD_O}	Output voltage tolerance on HPD path	HPD input from 3.3V to 5.25V		3.3	3.6	V
V_{SDA_X}	Input Voltage on SDA path			5		V
V_{PASS} (SDA_X)	Switch output voltage tolerance input	V_{in} = 5.25V, Ii = 100uA, V_{DD} = 3.3V	1.8	2.2	2.5	V
V_{SCL_X}	Input Voltage on SCL path			5		V
V_{PASS} (SCL_X)	Switch output voltage tolerance input	V_{in} = 5.25V, Ii = 100uA, V_{DD} = 3.3V	1.8	2.2	2.5	V

Power Supply Characteristics (T_A = –40°C to +105°C)

Parameter	Description	Test Conditions(1)	Min	Typ(2)	Max	Units
I_{DD}	Power Supply Current	V_{DD} = 3.3V, V_{IN} = GND or V_{DD}		1	3	mA
$I_{DD,Off}$	Power Supply Current, Disabled	V_{DD} = 3.3V, V_{IN} = GND or V_{DD}, $V_{OE} < V_{IL}$		1	50	µA

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

Dynamic Electrical Characteristics over Operating Range (T_A = -40° to +105°C, V_{DD} = 3.3V ±10%)

Parameter	Description	Test Conditions[1]		Min	Typ[2]	MAX	Units
X_{TALK}	Crosstalk on High Speed Channels	See Fig. 1 for Measurement Setup	f= 3.0 GHz		-25	-22	
			f= 2.7 GHz		-28	-25	dB
			f = 1.35 GHz		-32	-28	
O_{IRR}	OFF Isolation on High Speed Channels	See Fig. 2 for Measurement Setup,	f= 3.0 GHz		-24	-20	
			f= 2.7 GHz		-25	-22	
			f = 1.35 GHz		-30	-27	
I_{LOSS}	Differential Insertion Loss on High Speed Channels	@6.0Gbps (see figure 4)		-2.3	-2.0		dB
		@5.4Gbps (see figure 3)		-2.0	-1.8		
R_{loss}	Differential Return Loss on high speed channels	@3.0GHz (6.0Gbps)			-12	-11	dB
		@ 2.7GHz (5.4Gbps)			-14	-12.5	
BW_Dx±	Bandwidth -3dB for Main high speed path (Dx±)	See figure 3		3.7	4.1		GHz
BW_AUX/ HPD	-3dB BW for AUX, DDC, and HPD signals	See figure 3		1.35	1.5		GHz

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

Switching Characteristics (T_A= -40° to +105°C, V_{DD} = 3.3V±10%)

Parameter	Description	Min.	Typ.	Max.	Units
T_{pd}	Propagation delay (input pin to output pin) on Dx± channels		80		ps
$t_{b\text{-}b}$	Bit-to-bit skew within the same differential pair of Dx± channels		5	7	ps
$t_{ch\text{-}ch}$	Channel-to-channel skew of Dx± channels			35	ps
Tsw a-b	time it takes to switch from port A to port B			0.1	us
Tsw b-a	time it takes to switch from port B to port A			0.1	us
Tstartup	Vdd valid to channel enable			10	us
Twakeup	Enabling output by changing OE from low to High			10	us

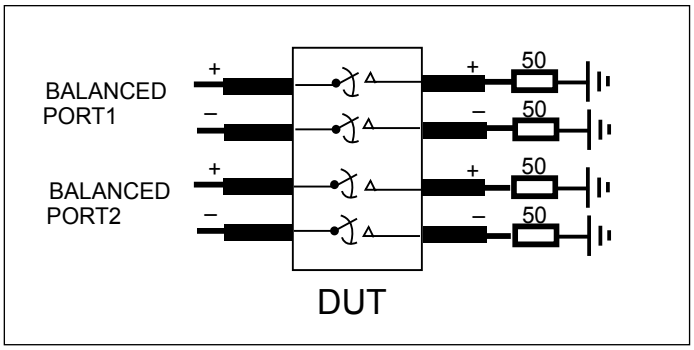


Fig 1. Crosstalk Setup

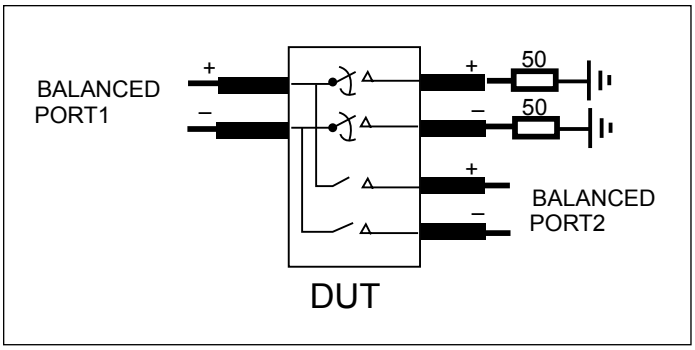


Fig 2. Off-isolation setup

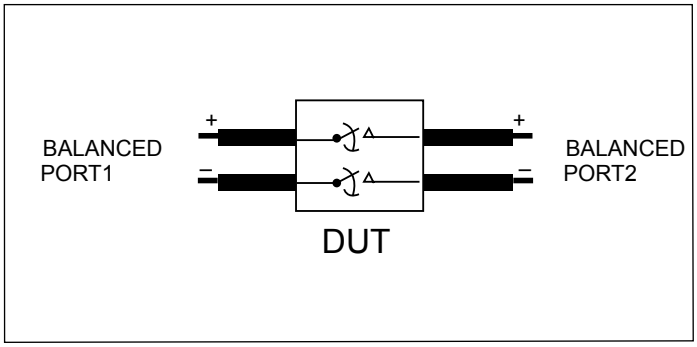
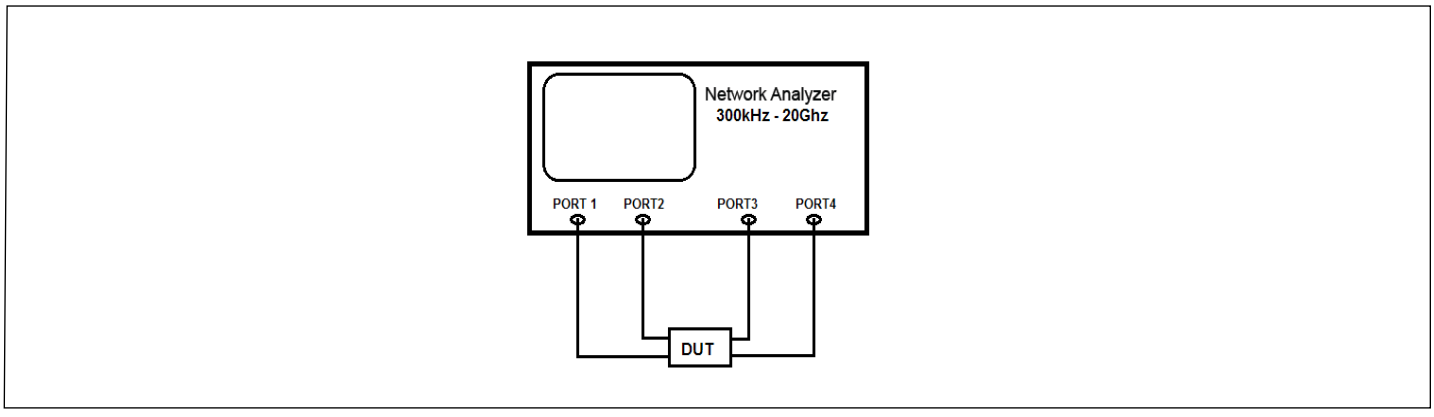


Fig 3. Differential Insertion Loss

Test Circuit for Dynamic Electrical Characteristics



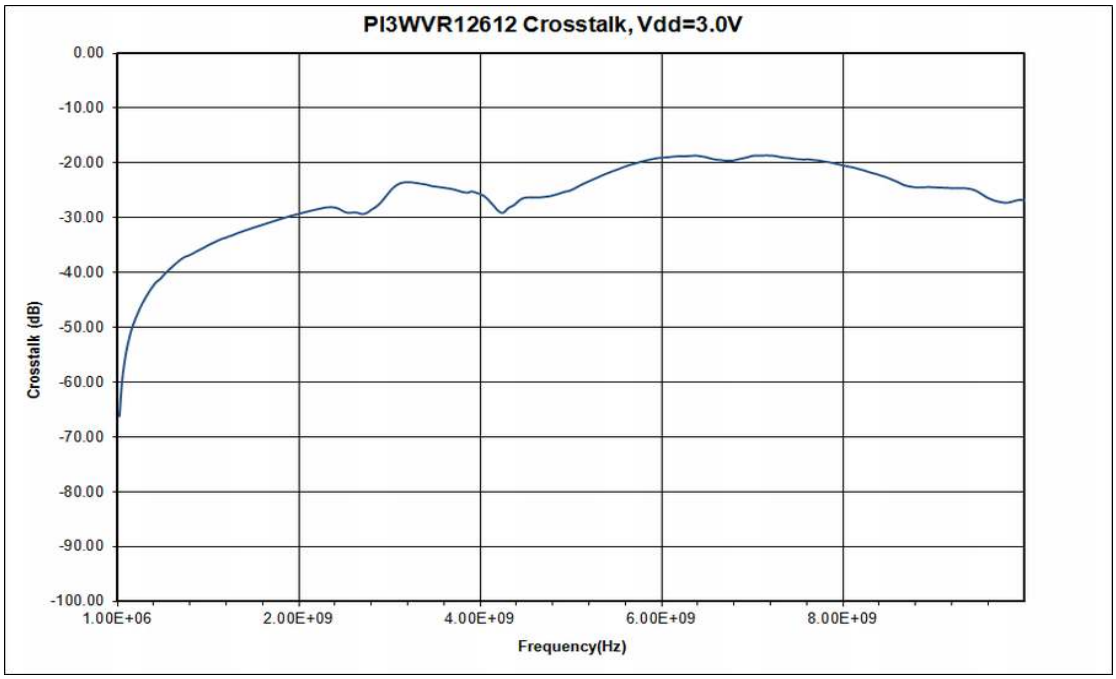


Fig 4. Crosstalk

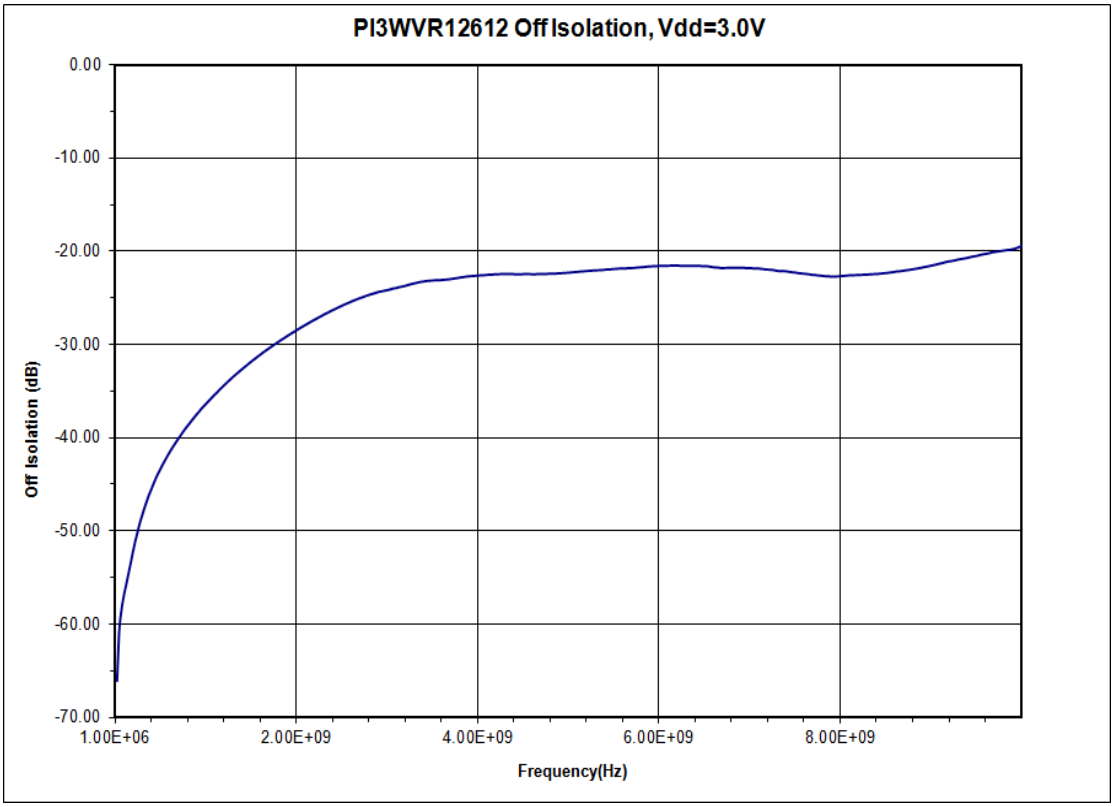


Fig 5. Off Isolation

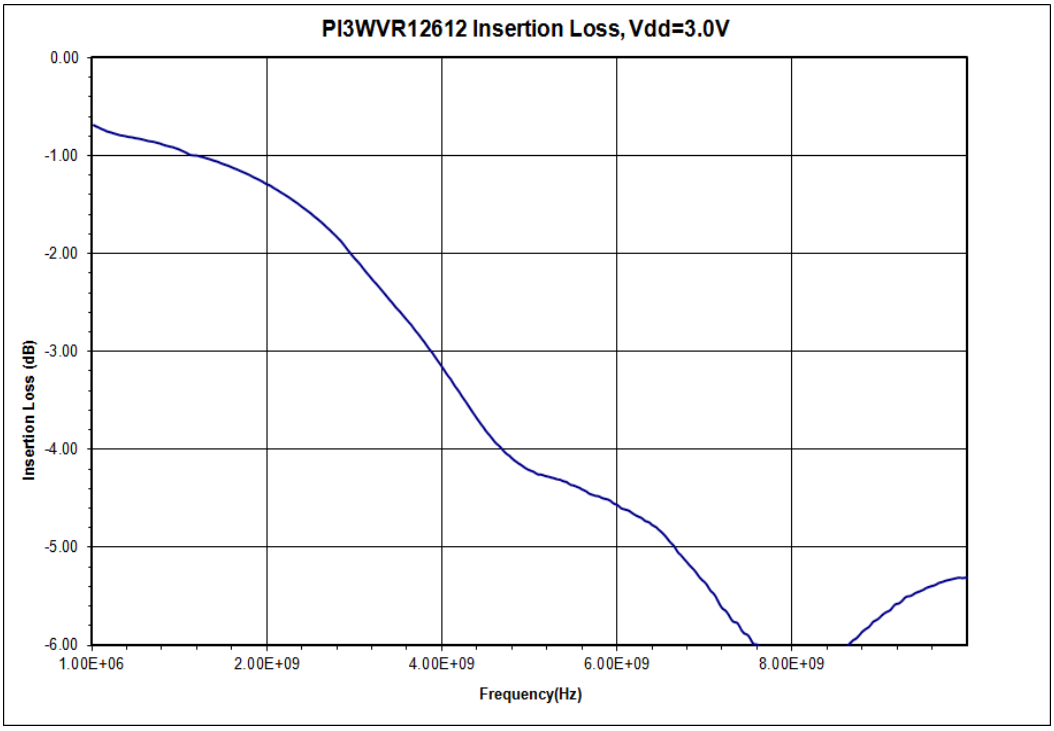


Fig 6. Insertion Loss

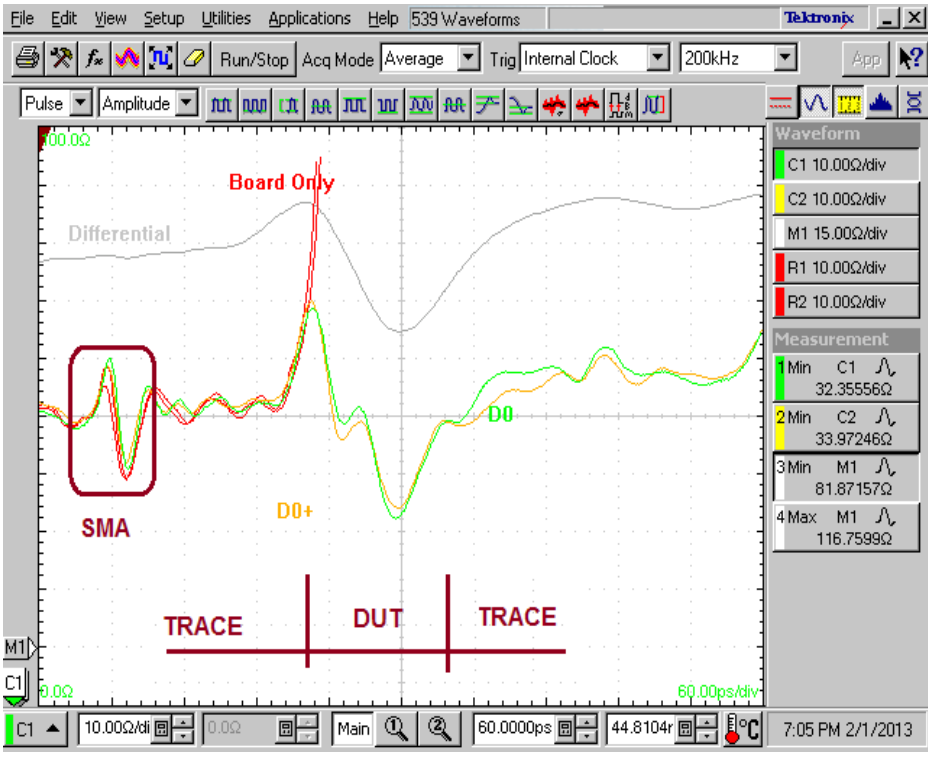


Fig 7. TDR Channel D0, VDD= 3.0V, 25C

Data Rate=2.7Gbps

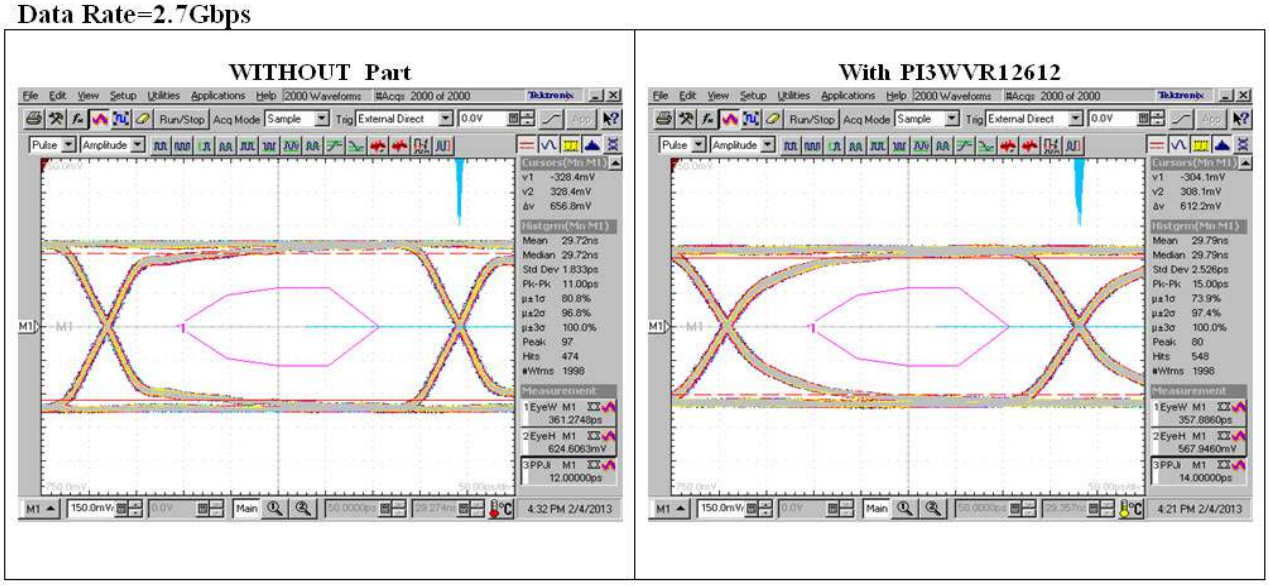


Fig 8. Differential output Eye at Input signal is a 2^7-1 PRBS, Vdd=3.0V, 25C, Input swing is 800mV differential

Data Rate=5.4Gbps

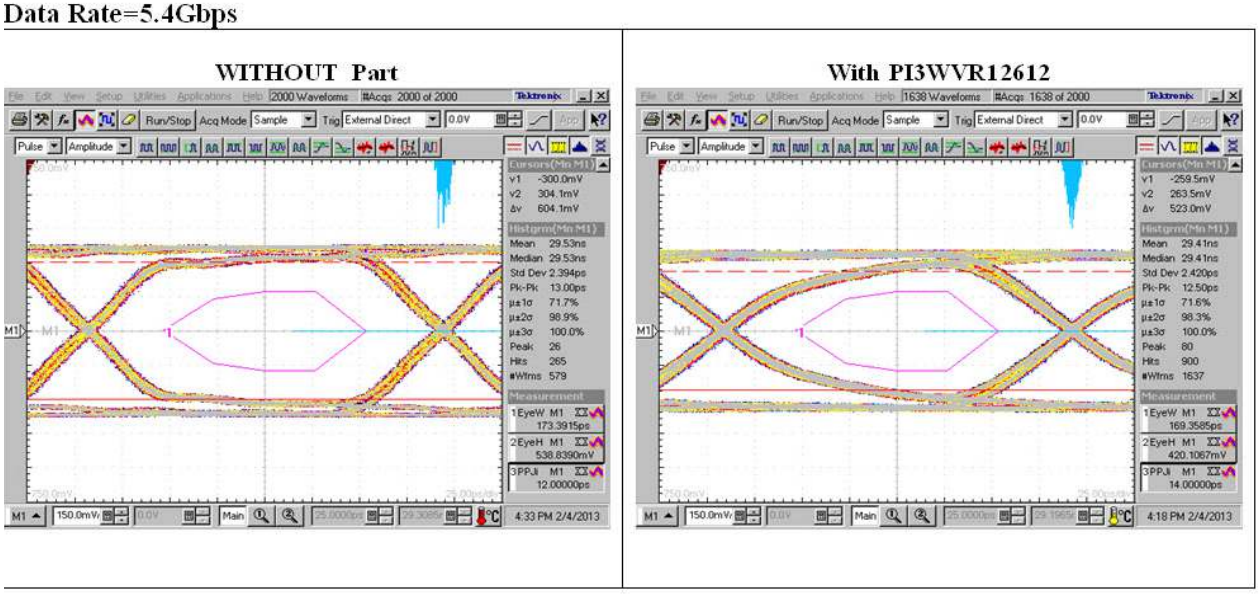
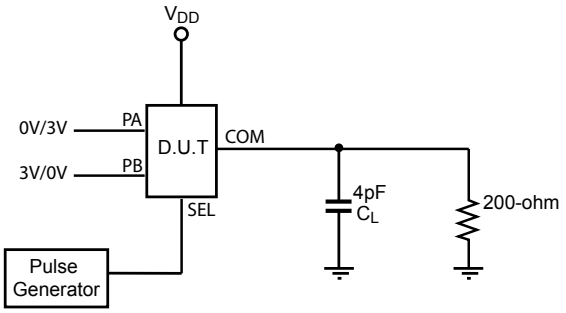


Fig 9. Differential output Eye at Input signal is a 2^7-1 PRBS, Vdd=3.0V, 25C, Input swing is 800mV differential

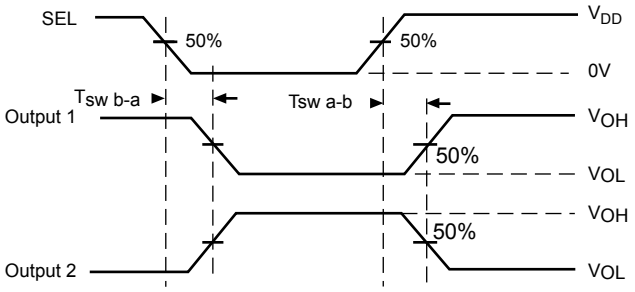
Test Circuit for Electrical Characteristics(1-5)



Notes:

1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
3. All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, $Z_O = 50\Omega$, $t_R \leq 2.5$ns, $t_F \leq 2.5$ns.
4. The outputs are measured one at a time with one transition per measurement.

Switching Waveforms

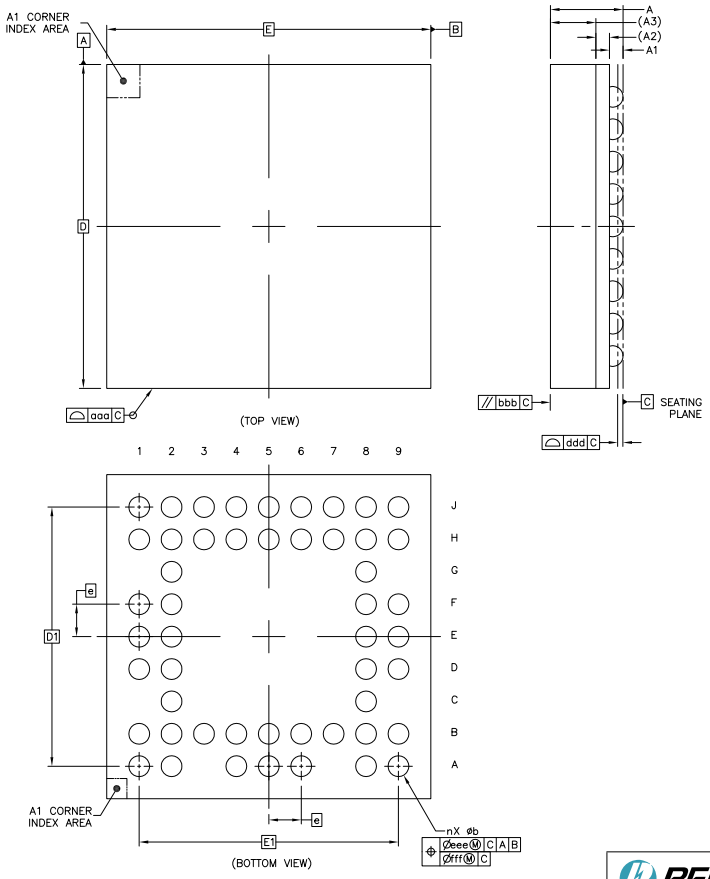


Voltage Waveforms Enable and Disable Times

Test Condition

Output 1 Test Conditon	Output 2 Test Conditon
PA = Low	PA = High
PB = High	PB = Low

Packaging Mechanical: 50-Ball TFBGA (NE50)



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.1
STAND OFF	A1	0.16	---	0.26
SUBSTRATE THICKNESS	A2		0.21	REF
MOLD THICKNESS	A3		0.54	REF
BODY SIZE	D		5	BSC
	E		5	BSC
BALL DIAMETER			0.3	
BALL OPENING			0.275	
BALL WIDTH	b	0.27	---	0.37
BALL PITCH	e		0.5	BSC
BALL COUNT	n		50	
EDGE BALL CENTER TO CENTER	D1		4	BSC
	E1		4	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

Notes:
1. Controlling dimensions in millimeters
2. Ref: JEDEC MO-195C

PERICOM® Enabling Serial Connectivity

DATE: 04/04/13

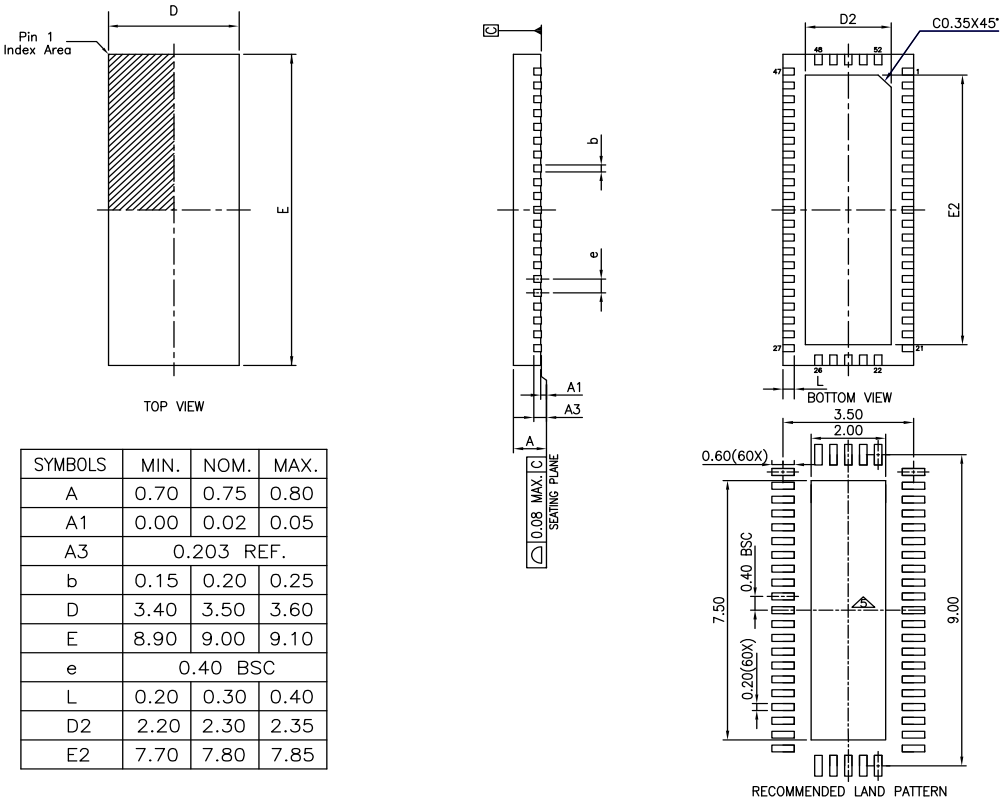
DESCRIPTION: 50-Ball, Thin Fine Pitch Ball Grid Array, (TFBGA)

PACKAGE CODE: NE50

DOCUMENT CONTROL #: PD - 2158 **REVISION: -**

13-0150

Packaging Mechanical: 52-Pin TQFN (ZL52)



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D	3.40	3.50	3.60
E	8.90	9.00	9.10
e		0.40 BSC	
L	0.20	0.30	0.40
D2	2.20	2.30	2.35
E2	7.70	7.80	7.85

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220.
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).

PERICOM Enabling Serial Connectivity — DATE: 04/25/14

DESCRIPTION: 52-Pin, TQFN 3.5X9.0mm

PACKAGE CODE: ZL (ZL52)

DOCUMENT CONTROL #: PD-2102 — REVISION: A

14-0122

Note:

For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Code	Package Code	Package Description
PI3WVR12612NEE	NE	50-Pin, Thin Fine Pitch Ball Grid Array (TFBGA)
PI3WVR12612NEEX	NE	50-Pin, Thin Fine Pitch Ball Grid Array (TFBGA), Tape & Reel
PI3WVR12612ZLE	ZL	52-Pin, 3.5 x 9.0 mm (TQFN)
PI3WVR12612ZLEX	ZL	52-Pin, 3.5 x 9.0 mm (TQFN), Tape & Reel

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging