*Click **here** to ask an associate for production status of specific part numbers.*

MAX32655

Low-Power, Arm Cortex-M4 Processor with FPU-Based Microcontroller and Bluetooth 5.2

General Description

The MAX32655 microcontroller (MCU) is an advanced system-on-chip (SoC) featuring an Arm® Cortex®-M4F CPU for efficient computation of complex functions and algorithms that is qualified to operate at a temperature range of -40°C to +105°C. The SoC integrates power regulation and management with a single inductor multiple-output (SIMO) buck regulator system. On board is the latest generation Bluetooth® 5.2 Low Energy (LE) radio, supporting LE Audio, angle of arrival (AoA), and angle of departure (AoD) for direction finding, long-range (coded), and high-throughput modes.

The device offers large onboard memory with 512KB flash and 128KB SRAM, with optional error correction coding on one 32KB SRAM bank. This 32KB bank can be optionally retained in BACKUP mode. An 8KB user OTP area is available, of which 8 bytes are retained, even during POWER DOWN mode.

Many high-speed interfaces are supported on the device, including multiple SPI, UART, and I^2C serial interfaces, plus one I^2S port for connecting to an audio codec. An eight-input, 10-bit ADC is available to monitor analog input from external analog sources.

The MAX32655 is available in a 81 CTBGA (8mm x 8mm, 0.8mm pitch) and a 60 WLP (3.13mm x 3.25mm, 0.35mm pitch).

Applications

- Asset Tracking
- Fitness/Health and Medical Wearables
- Hearables
- Industrial Sensors
- Wireless Computer Peripherals and I/O Devices

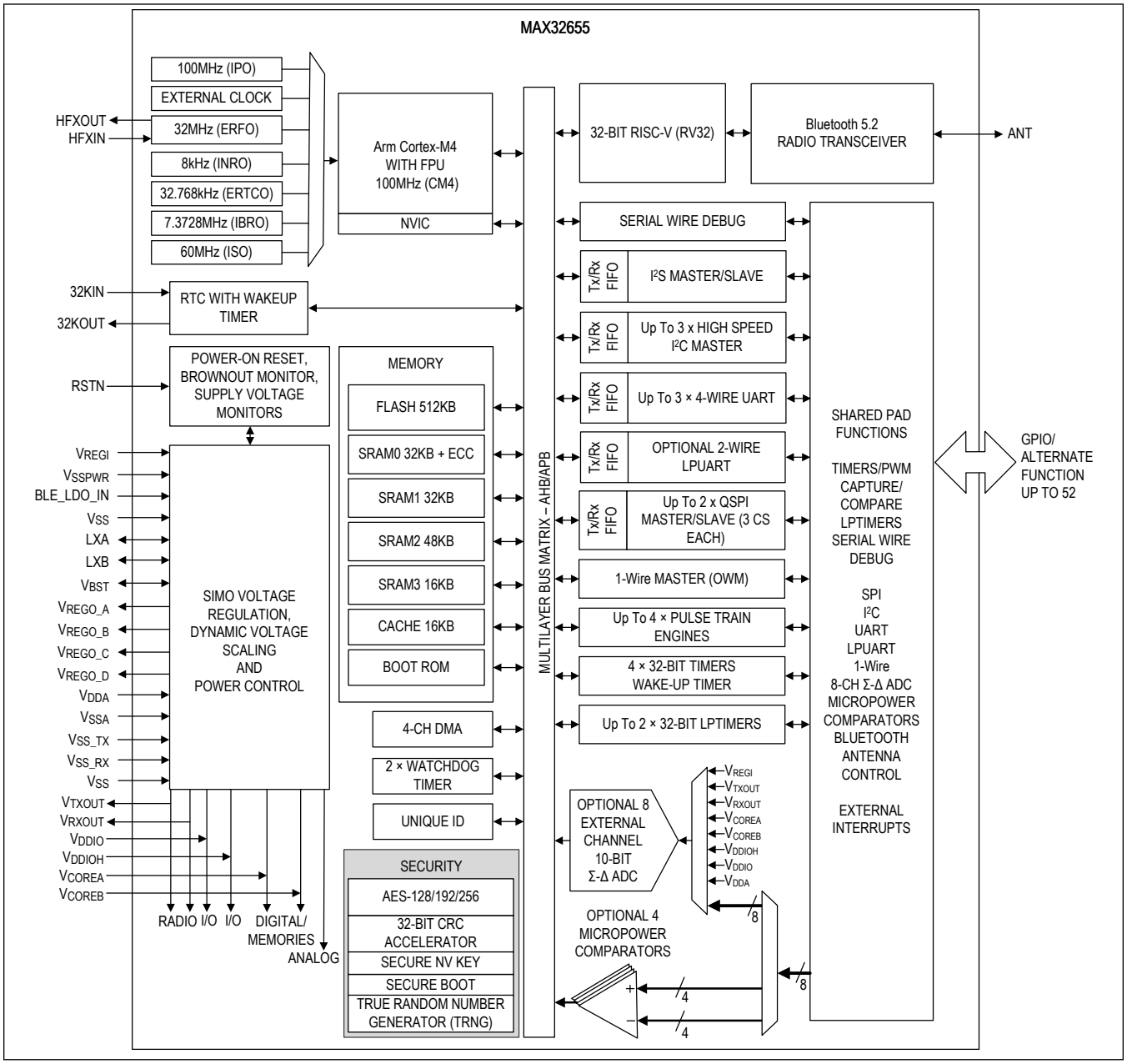
Benefits and Features

- Ultra-Low-Power Wireless Microcontroller
  - Internal 100MHz Oscillator
  - Flexible Low-Power Modes with 7.3728MHz System Clock Option
  - 512KB Flash and 128KB SRAM
    - Optional ECC on One 32KB SRAM Bank
  - 16KB Instruction Cache
- Bluetooth 5.2 LE Radio
  - Dedicated, Ultra-Low-Power, 32-Bit RISC-V Coprocessor to Offload Timing-Critical Bluetooth Processing
  - Fully Open-Source Bluetooth 5.2 Stack Available
  - Supports AoA, AoD, LE Audio, and Mesh
  - High-Throughput (2Mbps) Mode
  - Long-Range (125kbps and 500kbps) Modes
  - Rx Sensitivity: -97.5dBm; Tx Power: +4.5dBm
  - Single-Ended Antenna Connection (50Ω)
- Power Management Maximizes Battery Life
  - 2.0V to 3.6V Supply Voltage Range
  - Integrated SIMO Power Regulator
  - Dynamic Voltage Scaling (DVS)
  - 23.8µA/MHz Active Current at 3.0V
  - 4.4µA at 3.0V Retention Current for 32KB
  - Selectable SRAM Retention + RTC in Low-Power Modes
- Multiple Peripherals for System Control
  - Up to Two High-Speed SPI Master/Slave
  - Up to Three High-Speed I^2C Master/Slave (3.4Mbps)
  - Up to Four UART, One I^2S Master/Slave
  - Up to 8-Input, 10-Bit Sigma-Delta ADC 7.8ksps
  - Up to Four Micro-Power Comparators
  - Timers: Up to Four 32-Bit, Two LP, Two Watchdog Timers
  - 1-Wire® Master
  - Up to Four Pulse Train (PWM) Engines
  - RTC with Wake-Up Timer
  - Up to 52 GPIOs
- Security and Integrity
  - Available Secure Boot
  - TRNG Seed Generator
  - AES 128/192/256 Hardware Acceleration Engine

***Ordering Information** appears at end of data sheet.*

19-100883; Rev 2; 11/21

Simplified Block Diagram



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V_{DDIOH} ..... -0.3V to +3.6V
V_{REGI} ..... -0.3V to +3.6V
V_{DDA} ..... -0.3V to +1.89V
BLE_LDO_IN ..... -0.3V to 1.5V
RSTN, GPIO (V_{DDIOH}) ..... -0.3V to V_{DDIOH} + 0.5V
GPIO (V_{DDIO}) ..... -0.3V to V_{DDIO} + 0.5V
32KIN, 32KOUT ..... -0.3V to V_{DDA} + 0.2V
HFXIN, HFXOUT ..... -0.3V to V_{DDA} + 0.2V
Output Current (sink) by Any GPIO Pin 25mA
Output Current (source) by Any GPIO Pin ..... -25mA
V_{DDIO} Combined Pins (sink) 100mA
V_{DDIOH} Combined Pins (sink) 100mA
V_{SSA} 100mA
V_{SS}, V_{SS_TX}, V_{SS_RX} 100mA
V_{SSPWR} 100mA
Continuous Package Power Dissipation CTBGA (multilayer board) T_A = +70°C (derate 24.10mW/°C above +70°C) 1928.18mW
Continuous Package Power Dissipation WLP (multilayer board) T_A = +70°C (derate 22.33mW/°C above +70°C) 1228mW
Operating Temperature Range ..... -40°C to +105°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

81 CTBGA

Package Code	X8188+4C
Outline Number	21-0735
Land Pattern Number	90-0460
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	41.49°C/W
Junction to Case (θ_{JC})	10.81°C/W

60 WLP

Package Code	W603B3+1
Outline Number	21-100635
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	44.78°C/W
Junction to Case (θ_{JC})	N/A

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. TYP specifications are provided for T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Core Input Supply Voltage A	V_{COREA}		0.9	1.1	1.21	V
Core Input Supply Voltage B	V_{COREB}		0.9	1.1	1.21	V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. TYP specifications are provided for T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Voltage, Battery	V_{REGI}	Falling	2.0	3.0	3.6	V
		Rising	2.45	3.0	3.6	
Input Supply Voltage, Analog	V_{DDA}		1.71	1.8	1.89	V
Input Supply Voltage, TXIN	V_{TXIN}	Bluetooth transmitter supply	1.1	1.3	1.9	V
Input Supply Voltage, RXIN	V_{RXIN}	Bluetooth receiver supply	1.1	1.3	1.9	V
Input Supply Voltage, GPIO	V_{DDIO}		1.71	1.8	1.89	V
Input Supply Voltage, GPIO (High)	V_{DDIOH}		1.71	3.0	3.6	V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{COREA}		0.76		V
		Monitors V_{COREB}	0.72	0.77		
		Monitors V_{DDA}	1.58	1.64	1.69	
		Monitors V_{DDIO}	1.58	1.64	1.69	
		Monitors V_{DDIOH}	1.58	1.64	1.69	
		Monitors V_{REGI}	1.91	1.98	2.08	
		Monitors V_{RXOUT}		0.773		
		Monitors V_{TXOUT}		0.773		
Power-On Reset Voltage	V_{POR}	Monitors V_{COREA}		0.57		V
		Monitors V_{DDA}		1.25		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. TYP specifications are provided for T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{REGI} Current, ACTIVE Mode	I_{REGI_DACT}	Dynamic, IPO enabled, $f_{SYS\_CLK(MAX)}$ = 100MHz, total current into V_{REGI} pin, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, CM4 in ACTIVE mode executing Coremark®, RV32 in SLEEP mode, ECC disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		23.8		µA/MHz
		Dynamic, IPO enabled, $f_{SYS\_CLK(MAX)}$ = 100MHz, total current into V_{REGI} pin, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, CM4 and RV32 in ACTIVE mode executing While(1), ECC disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA. This specification is a function of the IPO frequency.		29.3		
		Dynamic, IPO enabled, $f_{SYS\_CLK(MAX)}$ = 100MHz, total current into V_{REGI} pin, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, CM4 in ACTIVE mode executing While(1), RV32 in SLEEP mode, ECC disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		22.2		
		Dynamic, total current into V_{REGI} pin, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, CM4 in SLEEP mode, RV32 in ACTIVE mode running from ISO, ECC disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		18.7		
	I_{REGI_FACT}	Fixed, IPO enabled, ISO enabled, total current into V_{REGI}, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, CM4 in ACTIVE mode 0MHz, RV32 in ACTIVE mode 0MHz; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		740		µA
V_{REGI} Current, SLEEP Mode	I_{REGI_DSLP}	Dynamic, IPO enabled, $f_{SYS\_CLK(MAX)}$ = 100MHz, ISO enabled, total current into V_{REGI} pins, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, CM4 in SLEEP mode, RV32 in SLEEP mode, ECC disabled, standard DMA with two channels active; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		6.4		µA/MHz
	I_{REGI_FSLP}	Fixed, IPO enabled, ISO enabled, total current into V_{REGI} pins, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, CM4 in SLEEP mode, RV32 in SLEEP mode, ECC disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		1.33		mA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. TYP specifications are provided for T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REGI} Current, LOW POWER Mode	I_{REGI_DLP}	Dynamic, ISO enabled, total current into V_{REGI} pins, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, CM4 powered off, RV32 in ACTIVE mode, $f_{SYS\_CLK(MAX)}$ = 60MHz; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA			18.7		µA/MHz
	I_{REGI_FLP}	Fixed, ISO enabled, total current into V_{REGI} pins, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, CM4 powered off, RV32 in ACTIVE mode 0MHz; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA			630		µA
V_{REGI} Current, MICRO POWER Mode	I_{REGI_DMP}	Dynamic, ERTCO enabled, IBRO enabled, total current into V_{REGI} pins, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, LPUART active, f_{LPUART} = 32.768kHz; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA			230		µA
V_{REGI} Current, STANDBY Mode	I_{REGI_STBY}	Fixed, total current into V_{REGI} pins, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA			7.1		µA
V_{REGI} Current, BACKUP Mode	I_{REGI_BK}	Total current into V_{REGI} pins, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, RTC disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA	All SRAM retained		6.3		µA
		Total current into V_{REGI} pins, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, RTC disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}, outputs source/sink 0mA	No SRAM retention		3		
		Total current into V_{REGI} pins, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, RTC disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA	SRAM0 retained		4.4		
			SRAM0 and SRAM1 retained		5.2		
			SRAM0, SRAM1, and SRAM2 retained		5.6		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. TYP specifications are provided for T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{REGI} Current, POWER DOWN Mode	I_{REGI_PDM}	Total current into V_{REGI} pins, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		0.16		µA
V_{REGO_X} Output Current	$V_{REGO\_X\_IOUT}$	Output current for each of the V_{REGO_X} outputs		5	50	mA
V_{REGO_X} Output Current Combined	$V_{REGO\_X\_IOUT\_TOT}$	All four V_{REGO_X} outputs combined		15	100	mA
V_{REGO_X} Output Voltage Range	$V_{REGO\_X\_RANGE}$	V_{REGI} ≥ V_{REGO_X} + 200mV; output voltage range must be configured to meet the input voltage range of the load device pin (V_{RST} to V_{MAX})	V_{RST}	1.0	V_{MAX}	V
V_{REGO_X} Efficiency	$V_{REGO\_X\_EFF}$	V_{REGI} = 2.7V, V_{REGO_X} = 1.1V, load = 30mA		90		%
SLEEP Mode Resume Time	t_{SLP_ON}	Time from power mode exit to execution of first user instruction		0.847		µs
LOW POWER Mode Resume Time	t_{LP_ON}	Time from power mode exit to execution of first user instruction		6.08		µs
MICRO POWER Mode Resume Time	t_{MP_ON}	Time from power mode exit to execution of first user instruction		12.4		us
STANDBY Mode Resume Time	t_{STBY_ON}	Time from power mode exit to execution of first user instruction		14.7		µs
BACKUP Mode Resume Time	t_{BKU_ON}	Time from power mode exit to execution of first user instruction		1.15		ms
POWER DOWN Mode Resume Time	t_{PDM_ON}	Time from power mode exit to execution of first user instruction		5		ms
CLOCKS						
System Clock Frequency	f_{SYS_CLK}				100,000	kHz
Internal Primary Oscillator (IPO)	f_{IPO}			100		MHz
Internal Secondary Oscillator (ISO)	f_{ISO}			60		MHz
Internal Baud Rate Oscillator (IBRO)	f_{IBRO}			7.3728		MHz
Internal Nano-Ring Oscillator (INRO)	f_{INRO}	8kHz selected		8		kHz
		16kHz selected		16		
		30kHz selected		30		
External RTC Oscillator (ERTCO)	f_{ERTCO}	32kHz watch crystal, C_L = 6pF, ESR < 90kΩ, C_0 ≤ 2pF		32.768		kHz
External RF Oscillator Frequency (ERFO)	f_{ERFO}	32MHz crystal, C_L = 12pF, ESR ≤ 50Ω, C_0 ≤ 7pF, temperature stability ±20ppm, initial tolerance ±20ppm		32		MHz

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. TYP specifications are provided for T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RTC Operating Current	I_{RTC}	All power modes, RTC enabled			0.3		µA
RTC Power-Up Time	t_{RTC_ON}				250		ms
External System Clock Input Frequency	f_{EXT_CLK}	EXT_CLK selected				80	MHz
External Low-Power Timer 1 Clock Input Frequency	$f_{EXT\_LPTMR1\_CLK}$	LPTMR1_CLK selected				8	MHz
External Low-Power Timer 2 Clock Input Frequency	$f_{EXT\_LPTMR2\_CLK}$	LPTMR2_CLK selected				8	MHz
GENERAL-PURPOSE I/O							
Input Low Voltage for All GPIO Except P3.0 and P3.1	V_{IL_VDDIO}	P3.0 and P3.1 can only use V_{DDIOH} as I/O supply and cannot use V_{DDIO} as I/O supply	V_{DDIO} selected as I/O supply			0.3 × V_{DDIO}	V
Input Low Voltage for All GPIO	V_{IL_VDDIOH}	V_{DDIOH} selected as I/O supply				0.3 × V_{DDIOH}	V
Input Low Voltage for RSTN	V_{IL_RSTN}				0.5 x V_{DDIOH}		V
Input High Voltage for All GPIO Except P3.0 and P3.1	V_{IH_VDDIO}	P3.0 and P3.1 can only use V_{DDIOH} as I/O supply and cannot use V_{DDIO} as I/O supply	V_{DDIO} selected as I/O supply	0.7 × V_{DDIO}			V
Input High Voltage for All GPIO	V_{IH_VDDIOH}	V_{DDIOH} selected as I/O supply		0.7 × V_{DDIOH}			V
Input High Voltage for RSTN	V_{IH_RSTN}				0.5 x V_{DDIOH}		V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. TYP specifications are provided for T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Low Voltage for All GPIO Except P3.0 and P3.1	V_{OL_VDDIO}	P3.0 and P3.1 can only use V_{DDIOH} as I/O supply and cannot use V_{DDIO} as I/O supply	V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 00, I_{OL} = 1mA		0.2	0.4	V
			V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 01, I_{OL} = 2mA		0.2	0.4	
			V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 10, I_{OL} = 4mA		0.2	0.4	
			V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 11, I_{OL} = 8mA		0.2	0.4	
Output Low Voltage for All GPIO	V_{OL_VDDIOH}	V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 00, I_{OL} = 1mA			0.2	0.4	V
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 01, I_{OL} = 2mA			0.2	0.4	
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 10, I_{OL} = 4mA			0.2	0.4	
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 11, I_{OL} = 8mA			0.2	0.4	
Combined I_{OL}, All GPIO	I_{OL_TOTAL}					48	mA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. TYP specifications are provided for T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output High Voltage for All GPIO Except P3.0 and P3.1	V_{OH_VDDIO}	P3.0 and P3.1 can only use V_{DDIOH} as I/O supply and cannot use V_{DDIO} as I/O supply	V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 00, I_{OL} = -1mA	V_{DDIO} - 0.4			V
			V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 01, I_{OL} = -2mA	V_{DDIO} - 0.4			
			V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 10, I_{OL} = -4mA	V_{DDIO} - 0.4			
			V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 11, I_{OL} = -8mA	V_{DDIO} - 0.4			
Output High Voltage for All GPIO Except P3.0 and P3.1	V_{OH_VDDIOH}	V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 00, I_{OL} = -1mA		V_{DDIOH} - 0.4			V
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 01, I_{OL} = -2mA		V_{DDIOH} - 0.4			
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 10, I_{OL} = -8mA		V_{DDIOH} - 0.4			
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 11, I_{OL} = -8mA		V_{DDIOH} - 0.4			
Output High Voltage for P3.0 and P3.1	V_{OH_VDDIOH}	V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] fixed at 00, I_{OL} = -1mA		V_{DDIOH} - 0.4			V
Combined I_{OH}, All GPIO	I_{OH_TOTAL}					-48	mA
Input Hysteresis (Schmitt)	V_{IHYS}				300		mV
Input Leakage Current Low	I_{IL}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 0V, internal pullup disabled		-100		+100	nA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. TYP specifications are provided for T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current High	I_{IH}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 3.6V, internal pulldown disabled	-800		+800	nA
	I_{OFF}	V_{DDIO} = 0V, V_{DDIOH} = 0V, V_{DDIO} selected as I/O supply, V_{IN} < 1.89V	-1		+1	µA
	I_{IH3V}	V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, V_{IN} = 3.6V	-2		+2	
Input Pullup Resistor RSTN	R_{PU_R}	Pullup to V_{DDIOH}		25		kΩ
Input Pullup/Pulldown Resistor for All GPIO	R_{PU1}	Normal resistance, P1M = 0		25		kΩ
	R_{PU2}	Highest resistance, P1M = 1		1		MΩ
BLUETOOTH RADIO / POWER						
Bluetooth LDO Input Voltage	$V_{BLE\_LDO\_IN}$		0.9	1.1	1.5	V
BLUETOOTH RADIO / FREQUENCY						
Operating Frequency		1MHz channel spacing	2360		2500	MHz
PLL Programming Resolution	PLL_{RES}			1		MHz
Frequency Deviation at 1Mbps	Δf_{1MHz}			±170		kHz
Frequency Deviation at BLE 1Mbps	$\Delta f_{BLE1MHz}$			±250		kHz
Frequency Deviation at 2Mbps	Δf_{2MHz}			±320		kHz
Frequency Deviation at BLE 2Mbps	$\Delta f_{BLE2MHz}$			±500		kHz
BLUETOOTH RADIO / CURRENT CONSUMPTION (SIMO enabled, V_{REGI} = 3.3V. IPO enabled, f_{SYS_CLK} = 100MHz, Bluetooth LE stack running on CM4. Measured at the V_{REGI} device pin, V_{REGO_B} = 0.9V, V_{REGO_C} = 1.0V, RV32 in SLEEP mode.)						
Tx Run Current	$I_{TX\_+4.5DBM}$	P_{RF} = +4.5dBm		6.35		mA
	$I_{RFFE\_+4.5DBM}$			4.3		
	I_{TX_0DBM}	P_{RF} = 0dBm		4.17		
	I_{RFFE_0DBM}			2.12		
	I_{TX_-10DBM}	P_{RF} = -10dBm		3.65		
	I_{RFFE_-10DBM}			1.65		
Tx Startup Current	I_{START_TX}			2.05		mA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. TYP specifications are provided for T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BLUETOOTH RADIO / CURRENT CONSUMPTION (SIMO enabled, V_{REGI} = 3.3V. IPO Enabled, f_{SYS_CLK} = 100MHz, BLE stack running on CM4. Measured at the V_{REGI} device pin, V_{REGO_B} = 0.9V, V_{REGO_C} = 1.0V, RV32 in SLEEP mode)							
Rx Run Current	I_{RX_1M}	f_{RX} = 1Mbps			4.0		mA
	I_{RX_2M}	f_{RX} = 2Mbps			4.12		
	I_{RFFE_1M}	f_{RX} = 1Mbps			1.95		
	I_{RFFE_2M}	f_{RX} = 2Mbps			2.07		
Rx Startup Current	I_{START_RX}				2.05		mA
BLUETOOTH RADIO / TRANSMITTER							
Maximum Output Power	P_{RF}				+4.5		dBm
RF Power Accuracy	P_{RF_ACC}				±1		dB
First Adjacent Channel Transmit Power ±2MHz	P_{RF1_1}	1Mbps Bluetooth LE			-30.5		dBc
First Adjacent Channel Transmit Power ±4MHz	P_{RF2_1}	1Mbps Bluetooth LE			-40		dBc
BLUETOOTH RADIO / RECEIVER							
Maximum Received Signal Strength at < 0.1% PER	P_{RX_MAX}				0		dBm
Receiver Sensitivity, Ideal Transmitter	P_{SENS_IT}	Measured with 37 byte payload	1Mbps Bluetooth LE		-97.5		dBm
			2Mbps Bluetooth LE		-94		
Receiver Sensitivity, Dirty Transmitter	P_{SENS_DT}	Measured with 37 byte payload	1Mbps Bluetooth LE		-95.5		dBm
			2Mbps Bluetooth LE		-93		
Receiver Sensitivity, Long Range Coded	P_{SENS_LR}	Measured with 37 Byte Payload	125kbps Bluetooth LE		-105.5		dBm
			500kbps Bluetooth LE		-101		
C/I Cochannel	C/I_{1MHz}	1Mbps Bluetooth LE			6.7		dB
	C/I_{2Mhz}	2Mbps Bluetooth LE			7		
Adjacent Interference	C/I_{+1_1}	+1MHz offset, 1Mbps Bluetooth LE			-2.5		dBm
	C/I_{-1_1}	-1MHz offset, 1Mbps Bluetooth LE			-2.6		
	C/I_{+2_1}	+2MHz offset, 1Mbps Bluetooth LE			-22		dB
	C/I_{-2_1}	-2MHz offset, 1Mbps Bluetooth LE			-24		
	C/I_{+2_2}	+2MHz offset, 2Mbps Bluetooth LE			-2		
	C/I_{-2_2}	-2MHz offset, 2Mbps Bluetooth LE			-3		
	C/I_{+4_2}	+4MHz offset, 2Mbps Bluetooth LE			-32		
	C/I_{-4_2}	-4MHz offset, 2Mbps Bluetooth LE			-34		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. TYP specifications are provided for T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Adjacent Interference, (3+n) MHz Offset [n = 0, 1, 2, . . .]	C/I_{3+MHZ}	1Mbps Bluetooth LE			-34.5		dB
Adjacent Interference, (6+2n) MHz Offset [n = 0, 1, 2, . . .]	C/I_{6+MHZ}	2Mbps Bluetooth LE			-34		dB
Intermodulation Performance, 1Mbps Bluetooth LE with 3MHz, 4MHz, 5MHz Offset	P_{IMD_1MBPS}	1Mbps Bluetooth LE			-38		dBm
Intermodulation Performance, 2Mbps Bluetooth LE with 6MHz, 8MHz, 10MHz Offset	P_{IMD_2MBPS}	2Mbps Bluetooth LE			-38		dBm
Received Signal Strength Indicator Accuracy	$RSSI_{ACC}$				±3		dB
Received Signal Strength Indicator Range	$RSSI_{RANGE}$				-98 to -50		dB
ADC (SIGMA-DELTA)							
Resolution					10		Bits
ADC Clock Rate	f_{ACLK}			0.1		8	MHz
ADC Clock Period	t_{ACLK}				$1/f_{ACLK}$		µs
Input Voltage Range	V_{AIN}	AIN[7:0], ADC_DIVSEL = [00], ADC_CH_SEL = [7:0]	REF_SEL = 0, INPUT_SCALE = 0	V_{SSA} + 0.05		V_{BG}	V
		AIN[7:0], ADC_DIVSEL = [01], ADC_CH_SEL = [7:0]	REF_SCALE = 0, INPUT_SCALE = 0	V_{SSA} + 0.05		2 x V_{BG}	
		AIN[7:0], ADC_DIVSEL = [10], ADC_CH_SEL = [7:0]	REF_SCALE = 0, INPUT_SCALE = 0, V_{DDIOH} selected as the I/O supply	V_{SSA} + 0.05		V_{DDIOH}	
		AIN[7:0], ADC_DIVSEL = [11], ADC_CH_SEL = [7:0]	REF_SEL = 0, INPUT_SCALE = 0, V_{DDIOH} selected as the I/O supply	V_{SSA} + 0.05		V_{DDIOH}	
Input Impedance	R_{AIN}				30		kΩ

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. TYP specifications are provided for T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. GPIO are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Input Capacitance	C_{AIN}	Fixed capacitance to V_{SSA}		1		pF
		Dynamically switched capacitance		250		fF
Integral Nonlinearity	INL	Measured at +25°C			±2	LSb
Differential Nonlinearity	DNL	Measured at +25°C			±1	LSb
Offset Error	V_{OS}			±1		LSb
ADC Active Current	I_{ADC}	ADC active, reference buffer enabled, input buffer disabled		102		µA
ADC Setup Time	t_{ADC_SU}	Any power-up of ADC clock or ADC bias to CpuAdcStart			10	µs
ADC Output Latency	t_{ADC}			1067		t_{ACLK}
ADC Sample Rate	f_{ADC}				7.8	ksps
ADC Input Leakage	I_{ADC_LEAK}	ADC inactive or channel not selected		10		nA
Full-Scale Voltage	V_{FS}	ADC code = 0x3FF		1.2		V
Bandgap Temperature Coefficient	V_{TEMPCO}	Box method		30		ppm
COMPARATORS						
Input Offset Voltage	V_{OFFSET}			±1		mV
Input Hysteresis	V_{HYST}	AINCOMPHYST[1:0] = 00		±23		mV
		AINCOMPHYST[1:0] = 01		±50		
		AINCOMPHYST[1:0] = 10		±2		
		AINCOMPHYST[1:0] = 11		±7		
Input Voltage Range	V_{IN_CMP}	Common-mode range	0.6		1.35	V
FLASH MEMORY						
Flash Erase Time	t_{M_ERASE}	Mass erase		20		ms
	t_{P_ERASE}	Page erase		20		
Flash Programming Time per Word	t_{PROG}			42		µs
Flash Endurance			10			kcycles
Data Retention	t_{RET}	T_A = +105°C	10			years

Electrical Characteristics—SPI

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MASTER MODE						
SPI Master Operating Frequency for SPI0	f_{MCK0}	f_{SYS_CLK} = 100MHz, $f_{MCK0(MAX)}$ = f_{SYS_CLK}/2			50	MHz
SPI Master Operating Frequency for SPI1	f_{MCK1}	f_{SYS_CLK} = 100MHz, $f_{MCK1(MAX)}$ = f_{SYS_CLK}/4			25	MHz
SPI Master SCK Period	t_{MCKX}			$1/f_{MCKX}$		ns

Electrical Characteristics—SPI (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MCKX}/2$			ns
MOSI Output Hold Time After SCK Sample Edge	t_{MOH}		$t_{MCX}/2$			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCKX}/2$			ns
MOSI Output Hold Time After SCK Low Idle	t_{MLH}			$t_{MCKX}/2$		ns
MISO Input Valid to SCK Sample Edge Setup	t_{MIS}			5		ns
MISO Input to SCK Sample Edge Hold	t_{MIH}			$t_{MCKX}/2$		ns
SLAVE MODE						
SPI Slave Operating Frequency	f_{SCK}				50	MHz
SPI Slave SCK Period	t_{SCK}			$1/f_{SCK}$		ns
SCK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		
SSx Active to First Shift Edge	t_{SSE}			10		ns
MOSI Input to SCK Sample Edge Rise/Fall Setup	t_{SIS}			5		ns
MOSI Input from SCK Sample Edge Transition Hold	t_{SIH}			1		ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}			5		ns
SCK Inactive to SSx Inactive	t_{SSD}			10		ns
SSx Inactive Time	t_{SSH}			$1/f_{SCK}$		µs
MISO Hold Time After SSx Deassertion	t_{SLH}			10		ns

Electrical Characteristics—I^2C

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STANDARD MODE						
Output Fall Time	t_{OF}	Standard mode, from $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
SCL Clock Frequency	f_{SCL}		0		100	kHz
Low Period SCL Clock	t_{LOW}		4.7			µs

Electrical Characteristics—I²C (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Time SCL Clock	t_{HIGH}		4.0			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		4.7			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		4.0			µs
Data Setup Time	$t_{SU;DAT}$			300		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			800		ns
Fall Time for SDA and SCL	t_F			200		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		4.0			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		4.7			µs
Data Valid Time	$t_{VD;DAT}$		3.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		3.45			µs
FAST MODE						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		400	kHz
Low Period SCL Clock	t_{LOW}		1.3			µs
High Time SCL Clock	t_{HIGH}		0.6			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.6			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.6			µs
Data Setup Time	$t_{SU;DAT}$			125		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			30		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.6			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		1.3			µs
Data Valid Time	$t_{VD;DAT}$		0.9			µs

Electrical Characteristics—I²C (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.9			µs
FAST MODE PLUS						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		80		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		1000	kHz
Low Period SCL Clock	t_{LOW}		0.5			µs
High Time SCL Clock	t_{HIGH}		0.26			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.26			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.26			µs
Data Setup Time	$t_{SU;DAT}$			50		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			50		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.26			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		0.5			µs
Data Valid Time	$t_{VD;DAT}$		0.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.45			µs

Electrical Characteristics—I²S

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bit Clock Frequency	f_{BCLK}				25	MHz
BCLK High Time	t_{WBCLKH}			0.5 x $1/f_{BCLK}$		ns
BCLK Low Time	t_{WBCLKL}			0.5 x $1/f_{BCLK}$		ns
LRCLK Setup Time	t_{LRCLK_BLCK}			25		ns
Delay Time, BCLK to SD (Output) Valid	t_{BCLK_SDO}			12		ns
Setup Time for SD (Input)	t_{SU_SDI}			6		ns
Hold Time SD (Input)	t_{HD_SDI}			3		ns

Electrical Characteristics—1-Wire Master

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Write 0 Low Time	t_{W0L}	Standard		60		µs
		Overdrive		8		
Write 1 Low Time	t_{W1L}	Standard		6		µs
		Standard, Long Line mode		8		
		Overdrive		1		
Presence Detect Sample	t_{MSP}	Standard		70		µs
		Standard, Long Line mode		85		
		Overdrive		9		
Read Data Value	t_{MSR}	Standard		15		µs
		Standard, Long Line mode		24		
		Overdrive		3		
Recovery Time	t_{REC0}	Standard		10		µs
		Standard, Long Line mode		20		
		Overdrive		4		
Reset Time High	t_{RSTH}	Standard		480		µs
		Overdrive		58		
Reset Time Low	t_{RSTL}	Standard		600		µs
		Overdrive		70		
Time Slot	t_{SLOT}	Standard		70		µs
		Overdrive		12		

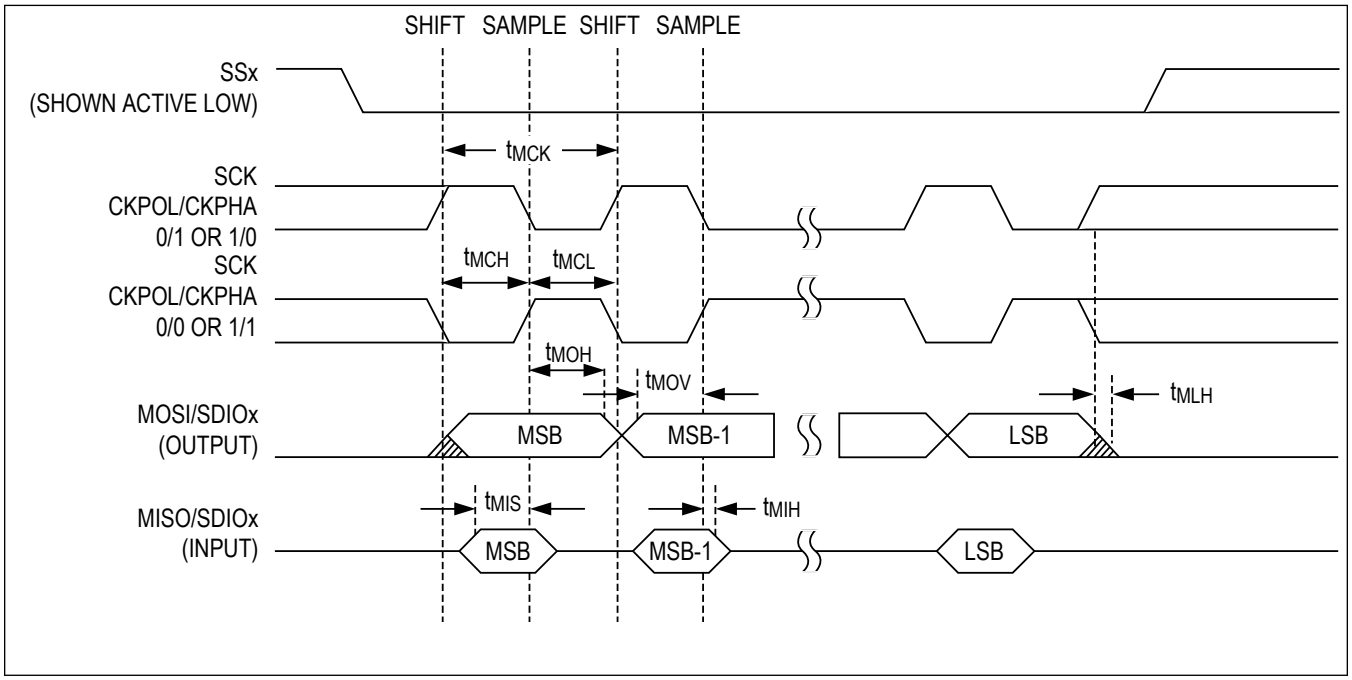


Figure 1. SPI Master Mode Timing Diagram

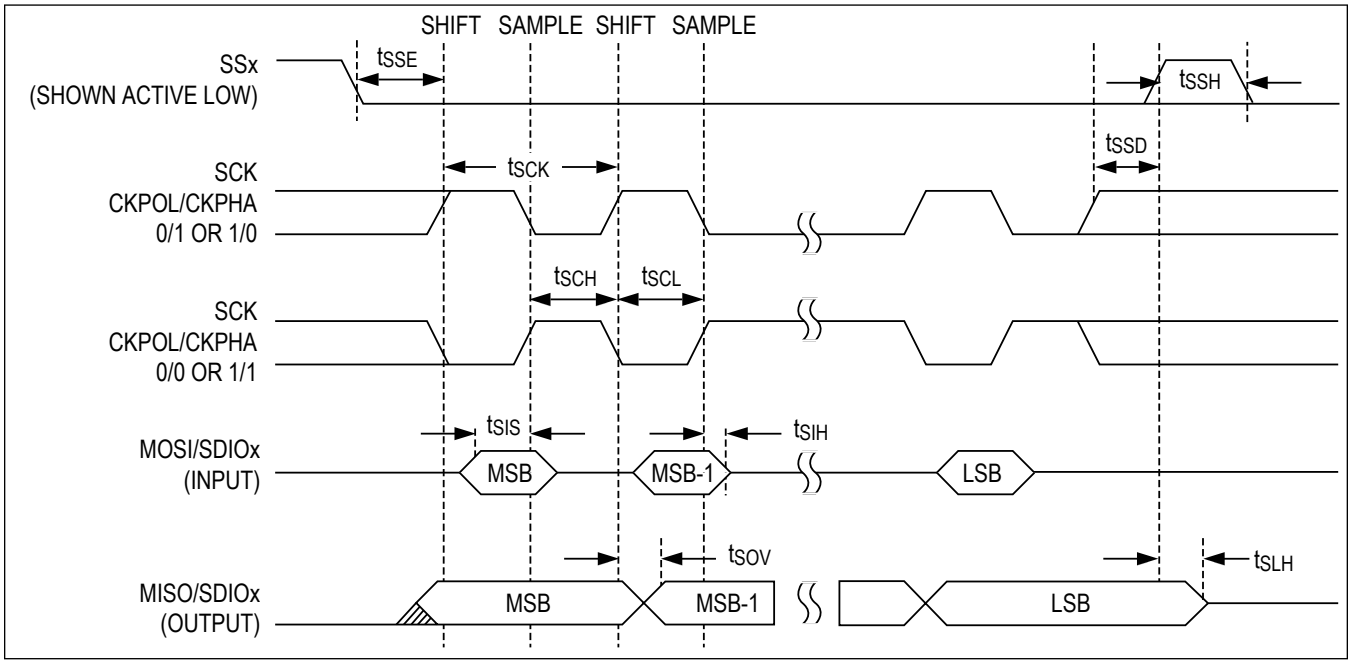


Figure 2. SPI Slave Mode Timing Diagram

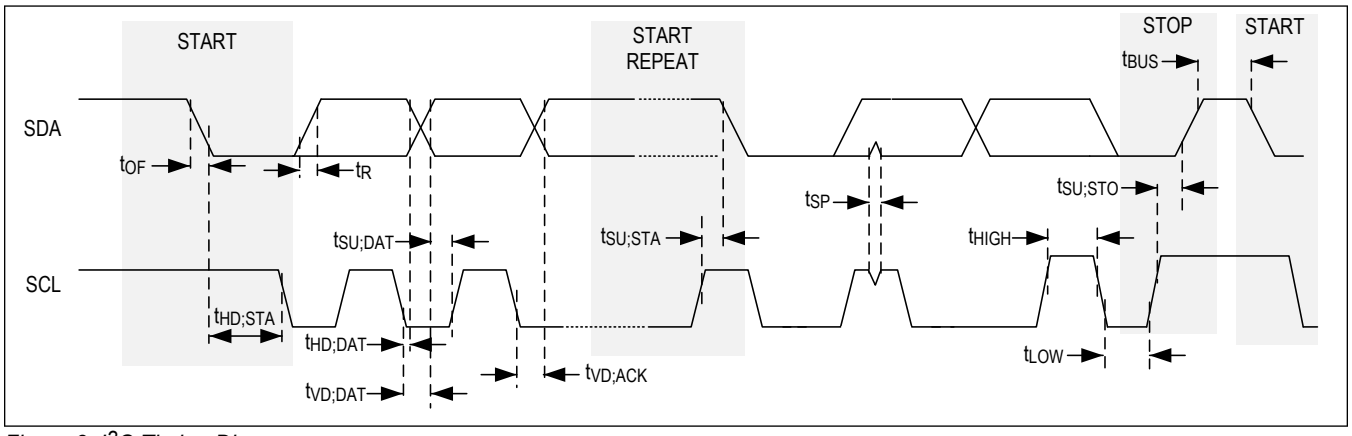


Figure 3. I²C Timing Diagram

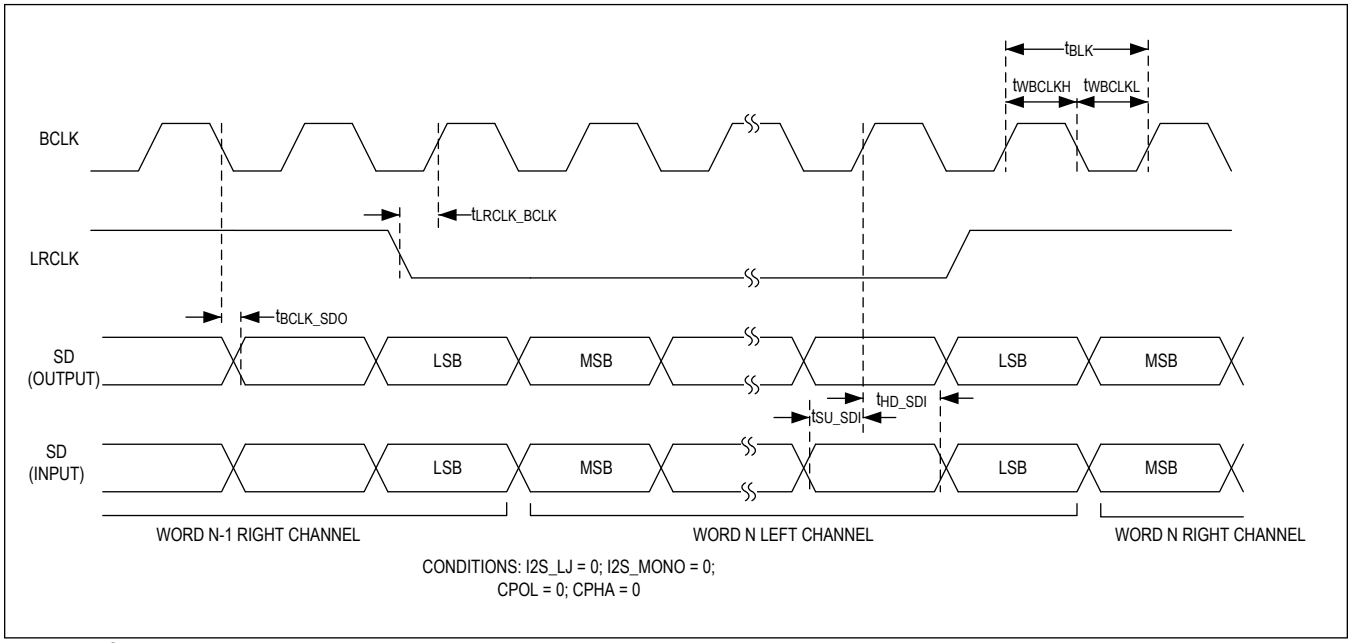


Figure 4. I²S Timing Diagram

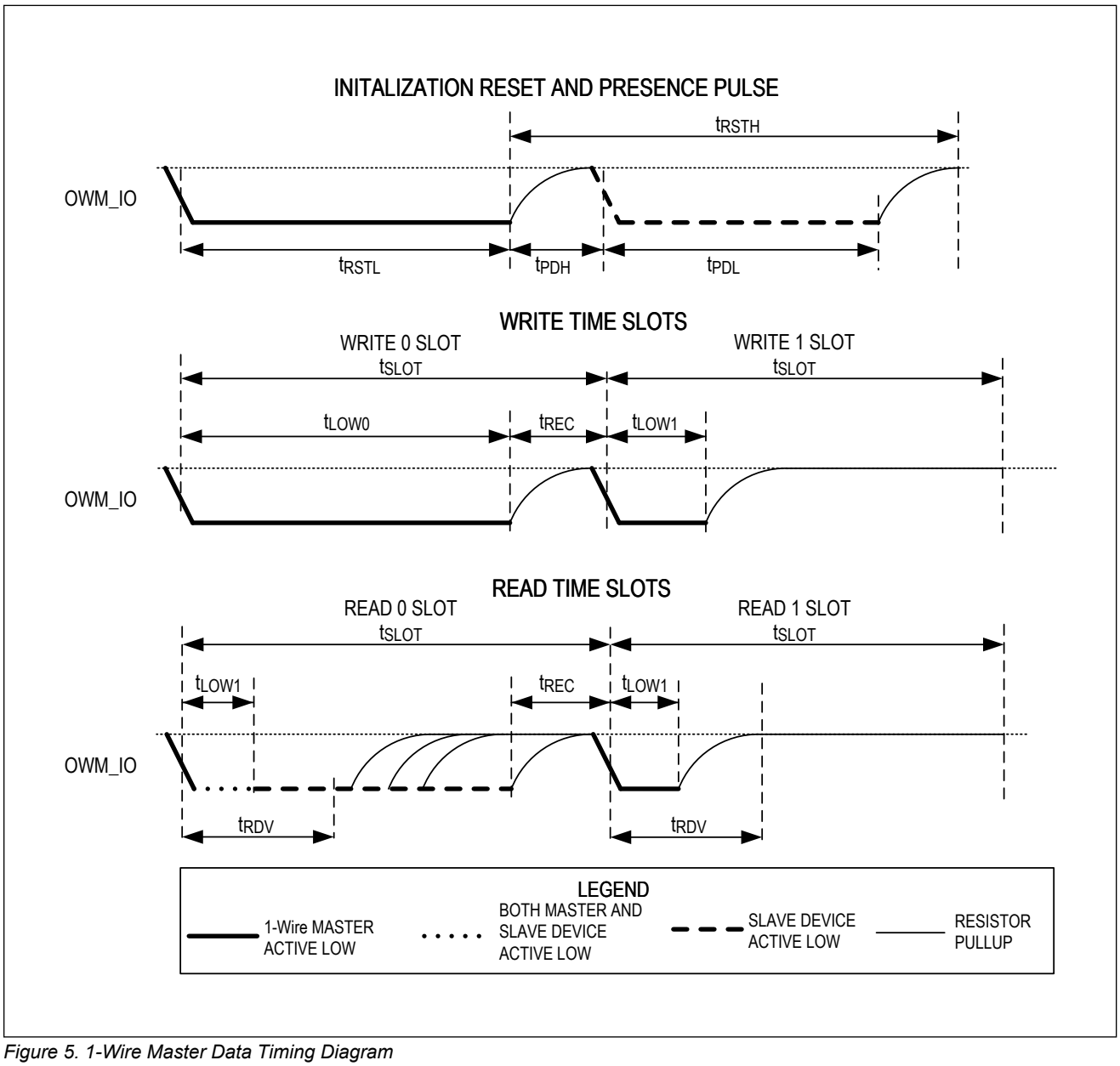
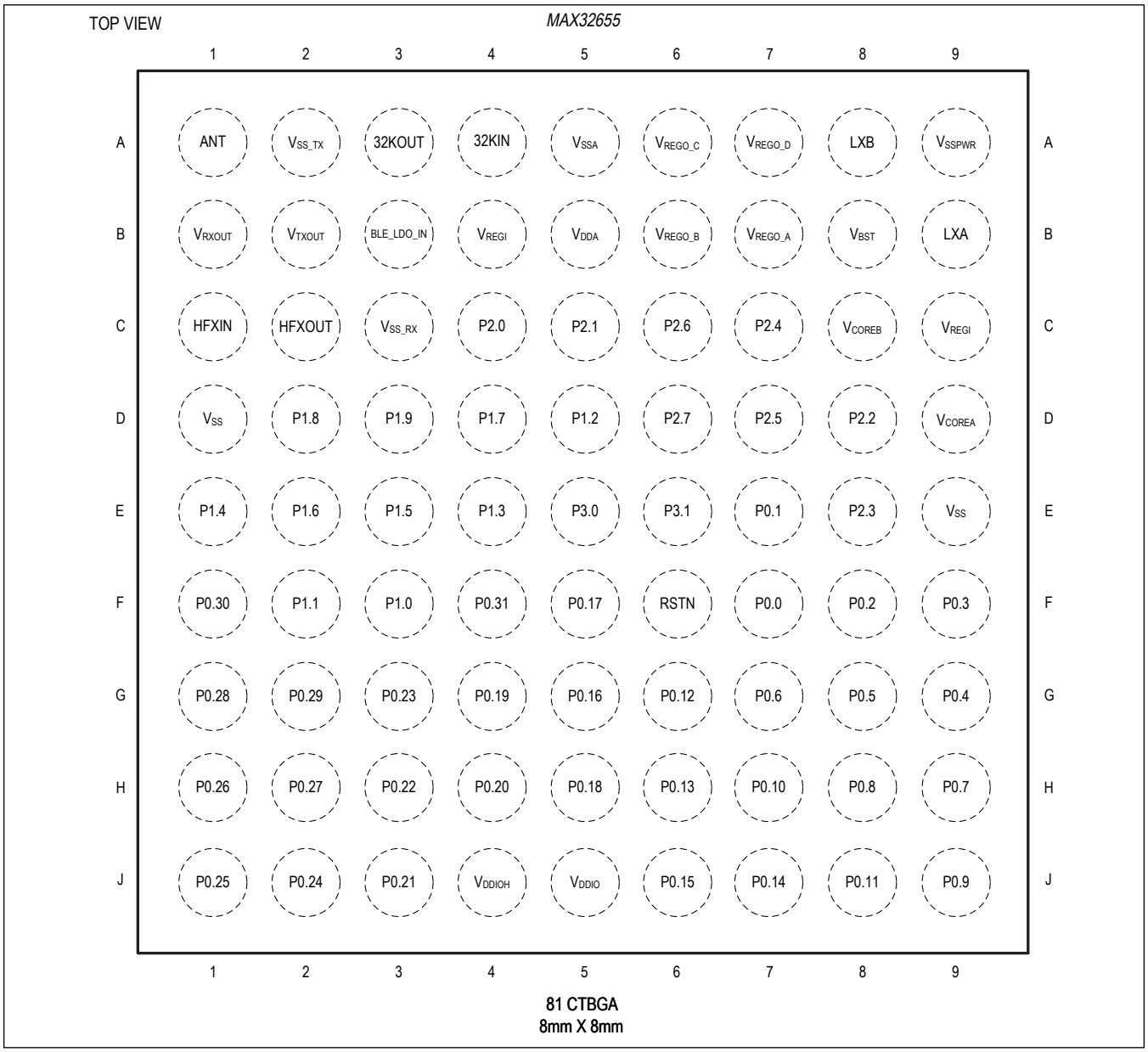


Figure 5. 1-Wire Master Data Timing Diagram

Pin Configuration

81 CTBGA



Pin Descriptions – 81 CTBGA

PIN	NAME	FUNCTION MODE			FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	
POWER (See the *Applications Information* section for bypass capacitor recommendations.)					
C9, B4	V_{REGI}	—	—	—	Battery Power Supply for the SIMO Switch-Mode Power Supply (SMPS). Bypass device pin C9 with 2 x 47µF capacitors placed as close as possible to the device pin C9 and V_{SSPWR} pins for applications using a coin cell as the battery. See *Bypass Capacitors* for more information. If power to the device is cycled, the voltage applied to this device pin must reach V_{REGI} (rising).
B3	BLE_LDO_IN	—	—	—	Bluetooth LDO Input. Bypass BLE_LDO_IN with a 100nF capacitor to V_{SS} placed as close as possible to the BLE_LDO_IN device pin.
B5	V_{DDA}	—	—	—	1.8V Analog Power Supply
D9	V_{COREA}	—	—	—	Digital Core Supply Voltage A
C8	V_{COREB}	—	—	—	Digital Core Supply Voltage B
B1	V_{RXOUT}	—	—	—	Radio Receiver Supply Voltage Output. Bypass this pin to V_{SS_RX} with a 1.0µF capacitor placed as close as possible to the package.
B2	V_{TXOUT}	—	—	—	Radio Transmitter Supply Voltage Output. Bypass this pin to V_{SS_TX} with a 1.0µF capacitor placed as close as possible to the package.
B8	V_{BST}	—	—	—	Boosted Supply Voltage for the Gate Drive of High-Side Switches. Bypass V_{BST} to LXB with a 3.3nF capacitor.
B7	V_{REGO_A}	—	—	—	Buck Converter A Voltage Output. Bypass V_{REGO_A} with a 22µF capacitor to V_{SS} placed as close as possible to the V_{REGO_A} device pin. This capacitor should be placed on the PCB trace between the V_{REGO_A} device pin and the V_{DDA} device pin.
B6	V_{REGO_B}	—	—	—	Buck Converter B Voltage Output. Bypass V_{REGO_B} with a 22µF capacitor to V_{SS} placed as close as possible to the V_{REGO_B} device pin.This capacitor should be placed on the PCB trace between the V_{REGO_B} device pin and the closest V_{COREB} device pin.
A6	V_{REGO_C}	—	—	—	Buck Converter C Voltage Output. Bypass V_{REGO_C} with a 22µF capacitor to V_{SS} placed as close as possible to the V_{REGO_C} device pin. This capacitor should be placed on the PCB trace between the V_{REGO_C} device pin and the closest V_{COREA} device pin.

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PIN	NAME	FUNCTION MODE			FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	
A7	V_{REGO_D}	—	—	—	Buck Converter D Voltage Output. Bypass V_{REGO_D} with a 22µF capacitor to V_{SS} placed as close as possible to the V_{REGO_D} device pin. This capacitor should be placed on the PCB trace between the V_{REGO_D} device pin and the BLE_LDO_IN device pin.
J5	V_{DDIO}	—	—	—	GPIO Supply Voltage. Bypass this pin to V_{SS} with a 1.0µF capacitor placed as close as possible to the package.
J4	V_{DDIOH}	—	—	—	GPIO Supply Voltage, High. $V_{DDIOH} \geq V_{DDIO}$. Bypass this pin to V_{SS} with a 1.0µF capacitor placed as close as possible to the package.
D1, E9	V_{SS}	—	—	—	Digital Ground
A5	V_{SSA}	—	—	—	Analog Ground
A9	V_{SSPWR}	—	—	—	Ground for the SIMO SMPS. This device pin is the return path for V_{REGI} device pins C6 and C9.
C3	V_{SS_RX}	—	—	—	Bluetooth Receiver Ground
A2	V_{SS_TX}	—	—	—	Bluetooth Transmitter Ground
B9	LXA	—	—	—	Switching Inductor Input A. Connect a 2.2µH inductor between LXA and LXB.
A8	LXB	—	—	—	Switching Inductor Input B. Connect a 2.2µH inductor between LXA and LXB.
RESET AND CONTROL					
F6	RSTN	—	—	—	Active-Low, External System Reset Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR (resetting all logic on all supplies except for real-time clock circuitry) and begins execution. This pin has an internal pullup to the V_{DDIOH} supply.
CLOCK					
A3	32KOUT	—	—	—	32kHz Crystal Oscillator Output
A4	32KIN	—	—	—	32kHz Crystal Oscillator Input. Connect a 32kHz crystal between 32KIN and 32KOUT for RTC operation. Optionally, this pin can be configured as the input for an external CMOS-level clock source.
C2	HFXOUT	—	—	—	32MHz Crystal Oscillator Output
C1	HFXIN	—	—	—	32MHz Crystal Oscillator Input. Connect a 32MHz crystal between HFXIN and HFXOUT for Bluetooth operation. Optionally, this pin can be configured as the input for an external CMOS-level clock source.
GPIO AND ALTERNATE FUNCTION					
F7	P0.0	P0.0	UART0A_RX	—	UART0 Receive Port Map A

81 CTBGA

PIN	NAME	FUNCTION MODE			FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	
E7	P0.1	P0.1	UART0A_TX	—	UART0 Transmit Port Map A
F8	P0.2	P0.2	TMR0A_IOA	UART0B_CTS	Timer 0 I/O 32 Bits or Lower 16 Bits Port Map A; UART0 Clear to Send Port Map B
F9	P0.3	P0.3	EXT_CLK/ TMR0A_IOB	UART0B_RTS	External Clock for Use as SYS_OSC/Timer 0 I/O Upper 16 Bits Port Map A; UART0 Request to Send Port Map B
G9	P0.4	P0.4	SPI0_SS0	TMR0B_IOAN	SPI0 Slave Select 0; Timer 0 Inverted Output Port Map B
G8	P0.5	P0.5	SPI0_MOSI	TMR0B_IOBN	SP0 Master Out Slave In Serial Data 0; 32-bit Timer 0 Inverted Output Upper 16 Bits Port Map B
G7	P0.6	P0.6	SPI0_MISO	OWM_IO	SPI0 Master In Slave Out Serial Data 1; 1-Wire Master Data I/O
H9	P0.7	P0.7	SPI0_SCK	OWM_PE	SPI0 Clock; 1-Wire Master Pullup Enable Output
H8	P0.8	P0.8	SPI0_SDIO2	TMR0B_IOA	SPI0 Data 2 I/O; Timer 0 I/O 32 Bits or Lower 16 Bits Port Map B
J9	P0.9	P0.9	SPI0_SDIO3	TMR0B_IOB	SPI0 Data 3 I/O; Timer 0 I/O Upper 16 Bits Port Map B
H7	P0.10	P0.10	I2C0_SCL	SPI0_SS2	I2C0 Clock; SPI0 Slave Select 2
J8	P0.11	P0.11	I2C0_SDA	SPI0_SS1	I2C0 Serial Data; SPI0 Slave Select 1
G6	P0.12	P0.12	UART1A_RX	TMR1B_IOAN	UART1 Receive Port Map A; Timer 1 Inverted Output Port Map B
H6	P0.13	P0.13	UART1A_TX	TMR1B_IOBN	UART1 Transmit Port Map A; Timer 1 Inverted Output Upper 16 Bits Port Map B
J7	P0.14	P0.14	TMR1A_IOA	UART1B_CTS	Timer 1 I/O 32 Bits or Lower 16 Bits Port Map A; UART1 Clear to Send Port Map B
J6	P0.15	P0.15	TMR1A_IOB	UART1B_RTS	Timer 1 I/O Upper 16 Bits Port Map A; UART1 Request to Send Port Map B
G5	P0.16	P0.16	I2C1_SCL	PT2	I2C1 Clock; Pulse Train 2
F5	P0.17	P0.17	I2C1_SDA	PT3	I2C1 Serial Data; Pulse Train 3
H5	P0.18	P0.18	PT0	OWM_IO	Pulse Train 0; 1-Wire Master Data I/O
G4	P0.19	P0.19	PT1	OWM_PE	Pulse Train 1; 1-Wire Master Pullup Enable Output
H4	P0.20	P0.20	SPI1_SS0	TMR1B_IOA	SPI1 Slave Select 0; Timer 1 I/O 32 Bits or Lower 16 Bits Port Map B
J3	P0.21	P0.21	SPI1_MOSI	TMR1B_IOB	SPI1_Master Out Slave In Serial Data 0; Timer 1 I/O Upper 16 Bits Port Map B
H3	P0.22	P0.22	SPI1_MISO	TMR1B_IOAN	SPI1 Master In Slave Out Serial Data 1; Timer 1 Inverted Output Port Map B
G3	P0.23	P0.23	SPI1_SCK	TMR1B_IOBN	SPI1 Clock; Timer 1 Inverted Output Upper 16 Bits Port Map B
J2	P0.24	P0.24	SPI1_SDIO2	TMR2B_IOA	SPI1 Data 2; Timer 2 I/O 32 Bits or Lower 16 Bits Port Map B

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PIN	NAME	FUNCTION MODE			FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	
J1	P0.25	P0.25	SPI1_SDIO3	TMR2B_IOB	SPI1 Data 3; Timer 2 I/O Upper 16 Bits Port Map B
H1	P0.26	P0.26	TMR2A_IOA	SPI1_SS1	Timer 2 I/O 32 Bits or Lower 16 Bits Port Map A; SPI1 Slave Select 1
H2	P0.27	P0.27	TMR2A_IOB	SPI1_SS2	Timer 2 I/O Upper 16 Bits Port Map A; SPI1 Slave Select 2
G1	P0.28	P0.28	SWDIO	—	Serial Wire Debug Data I/O
G2	P0.29	P0.29	SWCLK	—	Serial Wire Debug Clock
F1	P0.30	P0.30	I2C2_SCL	UART2B_CTS	I2C2 Clock; UART2 Clear to Send Port Map B
F4	P0.31	P0.31	I2C2_SDA	UART2B_RTS	I2C2 Serial Data; UART2 Request to Send Port Map B
F3	P1.0	P1.0	UART2A_RX	RV_TCK	UART2 Receive Port Map A; 32-Bit RISC-V Test Port Clock
F2	P1.1	P1.1	UART2A_TX	RV_TMS	UART2 Transmit Port Map A; 32-Bit RISC-V Test Port Select
D5	P1.2	P1.2	I2S_SCK	RV_TDI	I^2S Bit Clock; 32-Bit RISC-V Test Port Data Input
E4	P1.3	P1.3	I2S_WS	RV_TDO	I^2S Left/Right Clock; 32-Bit RISC-V Test Port Data Output
E1	P1.4	P1.4	I2S_SDI	TMR3B_IOA	I^2S Serial Data Input; Timer 3 I/O 32 Bits or Lower 16 Bits Port Map B
E3	P1.5	P1.5	I2S_SDO	TMR3B_IOB	I^2S Serial Data Output; Timer 3 I/O Upper 16 Bits Port Map B
E2	P1.6	P1.6	TMR3A_IOA	BLE_ANT_CTRL2	Timer 3 I/O 32 Bits or Lower 16 Bits Port Map A; Bluetooth Antenna Control Line 2
D4	P1.7	P1.7	TMR3A_IOB	BLE_ANT_CTRL3	Timer 3 I/O Upper 16 Bits Port Map A; Bluetooth Antenna Control Line 3
D2	P1.8	P1.8	BLE_ANT_CTRL0	RXEV0	Bluetooth Antenna Control Line 0; CM4 Rx Event Input
D3	P1.9	P1.9	BLE_ANT_CTRL1	TXEV0	Bluetooth Antenna Control Line 1; CM4 Tx Event Output
C4	P2.0	P2.0	AIN0/AIN0N	—	Analog-to-Digital Converter Input 0/Comparator 0 Negative Input
C5	P2.1	P2.1	AIN1/AIN0P	—	Analog-to-Digital Converter Input 1/Comparator 0 Positive Input
D8	P2.2	P2.2	AIN2/AIN1N	—	Analog-to-Digital Converter Input 2/Comparator 1 Negative Input
E8	P2.3	P2.3	AIN3/AIN1P	—	Analog-to-Digital Converter Input 3/Comparator 1 Positive Input
C7	P2.4	P2.4	AIN4/AIN2N	LPTMR0B_IOA	Analog-to-Digital Converter Input 4/Comparator 2 Negative Input; Low-Power Timer 0 I/O Port Map B
D7	P2.5	P2.5	AIN5/AIN2P	LPTMR1B_IOA	Analog-to-Digital Converter Input 5/Comparator 2 Positive Input; Low-Power Timer 1 I/O Port Map B

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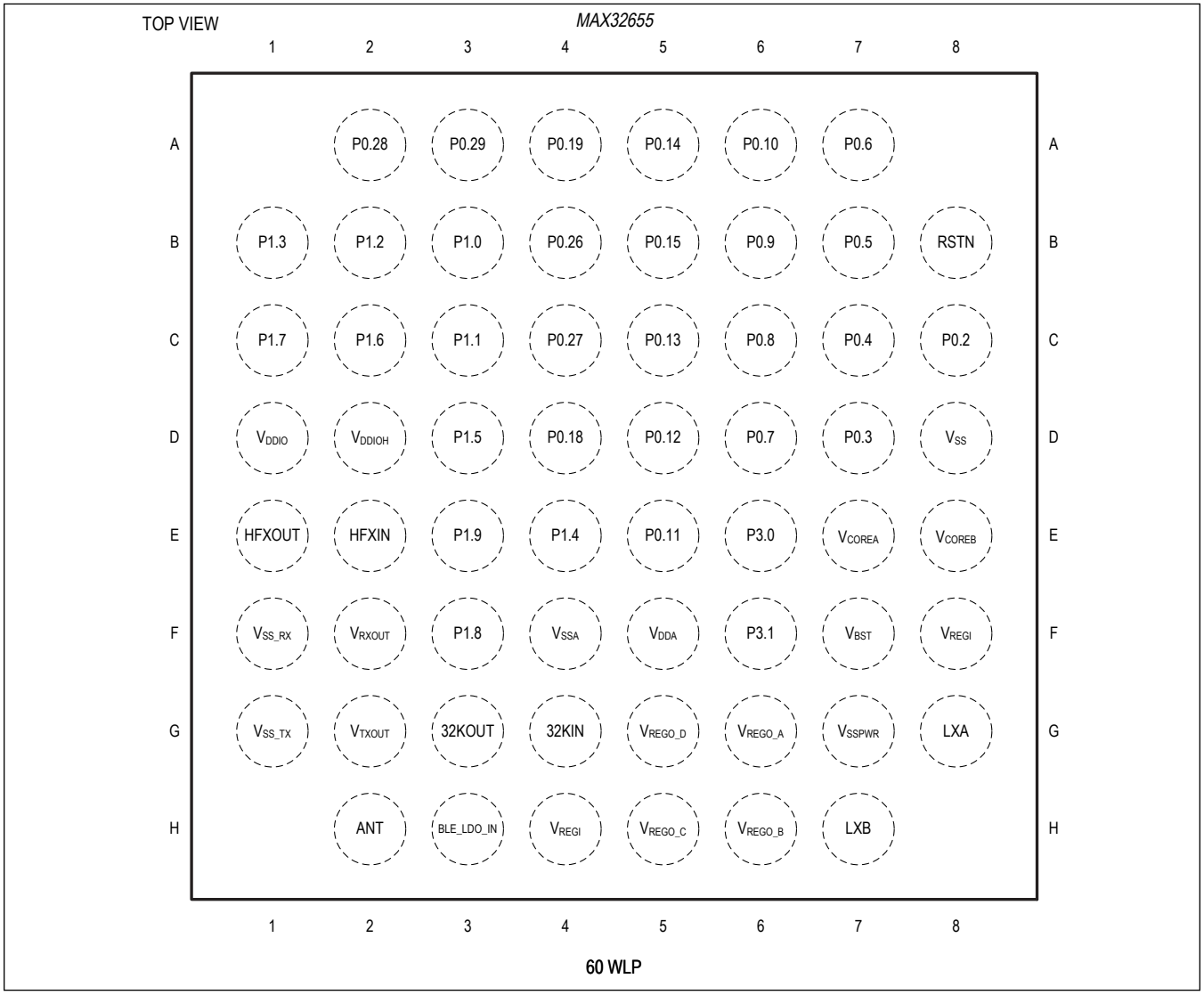
PIN	NAME	FUNCTION MODE			FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	
C6	P2.6	P2.6	LPTMR0_CLK/ AIN6/AIN3N	LPUARTB_RX	Low-Power Timer 0 External Clock Input/ Analog-to-Digital Converter Input 6/Comparator 3 Negative Input; Low-Power UART 0 Receive Port Map B
D6	P2.7	P2.7	LPTMR1_CLK/ AIN7/AIN3P	LPUARTB_TX	Low-Power Timer 1 External Clock Input/ Analog-to-Digital Converter Input 7/Comparator 3 Positive Input; Low-Power UART Transmit Port Map B
E5	P3.0	P3.0	PDOWN	WAKEUP	Power-Down Output; Wakeup Input. This device pin can only be powered by V_{DDIOH}.
E6	P3.1	P3.1	SQWOUT	WAKEUP	Square-Wave Output; Wakeup Input. This device pin can only be powered by V_{DDIOH}.
ANTENNA OUTPUT					
A1	ANT	—	—	—	Antenna for Bluetooth Radio. Attach the single-ended, unbalanced Bluetooth radio antenna.

Pin Configuration

60 WLP



Pin Descriptions – 60 WLP

PIN	NAME	FUNCTION MODE			FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	
POWER (See the *Applications Information* section for bypass capacitor recommendations.)					
F8, H4	V_{REGI}	—	—	—	Battery Power Supply for the SIMO Switch-Mode Power Supply (SMPS). Bypass device pin H4 with 2 x 47µF capacitors placed as close as possible to the device pin H4 and V_{SSPWR} pins for applications using a coin cell as the battery. See *Bypass Capacitors* for more information. If power to the device is cycled, the voltage applied to this device pin must reach V_{REGI} (rising).
H3	BLE_LDO_IN	—	—	—	Bluetooth LDO Input. Bypass BLE_LDO_IN with a 100nF capacitor to V_{SS} placed as close as possible to the BLE_LDO_IN device pin.
F5	V_{DDA}	—	—	—	1.8V Analog Power Supply
E7	V_{COREA}	—	—	—	Digital Core Supply Voltage A
E8	V_{COREB}	—	—	—	Digital Core Supply Voltage B
F2	V_{RXOUT}	—	—	—	Radio Receiver Supply Voltage Output. Bypass this pin to V_{SS_RX} with a 1.0µF capacitor placed as close as possible to the package.
G2	V_{TXOUT}	—	—	—	Radio Transmitter Supply Voltage Output. Bypass this pin to V_{SS_TX} with a 1.0µF capacitor placed as close as possible to the package.
F7	V_{BST}	—	—	—	Boosted Supply Voltage for the Gate Drive of High-Side Switches. Bypass V_{BST} to LXB with a 3.3nF capacitor.
G6	V_{REGO_A}	—	—	—	Buck Converter A Voltage Output. Bypass V_{REGO_A} with a 22µF capacitor to V_{SS} placed as close as possible to the V_{REGO_A} device pin. This capacitor should be placed on the PCB trace between the V_{REGO_A} device pin and the V_{DDA} device pin.
H6	V_{REGO_B}	—	—	—	Buck Converter B Voltage Output. Bypass V_{REGO_B} with a 22µF capacitor to V_{SS} placed as close as possible to the V_{REGO_B} device pin.This capacitor should be placed on the PCB trace between the V_{REGO_B} device pin and the closest V_{COREB} device pin.
H5	V_{REGO_C}	—	—	—	Buck Converter C Voltage Output. Bypass V_{REGO_C} with a 22µF capacitor to V_{SS} placed as close as possible to the V_{REGO_C} device pin. This capacitor should be placed on the PCB trace between the V_{REGO_C} device pin and the closest V_{COREA} device pin.

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PIN	NAME	FUNCTION MODE			FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	
G5	V_{REGO_D}	—	—	—	Buck Converter D Voltage Output. Bypass V_{REGO_D} with a 22µF capacitor to V_{SS} placed as close as possible to the V_{REGO_D} device pin. This capacitor should be placed on the PCB trace between the V_{REGO_D} device pin and the BLE_LDO_IN device pin.
D1	V_{DDIO}	—	—	—	GPIO Supply Voltage. Bypass this pin to V_{SS} with a 1.0µF capacitor placed as close as possible to the package.
D2	V_{DDIOH}	—	—	—	GPIO Supply Voltage, High. $V_{DDIOH} \geq V_{DDIO}$. Bypass this pin to V_{SS} with a 1.0µF capacitor placed as close as possible to the package.
D8	V_{SS}	—	—	—	Digital Ground
F4	V_{SSA}	—	—	—	Analog Ground
G7	V_{SSPWR}	—	—	—	Ground for the SIMO SMPS. This device pin is the return path for V_{REGI} device pins C6 and C9.
F1	V_{SS_RX}	—	—	—	Bluetooth Receiver Ground
G1	V_{SS_TX}	—	—	—	Bluetooth Transmitter Ground
G8	LXA	—	—	—	Switching Inductor Input A. Connect a 2.2µH inductor between LXA and LXB.
H7	LXB	—	—	—	Switching Inductor Input B. Connect a 2.2µH inductor between LXA and LXB.
RESET AND CONTROL					
B8	RSTN	—	—	—	Active-Low, External System Reset Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR (resetting all logic on all supplies except for real-time clock circuitry) and begins execution. This pin has an internal pullup to the V_{DDIOH} supply.
CLOCK					
G3	32KOUT	—	—	—	32kHz Crystal Oscillator Output
G4	32KIN	—	—	—	32kHz Crystal Oscillator Input. Connect a 32kHz crystal between 32KIN and 32KOUT for RTC operation. Optionally, this pin can be configured as the input for an external CMOS-level clock source.
E1	HFXOUT	—	—	—	32MHz Crystal Oscillator Output
E2	HFXIN	—	—	—	32MHz Crystal Oscillator Input. Connect a 32MHz crystal between HFXIN and HFXOUT for Bluetooth operation. Optionally, this pin can be configured as the input for an external CMOS-level clock source.

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PIN	NAME	FUNCTION MODE			FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	
GPIO AND ALTERNATE FUNCTION (See the *Applications Information* section for GPIO and Alternate Function Matrices.)					
C8	P0.2	P0.2	TMR0A_IOA	UART0B_CTS	Timer 0 I/O 32 Bits or Lower 16 Bits Port Map A; UART0 Clear to Send Port Map B
D7	P0.3	P0.3	EXT_CLK/ TMR0A_IOB	UART0B_RTS	External Clock for Use as SYS_OSC/Timer 0 I/O Upper 16 Bits Port Map A; UART0 Request to Send Port Map B
C7	P0.4	P0.4	SPI0_SS0	TMR0B_IOAN	SPI0 Slave Select 0; Timer 0 Inverted Output Port Map B
B7	P0.5	P0.5	SPI0_MOSI	TMR0B_IOBN	SP0 Master Out Slave In Serial Data 0; 32-Bit Timer 0 Inverted Output Upper 16 Bits Port Map B
A7	P0.6	P0.6	SPI0_MISO	OWM_IO	SPI0 Master In Slave Out Serial Data 1; 1-Wire Master Data I/O
D6	P0.7	P0.7	SPI0_SCK	OWM_PE	SPI0 Clock; 1-Wire Master Pullup Enable Output
C6	P0.8	P0.8	SPI0_SDIO2	TMR0B_IOA	SPI0 Data 2 I/O; Timer 0 I/O 32 Bits or Lower 16 Bits Port Map B
B6	P0.9	P0.9	SPI0_SDIO3	TMR0B_IOB	SPI0 Data 3 I/O; Timer 0 I/O Upper 16 Bits Port Map B
A6	P0.10	P0.10	I2C0_SCL	SPI0_SS2	I2C0 Clock; SPI0 Slave Select 2
E5	P0.11	P0.11	I2C0_SDA	SPI0_SS1	I2C0 Serial Data; SPI0 Slave Select 1
D5	P0.12	P0.12	UART1A_RX	TMR1B_IOAN	UART1 Receive Port Map A; Timer 1 Inverted Output Port Map B
C5	P0.13	P0.13	UART1A_TX	TMR1B_IOBN	UART1 Transmit Port Map A; Timer 1 Inverted Output Upper 16 Bits Port Map B
A5	P0.14	P0.14	TMR1A_IOA	UART1B_CTS	Timer 1 I/O 32 Bits or Lower 16 Bits Port Map A; UART1 Clear to Send Port Map B
B5	P0.15	P0.15	TMR1A_IOB	UART1B_RTS	Timer 1 I/O Upper 16 Bits Port Map A; UART1 Request to Send Port Map B
D4	P0.18	P0.18	PT0	OWM_IO	Pulse Train 0; 1-Wire Master Data I/O
A4	P0.19	P0.19	PT1	OWM_PE	Pulse Train 1; 1-Wire Master Pullup Enable Output
B4	P0.26	P0.26	TMR2A_IOA	SPI1_SS1	Timer 2 I/O 32 Bits or Lower 16 Bits Port Map A; SPI1 Slave Select 1
C4	P0.27	P0.27	TMR2A_IOB	SPI1_SS2	Timer 2 I/O Upper 16 Bits Port Map A; SPI1 Slave Select 2
A2	P0.28	P0.28	SWDIO	—	Serial Wire Debug Data I/O
A3	P0.29	P0.29	SWCLK	—	Serial Wire Debug Clock
B3	P1.0	P1.0	UART2A_RX	RV_TCK	UART2 Receive Port Map A; 32-Bit RISC-V Test Port Clock
C3	P1.1	P1.1	UART2A_TX	RV_TMS	UART2 Transmit Port Map A; 32-Bit RISC-V Test Port Select
B2	P1.2	P1.2	I2S_SCK	RV_TDI	I^2S Bit Clock; 32-Bit RISC-V Test Port Data Input

60 WLP

PIN	NAME	FUNCTION MODE			FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	
B1	P1.3	P1.3	I2S_WS	RV_TDO	I^2S Left/Right Clock; 32-Bit RISC-V Test Port Data Output
E4	P1.4	P1.4	I2S_SDI	TMR3B_IOA	I^2S Serial Data Input; Timer 3 I/O 32 Bits or Lower 16 Bits Port Map B
D3	P1.5	P1.5	I2S_SDO	TMR3B_IOB	I^2S Serial Data Output; Timer 3 I/O Upper 16 Bits Port Map B
C2	P1.6	P1.6	TMR3A_IOA	BLE_ANT_CTRL2	Timer 3 I/O 32 Bits or Lower 16 Bits Port Map A; Bluetooth Antenna Control Line 2
C1	P1.7	P1.7	TMR3A_IOB	BLE_ANT_CTRL3	Timer 3 I/O Upper 16 Bits Port Map A; Bluetooth Antenna Control Line 3
F3	P1.8	P1.8	BLE_ANT_CTRL0	RXEV0	Bluetooth Antenna Control Line 0; CM4 Rx Event Input
E3	P1.9	P1.9	BLE_ANT_CTRL1	TXEV0	Bluetooth Antenna Control Line 1; CM4 Tx Event Output
E6	P3.0	P3.0	PDOWN	WAKEUP	Power-Down Output; Wakeup Input. This device pin can only be powered by V_{DDIOH}.
F6	P3.1	P3.1	SQWOUT	WAKEUP	Square-Wave Output; Wakeup Input. This device pin can only be powered by V_{DDIOH}.
ANTENNA OUTPUT					
H2	ANT	—	—	—	Antenna for Bluetooth Radio. Attach the single-ended, unbalanced Bluetooth radio antenna.

Detailed Description

The MAX32655 MCU is an advanced system-on-chip featuring an Arm Cortex-M4F CPU for efficient computation of complex functions and algorithms qualified to operate at a temperature range of -40°C to +105°C. The SoC integrates power regulation and management with a SIMO buck regulator system. On board is the latest generation Bluetooth 5.2 LE radio, supporting LE Audio, AoA, and AoD for direction finding, long-range (coded), and high-throughput modes. The device offers large onboard memory with 512KB flash and 128KB SRAM, with optional error correction coding on one 32K SRAM bank. This 32KB bank can be optionally retained in BACKUP mode. An 8KB user OTP area is available, of which 8 bytes are retained, even during POWER DOWN mode. Many high-speed interfaces are supported on the device, including SPI, UART, and I^2C serial interfaces, plus one I^2S port for connecting to an audio codec. Additional low-power peripherals include flexible LPTIMER, LPUART, and analog comparators. An eight-input, 10-bit ADC is available to monitor analog input from external analog sources.

Arm Cortex-M4 (CM4) with FPU Processor and RISC-V (RV32) Processor

The Arm Cortex-M4 with FPU processor is ideal for low-power system control. The architecture combines high-efficiency signal processing functionality with low power, low cost, and ease of use.

The Arm Cortex-M4 with FPU DSP supports single instruction multiple data (SIMD) path DSP extensions, providing:

- Four parallel 8-bit add/sub
- Floating-point single precision
- Two parallel 16-bit add/sub
- Two parallel MACs
- 32- or 64-bit accumulate
- Signed and unsigned data with or without saturation

The addition of 32-bit RISC-V processor (RV32) provides the system with ultra-low-power consumption signal processing.

Memory

Internal Flash Memory

512KB of internal flash memory provides nonvolatile storage of program and data memory.

Internal SRAM

The internal 128KB SRAM provides low-power retention of application information in all power modes except POWER DOWN. The SRAM is divided into four banks. SRAM0 and SRAM1 are both 32KB, SRAM2 is 48KB, and SRAM3 is 16KB. SRAM2 and SRAM3 are accessible by the RV32 in LOW POWER mode. For enhanced system reliability, SRAM0 (32KB) can be configured with error correction coded (ECC), single error correction-double error detection (SED-DED). This data retention feature is optional and configurable. This granularity allows the application to minimize its power consumption by only retaining the most essential data.

Bluetooth 5.2

Bluetooth 5.2 Low Energy Radio

Bluetooth 5.2 LE is the latest version of the Bluetooth wireless communication standard. It is used for wireless headphones and other audio hardware, as well as for communication between various smart home and internet of things (IoT) devices. Bluetooth LE communications operate in the unlicensed 2.4GHz industrial-scientific-medical (ISM) band. A frequency-hopping transceiver is used to combat interference and fading. The system operates in the 2.4GHz ISM band at 2400MHz to 2483.5MHz. It uses 40 RF channels. These RF channels have center frequencies 2402 + k x 2MHz, where k = 0, ..., 39. The Bluetooth stack runs on RV32 so that the CM4 can be freed to run application code. The features of the radio include the following:

- Higher transmit power up to +4.5dbm
- 1Mbps, 2Mbps, and long-range coded (125kbps and 500kbps)

- Increased broadcast capability
  - Advertising packet up to 255 bytes
- On-chip matching network to the antenna
- Antenna control outputs
- Direction finding with AoA and AoD
- Provides hardware on-the-fly encryption and decryption for lower power consumption
- Low transmit current of 4.17mA at 0dbm at 3.3V
- Low receive current of 4.0mA at 3.3V
- Supports mesh networking
- Supports high-quality audio streaming (isochronous)

Bluetooth 5.2 Software Stack

A Bluetooth 5.2 software stack is available for application developers to quickly add support to devices. The Arm Cordio®-B50 software stack is provided in library form and provides application developers access to Bluetooth technology without validation and development of a software stack. The Cordio-B50 software stack interfaces to the Bluetooth link layer running on dedicated hardware. The dedicated hardware for the stack enables the ultimate in power management for IoT applications. Cordio-B50 features the following:

- C library for linking directly into an application development tool
- Change PHY support
  - Host selects the PHY it needs to use at any given time enabling long range or higher bandwidth only when required
    - Bluetooth LE 1M
    - Bluetooth LE Coded S = 2
    - Bluetooth LE Coded S = 8
    - Bluetooth LE 2M
- Bluetooth 5.2 advertising extension support for enabling next-generation Bluetooth beacons
  - Larger packets and advertising channel offloading
  - Packets up to 255 octets long
  - Advertising packet chaining
  - Advertising sets
  - Periodic advertising
  - High-duty cycle non-connectable advertising
  - Sample applications using standard profiles built on the Cordio-B50 software framework

Comparators

The eight AIN[7:0] inputs can be configured as four pairs and deployed as four independent comparators with the following features:

- Comparison events can trigger interrupts
- Events can wake the CM4 from SLEEP, LOW POWER, MICRO POWER, STANDBY, or BACKUP operating modes
- Can be active in all power modes

See Table 1 for details of instances of the comparators.

Table 1. Comparator Instances

PACKAGE		INSTANCE
81 CTBGA	60 WLP	
Yes	No	CMP0, CMP1, CMP2, CMP3

Dynamic Voltage Scaling (DVS) Controller

The DVS controller works using the fixed high-speed oscillator and the V_{COREA} supply voltage to optimally operate the Arm core at the lowest practical voltage. The ability to adaptively adjust the voltage provides a significant reduction in dynamic power consumption.

The DVS controller provides the following features:

- DVS monitoring and adjustment functions
- Continuous monitoring with programmable monitor sample period
- Controlled transition to a programmable operating point
- Independent high and low operating limits for safe, bounded operation
- Independent high, center, and low operating range delay line monitors
- Programmable adjustment rate when an adjustment is required
- Single clock operation
- APB interface provides IP control and status access
- Interrupt capability during error

Clocking Scheme

Multiple clock sources can be selected as the system clock:

- Internal primary oscillator (IPO) at a nominal frequency of 100MHz
- Internal secondary oscillator (ISO) at a nominal frequency of 60MHz
- Configurable internal nano-ring oscillator (INRO) at 8kHz, 16kHz, or 30kHz
- External RTC oscillator at 32.768kHz (ERTCO)—external crystal required
- Internal baud rate oscillator at 7.3728MHz (IBRO)
- External square-wave clock up to 80MHz
- External RF oscillator at 32MHz (ERFO)—external crystal required

There are multiple external clock inputs:

- LPTMR0 and LPTMR1 can be clocked from unique external sources (81 CTBGA only).
- SYS_CLK can be derived from an external source.

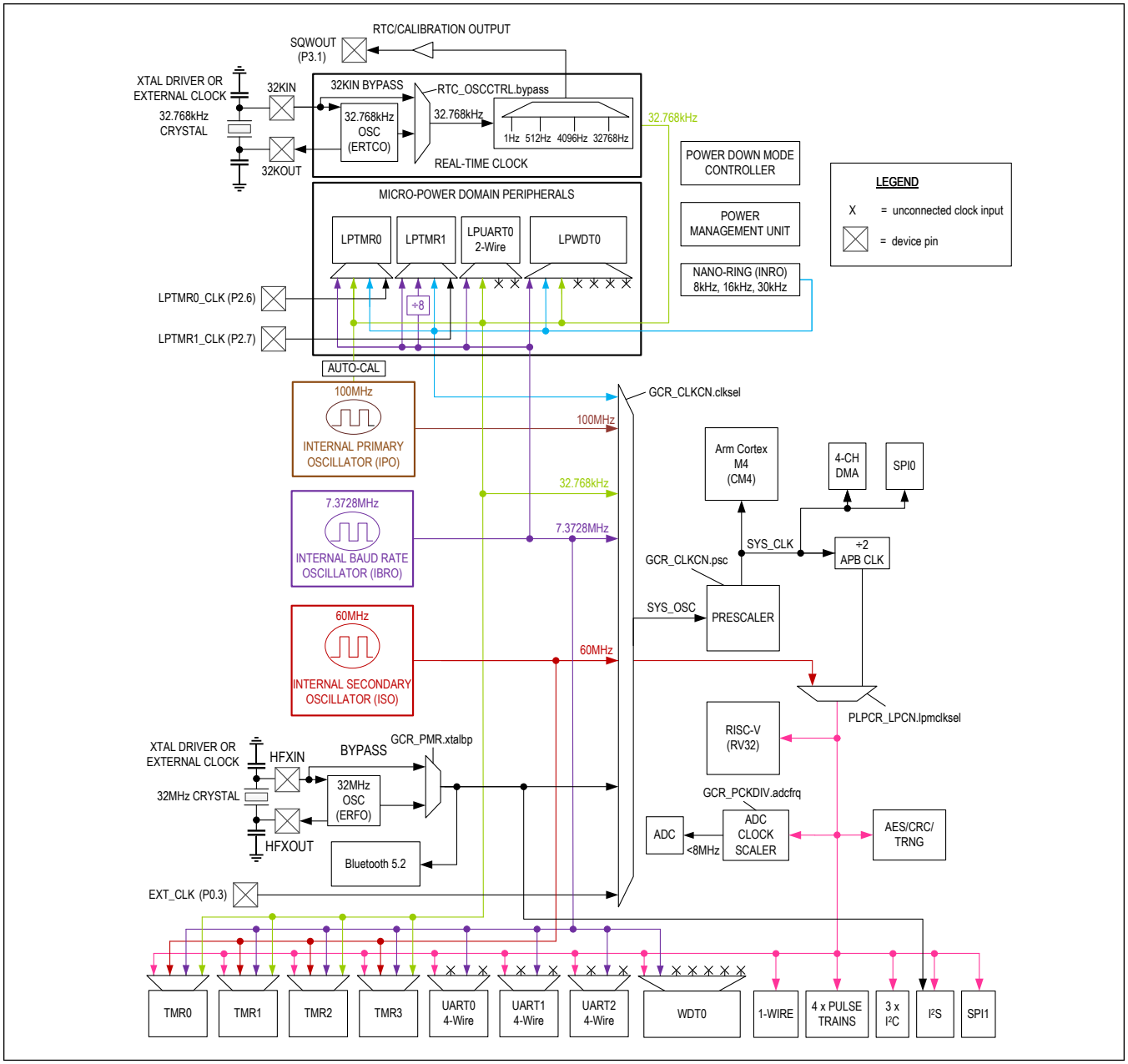

Figure 6. 81 CTBGA Clocking Scheme Diagram

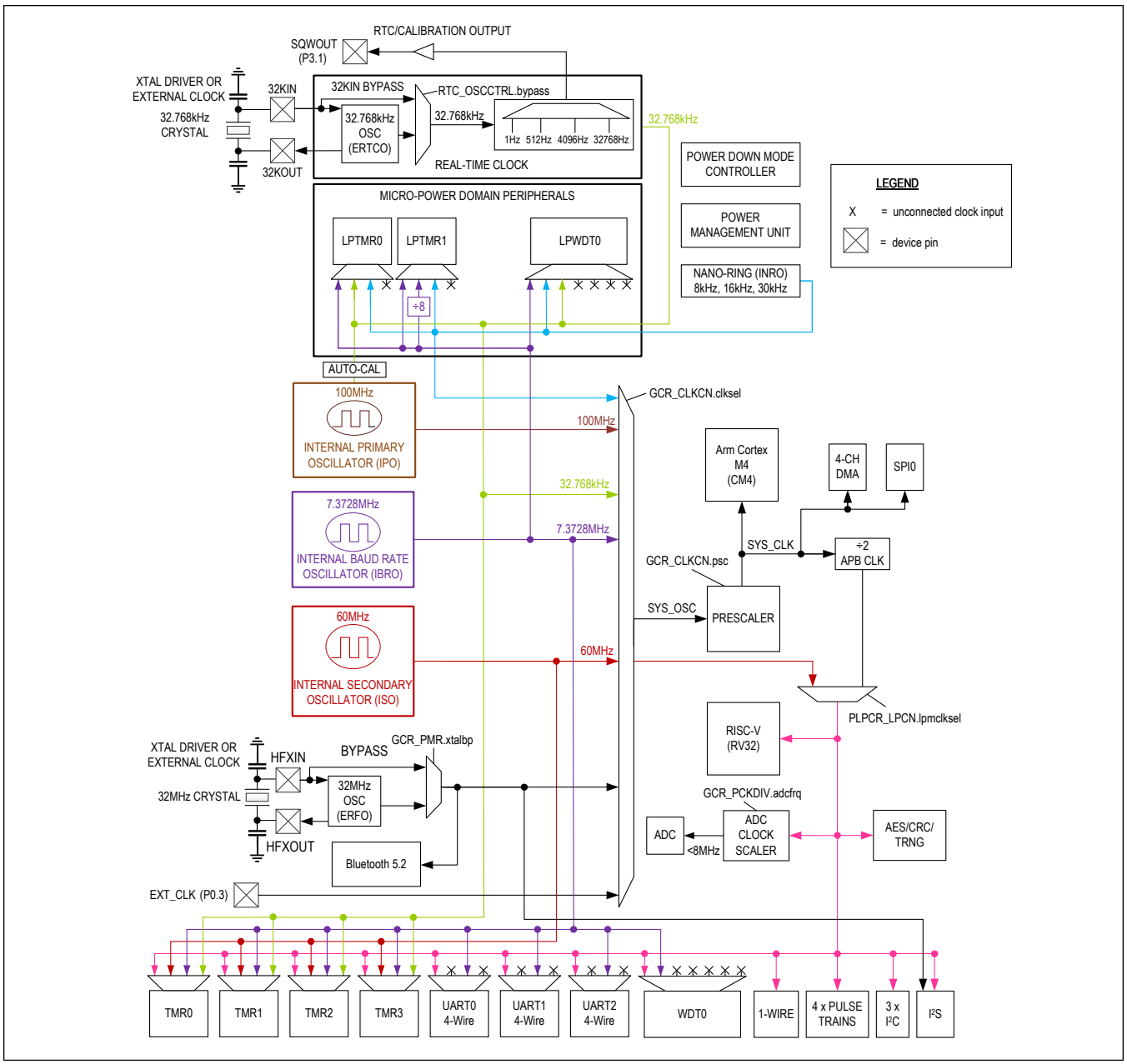

Figure 7. 60 WLP Clocking Scheme Diagram

General-Purpose I/O (GPIO) and Special Function Pins

Most GPIO pins share both a firmware-controlled I/O function and one or more alternate functions associated with peripheral modules. Pins can be individually enabled for GPIO or peripheral special function use. Configuring a pin as a special function usually supersedes its use as a firmware-controlled I/O. Although this multiplexing between peripheral and GPIO functions is usually static, it can also be done dynamically. The electrical characteristics of a GPIO pin are identical whether the pin is configured as an I/O or special function, except where explicitly noted in the Electrical Characteristics tables.

In GPIO mode, pins are logically divided into ports of 32 pins. Each pin of a port has an interrupt function that can be

independently enabled, and configured as a level- or edge-sensitive interrupt. All GPIOs of a given port share the same interrupt vector.

When configured as GPIO, all features can be independently enabled or disabled on a per-pin basis. The following features are provided:

- Configurable as input, output, bidirectional, or high impedance
- Optional internal pullup resistor or internal pulldown resistor when configured as input
- Exit from low-power modes on rising or falling edge
- Selectable standard- or high-drive modes

The MAX32655 provides up to 52 GPIO pins. Caution is needed since Port 3 (P3.0 and P3.1 device pins) is configured in a different manner from the above description.

Analog-to-Digital Converter (ADC)

The 10-bit sigma-delta (Σ-Δ) ADC provides an integrated reference generator and a single-ended input multiplexer. The multiplexer selects an input channel from one of the eight external analog input signals (AIN0–AIN7) or the internal power supply inputs.

The reference for the ADC can be:

- Internal 1.22V bandgap
- V_{SSA} analog supply

An optional feature allows samples captured by the ADC to be automatically compared against user-programmable high and low limits. Up to four channel limit pairs can be configured in this way. The comparison allows the ADC to trigger an interrupt (and potentially wake the CPU from a power mode) when a captured sample goes outside the preprogrammed limit range. Since this comparison is performed directly by the sample limit monitors, it can be performed even while the CPU is in SLEEP, LOW POWER or MICRO POWER mode. The eight AIN[7:0] inputs can be configured as four pairs and deployed as four independent comparators.

The ADC measures the following voltages:

- AIN[7:0] up to 3.3V
- V_{REGI}
- V_{COREA}
- V_{COREB}
- V_{DDIOH}
- V_{DDIO}
- V_{TXOUT}
- V_{RXOUT}
- V_{DDA}

See Table 2 for details of instances of the ADC.

Table 2. ADC Instances

PACKAGE		INSTANCE
81 CTBGA	60 WLP	
Yes	No	ADC0

Single-Inductor Multiple-Output (SIMO) Switch-Mode Power Supply (SMPS)

The SIMO SMPS built into the device provides a monolithic power supply architecture for operation from a single lithium cell. The SIMO provides four buck regulator outputs that are voltage programmable. This architecture optimizes power consumption efficiency of the device and minimizes the bill of materials for the circuit design since only a single inductor/capacitor pair is required.

Power Management

Power Management Unit (PMU)

The PMU provides high-performance operation while minimizing power consumption. It exercises intelligent, precise control of power distribution to the CPUs and peripheral circuitry.

The PMU provides the following features:

- User-configurable system clock
- Automatic enabling and disabling of crystal oscillators based on power mode
- Multiple power domains
- Fast wake-up of powered-down peripherals when activity detected

ACTIVE Mode

In this mode, the CM4 and the RV32 can execute application code and all digital and analog peripherals are available on demand. Dynamic clocking disables peripherals not in use, providing the optimal mix of high performance and low power consumption. The CM4 has access to all system SRAM. The RV32 has access to SRAM2 and SRAM3. Both the CM4 and the RV32 can execute from internal flash simultaneously. SRAM3 can be configured as an instruction cache for the RV32.

SLEEP Mode

This mode consumes less power, but wakes faster because the clocks can optionally be enabled.

The device status is as follows:

- CM4 is asleep
- RV32 is asleep
- Peripherals are on
- Standard DMA is available for optional use

LOW POWER Mode (LPM)

This mode is suitable for running the RV32 processor to collect and move data from enabled peripherals.

The device status is a follows:

- The CM4, SRAM0, and SRAM1 are in state retention.
- The RV32 can access the SPI, all UARTS, all timers, I^2C, 1-Wire, pulse train engines, I^2S, CRC, AES, TRNG, PCIF, and comparators, as well as SRAM2 and SRAM3. SRAM3 can be configured to operate as RV32 instruction cache
- The transition from LOW POWER mode to ACTIVE mode is faster than the transition from BACKUP mode because system initialization is not required.
- The DMA can access flash.
- IPO can be optionally powered down.
- The following oscillators are enabled:
  - IBRO
  - ERTCO
  - INRO
  - ISO
  - ERFO

MICRO POWER Mode (µPM)

This mode is used for extremely low power consumption while using a minimal set of peripherals to provide wakeup capability.

The device status is a follows:

- Both CM4 and RV32 are state retained. (System state and all SRAM is retained.)
- The GPIO pins retain their state.
- All non-MICRO POWER peripherals are state retained.
- IBRO can be optionally powered down.
- The following oscillators are powered down:

  - IPO
  - ISO
  - ERFO
- The following oscillators are enabled:
  - IBRO
  - ERTCO
  - INRO
- The following MICRO POWER mode peripherals are available for use to wake up the device:
  - LPUART0, LPUART1
  - WWDT1
  - All four low-power analog comparators

STANDBY Mode

This mode is used to maintain the system operation while keeping time with the RTC.

The device status is as follows:

- Both CM4 and RV32 are state retained. (System state and all SRAM is retained.)
- The GPIO pins retain their state.
- RTC is on.
- All peripherals are state retained.
- The following oscillators are powered down:
  - IPO
  - ISO
  - IBRO
  - ERFO
- The following oscillators are enabled:
  - ERTCO
  - INRO

BACKUP Mode

This mode is used maintain the system RAM. The device status is as follows:

- CM4 and RV32 are powered off.
- SRAM0, SRAM1, SRAM2 and SRAM3 can be configured to be state retained as per Table 3.
- All peripherals are powered off.
- The GPIO pins retain their state.
- RTC is on.
- The following oscillators are powered down:
  - IPO
  - ISO
  - IBRO
  - INRO
  - ERFO
- The following oscillators are enabled:
  - ERTCO

Table 3. BACKUP Mode SRAM Retention

RAM BLOCK	RAM SIZE
SRAM0	32KB + ECC
SRAM1	32KB
SRAM2	48KB

Table 3. BACKUP Mode SRAM Retention (continued)

SRAM3	16KB

POWER DOWN Mode (PDM)

This mode is used during product level distribution and storage.

The device status is as follows:

- The CM4 and RV32 are powered off.
- All peripherals and SRAM are powered down.
- All oscillators are powered down.
- 8 bytes of data are retained.
- Values in the flash are preserved.
- Voltage monitors are operational.

Wake-Up Sources

The sources of wake-up from the SLEEP, LOW POWER, MICRO POWER, STANDBY, BACKUP, and POWER DOWN operating modes are summarized in Table 4.

Table 4. Wake-Up Sources

OPERATING MODE	WAKE-UP SOURCE
SLEEP	Any enabled peripheral with interrupt capability; RSTN
LOW POWER (LPM)	SPI0, I^2S, I^2C, UARTs, timers, watchdog timers, wakeup timer, all comparators, RTC, GPIOs, RSTN, and RV32
MICRO POWER (µPM)	All comparators, LPUART (where available), LPTMR1, LPTIMER2, LPWDT0, RTC, wakeup timer, GPIOs, and RSTN
STANDBY	RTC, wakeup timer, GPIOs, CMP0 (where available), and RSTN
BACKUP	RTC, wakeup timer, GPIOs, CMP0 (where available), and RSTN
POWER DOWN (PDM)	P3.0, P3.1, and RSTN

Real-Time Clock (RTC)

An RTC keeps the time of day in absolute seconds. The 32-bit seconds register can count up to approximately 136 years and be translated to calendar format by application software.

The RTC provides a time-of-day alarm that is programmable to any future value between 1 second and 12 days. When configured for long intervals, the time-of-day alarm is usable as a power-saving timer, allowing the device to remain in an extremely low-power mode, but still awaken periodically to perform assigned tasks. A second independent 32-bit 1/4096 subsecond alarm is programmable with a tick resolution of 244µs. Both can be configured as recurring alarms. When enabled, either alarm can cause an interrupt or wake the device from most low-power modes.

The time base is generated by a 32.768kHz crystal or an external clock source that must meet the electrical/timing requirements in the *Electrical Characteristics* table.

The RTC calibration feature provides the ability for user software to compensate for minor variations in the RTC oscillator, crystal, temperature, and board layout. Enabling the SQWOUT alternate function outputs a timing signal derived from the RTC. External hardware can measure the frequency and adjust the RTC frequency in increments of ±127ppm with 1ppm resolution. Under most circumstances, the oscillator does not require any calibration.

Programmable Timers

32-Bit Timer/Counter/PWM (TMR, LPTMR)

General-purpose, 32-bit timers provide timing, capture/compare, or generation of pulse-width modulated (PWM) signals with minimal software interaction.

The timer provides the following features:

- 32-bit up/down autoreload
- Programmable prescaler
- PWM output generation
- Capture, compare, and capture/compare capability
- External pin multiplexed with GPIO for timer input, clock gating, or capture
- Timer output pin
- TMR0–TMR3 can be configured as two 16-bit general-purpose timers
- Timer interrupt

The MAX32655 provides six 32-bit timers (TMR0, TMR1, TMR2, TMR3, LPTMR0, and LPTMR1). LPTMR0 and LPTMR1 are capable of operation in the SLEEP, LOW POWER, and MICRO POWER modes.

I/O functionality is supported for all of the timers. Note that the function of a port can be multiplexed with other functions on the GPIO pins, so it might not be possible to use all the ports depending on the device configuration. See Table 5 for individual timer features.

Table 5. Timer Configuration Options

INSTANCE	REGISTER ACCESS NAME	SINGLE 32 BIT	DUAL 16 BIT	SINGLE 16 BIT	POWER MODE	CLOCK SOURCE						
						PCLK	ISO	IBRO	INRO	ERTCO	LPTMR0_CLK	LPTMR1_CLK
TMR0	TMR0	Yes	Yes	No	ACTIVE, SLEEP, LOW POWER	Yes	Yes	Yes	No	Yes	No	No
TMR1	TMR1	Yes	Yes	No	ACTIVE, SLEEP, LOW POWER	Yes	Yes	Yes	No	Yes	No	No
TMR2	TMR2	Yes	Yes	No	ACTIVE, SLEEP, LOW POWER	Yes	Yes	Yes	No	Yes	No	No
TMR3	TMR3	Yes	Yes	No	ACTIVE, SLEEP, LOW POWER	Yes	Yes	Yes	No	Yes	No	No
LPTMR0*	TMR4	No	No	Yes	ACTIVE, SLEEP, LOW POWER, MICRO POWER	No	No	Yes	Yes	Yes	Yes	No
LPTMR1*	TMR5	No	No	Yes	ACTIVE, SLEEP, LOW POWER, MICRO POWER	No	No	Yes	Yes	Yes	No	Yes

* Available as an internal timer only on the 60-WLP package. There is no external connection to this timer on the 60 WLP package.

Watchdog Timer (WDT)

Microcontrollers are often used in harsh environments where electrical noise and electromagnetic interference (EMI) are abundant. Without proper safeguards, these hazards can disturb device operation and corrupt program execution. One of the most effective countermeasures is the windowed WDT, which detects runaway code or system unresponsiveness.

The WDT is a 32-bit, free-running counter with a configurable prescaler. When enabled, the WDT must be periodically

reset by the application software. Failure to reset the WDT within the user-configurable timeout period indicates that the application software is not operating correctly and results in a WDT timeout. A WDT timeout can trigger an interrupt, system reset, or both. Either response forces the instruction pointer to a known good location before resuming instruction execution. The windowed timeout period feature provides more detailed monitoring of system operation, requiring the WDT to be reset within a specific window of time. See Table 6 for individual timer features.

The MAX32655 provides two instances of the watchdog timer—WDT0 and LPWDT0.

Table 6. Watchdog Timer Configuration Options

INSTANCE NAME	REGISTER ACCESS NAME	POWER MODE	CLOCK SOURCE			
			PCLK	IBRO	INRO	ERTCO
WDT0	WDT0	ACTIVE, SLEEP, LOW POWER	Yes	Yes	No	No
LPWDT0	WDT1	ACTIVE, SLEEP, LOW POWER, MICRO POWER	No	Yes	Yes	Yes

Pulse Train Engine (PT)

Multiple, independent pulse train generators can provide either a square-wave or a repeating pattern from 2 to 32 bits in length. Any single pulse train generator or any desired group of pulse train generators can be synchronized at the bit level allowing for multibit patterns. Each pulse train generator is independently configurable.

The pulse train generators provide the following features:

- Independently enabled
- Safe enable and disable for pulse trains without bit banding
- Multiple pin configurations allow for flexible layout
- Pulse trains can be started/synchronized independently or as a group
- Frequency of each enabled pulse train generator is also set separately, based on a divide down (divide by 2, divide by 4, divide by 8, and so on) of the input pulse train module clock
- Input pulse train module clock can be optionally configured to be independent from the system AHB clock
- Multiple repetition options
  - Single shot (nonrepeating pattern of 2 to 32 bits)
  - Pattern repeats a user-configurable number of times or indefinitely
  - Termination of one pulse train loop count can restart one or more other pulse trains

The pulse train engine feature is an alternate function associated with a GPIO pin. In most cases, enabling the pulse train engine function supersedes the GPIO function.

See Table 7 for details of instances of the pulse train peripheral.

Table 7. Pulse Train Instances

PACKAGE		INSTANCE
81 CTBGA	60 WLP	
Yes	Yes	PT0
Yes	Yes	PT1
Yes	No	PT2
Yes	No	PT3

Serial Peripherals

I^2C Interface (I2C)

The I^2C interface is a bidirectional, two-wire serial bus that provides a medium-speed communications network. It can

operate as a one-to-one, one-to-many, or many-to-many communications medium. This interface supports standard-mode, fast-mode, fast-mode plus, and high-speed mode I2C speeds. It provides the following features:

- Master or slave mode operation
  - Supports up to 4 different slave addresses in slave mode
- Supports standard 7-bit addressing or 10-bit addressing
- RESTART condition
- Interactive receive mode (IRXM)
- Transmitter FIFO preloading
- Support for clock stretching to allow slower slave devices to operate on higher speed busses
- Multiple transfer rates
  - Standard mode: 100kbps
  - Fast mode: 400kbps
  - Fast mode plus: 1000kbps
  - High-speed mode: 3.4Mbps
- Internal filter to reject noise spikes
- Receiver FIFO depth of 8 bytes
- Transmitter FIFO depth of 8 bytes

See Table 8 for details of the instances of the I2C peripheral.

Table 8. I2C Instances

PACKAGE		INSTANCE
81 CTBGA	60 WLP	
Yes	Yes	I2C0
Yes	No	I2C1
Yes	No	I2C2

I2S Interface (I2S)

The I2S interface is a bidirectional, four-wire serial bus that provides serial communications for codecs and audio amplifiers compliant with the I2S Bus Specification, June 5, 1996. It provides the following features:

- Master and slave mode operation
- Support for 4 channels
- 8, 16, 24, and 32-bit frames
- Receive and transmit DMA support
- Wake-up on FIFO status (full/empty/threshold)
- Pulse density modulation support for the receive channel
- Word-select polarity control
- First-bit position selection
- Interrupts generated for FIFO status
- Receiver FIFO depth of 32 bytes
- Transmitter FIFO depth of 32 bytes

The MAX32655 provides one instance of the I2S peripheral (I2S0).

Serial Peripheral Interface (SPI)

The SPI is a highly configurable, flexible, and efficient synchronous interface where multiple SPI devices can coexist on a single bus. The bus uses a single clock signal and multiple data signals, as well as one or more slave select lines to address only the intended target device. The SPI operates independently and requires minimal processor overhead.

The provided SPI peripherals can operate in either slave or master mode and provide the following features:

- SPI modes 0, 1, 2, or 3 for single-bit communication
- 3- or 4-wire mode for single-bit slave device communication
- Full-duplex operation in single-bit, 4-wire mode

- Dual and quad data modes supported
- Multiple slave selects on some instances
- Multimaster mode fault detection
- Programmable interface timing
- Programmable SCK frequency and duty cycle
- 32-byte transmit and receive FIFOs
- Slave select assertion and deassertion timing with respect to leading/trailing SCK edge

See Table 9 for SPI configuration options.

Table 9. SPI Configuration Options

PACKAGE		INSTANCE	DATA	SLAVE SELECT LINES	MAXIMUM FREQUENCY MASTER MODE (MHz)	MAXIMUM FREQUENCY SLAVE MODE (MHz)
81 CTBGA	60 WLP					
Yes	Yes	SPI0	3-wire, 4-wire, dual, or quad data support	3	50	50
Yes	No	SPI1	3-wire, 4-wire, dual, or quad data support	1	25	50

UART (UART, LPUART)

The universal asynchronous receiver-transmitter (UART, LPUART) interface supports full-duplex asynchronous communication with optional hardware flow control (HFC) modes to prevent data overruns. If HFC mode is enabled on a given port, the system uses two extra pins to implement the industry-standard request to send (RTS) and clear to send (CTS) flow control signaling. Each instance is individually programmable.

- 2-wire interface or 4-wire interface with flow control
- 8-byte send/receive FIFO
- Full-duplex operation for asynchronous data transfers
- Interrupts available for frame error, parity error, CTS, Rx FIFO overrun, and FIFO full/partially full conditions
- Automatic parity and frame error detection
- Independent baud-rate generator
- Programmable 9th-bit parity support
- Multidrop support
- Start/stop bit support
- Hardware flow control using RTS/CTS
- 12.5Mbps for UART maximum baud rate
- 1.85Mbps for LPUART maximum baud rate
- Two DMA channels can be connected (read and write FIFOs)
- Programmable word size (5 bits to 8 bits)

The MAX32655 provides four instances of the UART peripheral—UART0, UART1, UART2, and LPUART0. LPUART0 is capable of operation in the SLEEP, LOW POWER, and MICRO POWER modes. See Table 10 for configuration options.

Table 10. UART Configuration Options

PACKAGE		INSTANCE NAME	REGISTER ACCESS NAME	HARDWARE FLOW CONTROL	POWER MODE	CLOCK SOURCE		
81 CTBGA	60 WLP					PCLK	IBRO	ERTCO
Yes	No	UART0	UART0	Yes	ACTIVE, SLEEP, LOW POWER	Yes	Yes	No
Yes	Yes	UART1	UART1	Yes	ACTIVE, SLEEP, LOW POWER	Yes	Yes	No
Yes	Yes	UART2	UART2	81 CTBGA only	ACTIVE, SLEEP, LOW POWER	Yes	Yes	No

Table 10. UART Configuration Options (continued)

Yes	No	LPUART0	UART3	No	ACTIVE, SLEEP, LOW POWER, MICRO POWER	No	Yes	Yes

1-Wire Master (OWM)

Maxim's 1-Wire bus consists of one signal that carries data and also supplies power to the slave devices and a ground return. The bus master communicates serially with one or more slave devices through the bidirectional, multidrop 1-Wire bus. The single-contact serial interface is ideal for communication networks requiring minimal interconnection.

The provided 1-Wire master supports the following features:

- Single contact for control and operation
- Unique factory identifier for any 1-Wire device
- Multiple device capability on a single line

The OWM supports both standard (15.6kbps) and overdrive (110kbps) speeds.

Standard DMA Controller

The standard DMA controller allows automatic one-way data transfer between two entities. These entities can be either memories or peripherals. The transfers are done without using CPU resources. The following transfer modes are supported:

- 4-channel
- Peripheral to data memory
- Data memory to peripheral
- Data memory to data memory
- Event support

All DMA transactions consist of an AHB burst read into the DMA FIFO, followed immediately by an AHB burst write from the FIFO.

The MAX32655 provides one instance of the standard DMA controller.

Security

AES

The dedicated hardware-based AES engine supports the following algorithms:

- AES-128
- AES-192
- AES-256

The AES keys are automatically generated by the engine and stored in dedicated flash to protect against tampering. Key generation and storage is transparent to the user.

True Random Number Generator (TRNG) Non-Deterministic Random Bit Generator (NDRBG)

The device provides a non-deterministic entropy source that can be used to generate cryptographic seeds or strong encryption keys as part of an overall framework for a secure customer application.

Software can use random numbers to trigger asynchronous events that add complexity to program execution to thwart replay attacks or key search methodologies.

The TRNG can support the system-level validation of many security standards. Maxim Integrated will work directly with the customer’s validation laboratory to provide the laboratory with any required information. Contact Maxim Integrated for details of compliance with specific standards.

CRC Module

A cyclic redundancy check (CRC) hardware module provides fast calculations and data integrity checks by application

software. It supports a user-defined programmable polynomial up to 32-bits. Direct memory access copies data into the CRC module so that CRC calculations on large blocks of memory are performed with minimal CPU intervention. Examples of common polynomials are depicted in Table 11.

Table 11. Common CRC Polynomials

ALGORITHM	POLYNOMIAL EXPRESSION	ORDER	POLYNOMIAL	CHECK
CRC-32-ETHERNET	$x^{32}+ x^{26}+ x^{23}+ x^{22}+ x^{16} + x^{12}+ x^{11}+ x^{10}+ x^8+ x^7+ x^5+ x^4+ x^2+ x^1+ x^0$	0xEDB8 8320	LSB	0xDEBB 20E3
CRC-CCITT	$x^{16}+ x^{12} + x^5 + x^0$	0x0000 8408	LSB	0x0000 F0B8
CRC-16	$x^{16}+ x^{15} + x^2 + x^0$	0x0000 A001	LSB	0x0000 B001
USB DATA	$x^{16}+ x^{15} + x^2+ x^0$	0x8005 0000	LSB	0x800D 0000
PARITY	$x^1+ x^0$	0x0000 0001	MSB	—

Secure Communications Protocol Bootloader (SCPBL)

The MAX32655 does not support an SCPBL. The user must use either JTAG or SWD to load firmware for execution.

Secure Boot

Following every reset, the device performs a secure boot to confirm the root of trust has not been compromised. The secure boot verifies the digital signature of the program memory to confirm it has not been modified or corrupted, ensuring the trustworthiness of the application software. Failure to verify the digital signature will transition the device to safe mode, which prevents execution of the customer code.

Debug and Development Interface (SWD, JTAG)

The serial wire debug (SWD) interface is used for code loading and debug for the CM4. The JTAG interface is provided for the RV32. All devices in mass production have the debugging/development interface enabled.

Applications Information

Bypass Capacitors

The proper use of bypass capacitors reduces noise generated by the IC into the ground plane. The *Pin Descriptions* table indicates which pins should be connected to bypass capacitors, and the appropriate ground plane.

It is recommended that one instance of a bypass capacitor should be connected to each pin/ball of the IC package. For example, if the *Pin Descriptions* table shows four device pins associated with voltage supply A, a separate capacitor should be connected to each pin for a total of four capacitors.

Capacitors should be placed as close as possible to their corresponding device pins. Pins which recommend more than one value of capacitor per pin should place them in parallel with the lowest value capacitor first, closest to the pin.

Ordering Information

PART	UART	SPI QUAD w/ 3 CHIP SELECTS	I²C	PULSE TRAINS	EXTERNAL ADC INPUTS	COMPARATORS	LOW-POWER UART	PIN-PACKAGE
MAX32655GXG+	4	2	3	4	8	4	2	81 CTBGA 8mm x 8mm 0.8mm pitch
MAX32655GXG+T	4	2	3	4	8	4	2	81 CTBGA 8mm x 8mm 0.8mm pitch
MAX32655GWY+	2	1	1	2	0	0	0	60 WLP 3.13mm x 3.25mm 0.35mm pitch
MAX32655GWY+T	2	1	1	2	0	0	0	60 WLP 3.13mm x 3.25mm 0.35mm pitch

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/20	Release for intro	—
1	9/21	Added 63 WLP *Pin Configuration*, *Pin Descriptions*, and *Package Information*. Updated the *Electrical Characteristics* and *Ordering Information*.	1, 7, 11, 32–36, 41, 52
2	11/21	Removed 63 WLP package and replaced with 60 WLP in *Pin Configuration, Pin Descriptions, Package Information*, *General Description*, and *Detailed Description*. Updated *Ordering information* to reflect package change to MAX32655GWY+ and MAX32655GWY+T.	1, 7, 32–36, 38, 41, 42, 46–49, 52