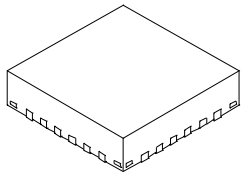
TOSHIBA CMOS Integrated Circuit Silicon Monolithic

TC78B025FTG

1-hall sine-wave PWM driver for 3-phase brushless DC motors

1. Outline

The TC78B025FTG is a 1-hall sine-wave PWM driver for 3-phase brushless DC motors. DMOS is used in output stages, realizing low-on-resistance of 0.2 Ω (total of high and low sides). A non-volatile memory (NVM) and a closed loop speed control function are incorporated. Cost can be suppressed without using microcomputers.



P-VQFN24-0404-0.50-002

Weight: 0.04g (typ.)

2. Applications

Fan motors

3. Features

- 1-hall sine-wave PWM drive
- Built-in closed loop speed control, configurable speed curve
- Low on resistance: $R_{DS(H+L)}$=0.2 Ω (typ.)
- Driving current: 3.5 A max (peak)
- Operating voltage range: 4.5 to 16 V
- Serial interface
- Standby mode
- Soft start
- Built-in protection circuits:
  Thermal shutdown (TSD), Under voltage lockout (UVLO), Over voltage protection (OVP), Under voltage protection for charge pump, Over current protection (ISD), Output current limit protection (OCP), and Lock detection protection.

4. Block Diagram

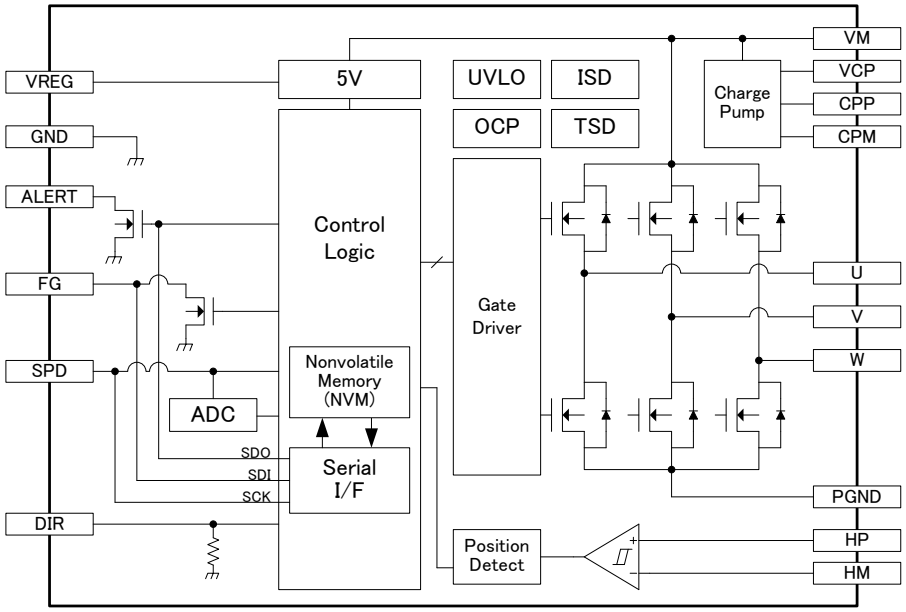


Figure 4.1 Block Diagram

Note: Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

5. Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings (Unless otherwise specified, T_a = 25°C)

Characteristics		Symbol	Rating	Unit
Power supply voltage		V_M	18	V
		V_{REG}	6 (Note 1)	
		V_{CP}	V_M + 6 (Note 1)	
Input voltage	HP, HM, DIR, FG	V_{IN}	-0.3 to 6	V
	SPD		-0.3 to 18	
Output voltage	U, V, W, FG, ALERT	V_{OUT}	18	V
Output current	FG, ALERT	I_{OUT1}	10	mA
	VREG	I_{OUT2}	10	
Power dissipation		P_D	1.7 (Note 2)	W
Operating temperature		T_{opr}	-40 to 105	°C
Storage temperature		T_{stg}	-55 to 150	°C
Junction temperature		$T_{j(MAX)}$	150	°C

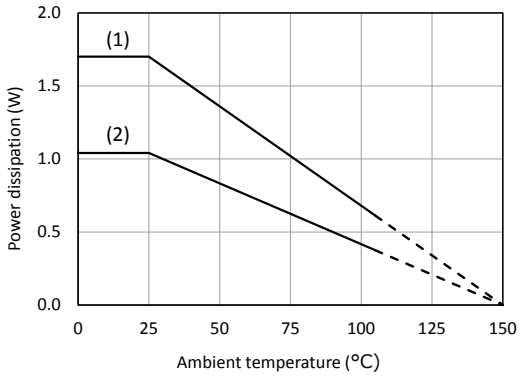
Note: The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the ratings may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion. Please use the IC within the specified operating ranges.

Note: Output current may be limited by the ambient temperature or the device implementation. The maximum junction temperature ($T_{j(MAX)}$) should not exceed 150°C.

Note 1: V_{REG} and V_{CP} pin voltage are generated in the IC. Do not apply voltage externally.

Note 2: When mounted on a board, (JEDEC 2-layer board, $R\theta_{ja}$=73.5°C/W)

5.1. Power Dissipation



Note 1: JEDEC 2-layer board, $R\theta_{ja}$=73.5°C/W
Note 2: Φ22 mm, 2-layer doughnut type board, $R\theta_{ja}$=120°C/W

Figure 5.1 Power Dissipation Characteristics

6. Operating Range

Table 6.1 Operating Range

Characteristics		Symbol	Min	Typ.	Max	Unit
VM pin power supply voltage 1		$V_{M(opr1)}$	5.5	12	16	V
VM pin power supply voltage 2 (Note 1)		$V_{M(opr2)}$	10.8	12	16	
VM pin power supply voltage 3 (Note 2)		$V_{M(opr3)}$	(4.5)	—	(5.5)	
Input PWM command frequency		f_{TSP}	1	—	100	kHz
Input SPI CLK frequency		f_{SCK}	15	—	500	kHz
Input voltage	HP, HM	V_{IN}	0.1	—	V_{REG}-2.0	V
	DIR, SPD, FG		-0.3	—	5.5	

Note 1: For NVM writing
Note 2: Electrical characteristics are only for reference because the variation of electrical characteristics becomes large.

Table 6.2 NVM Characteristics

Characteristics	Conditions	Min	Max	Unit
Program/Erase cycles	T_j=0 to 90°C	10	—	Cycle
Program/Erase period	On execution of NVM_SAVE	—	1	s

7. Pin Assignment(Top View)

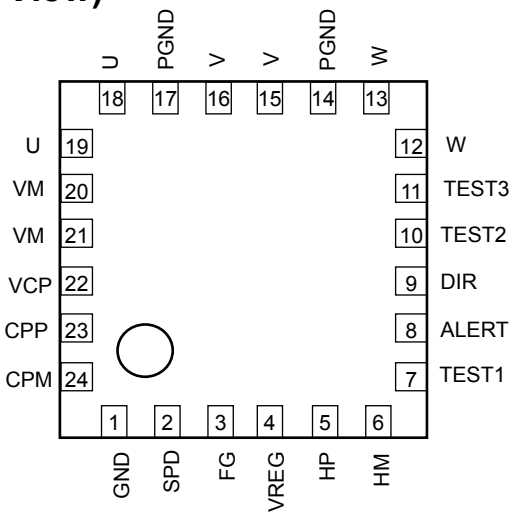


Figure 7.1 Pin Assignment

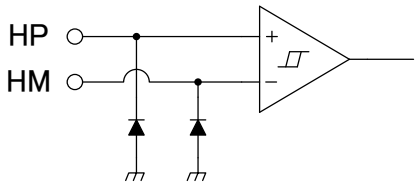
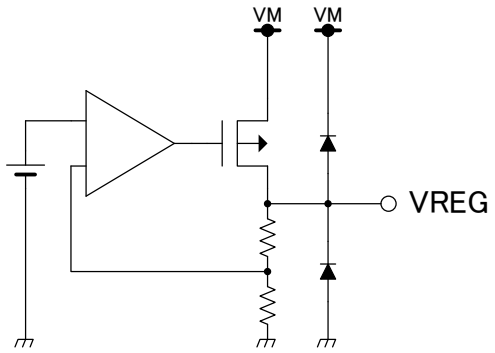
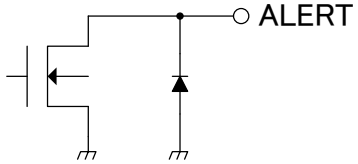
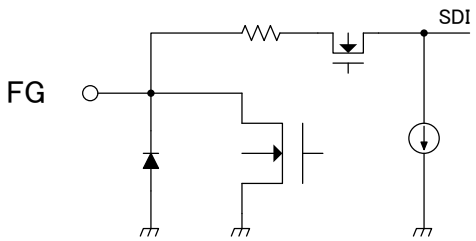
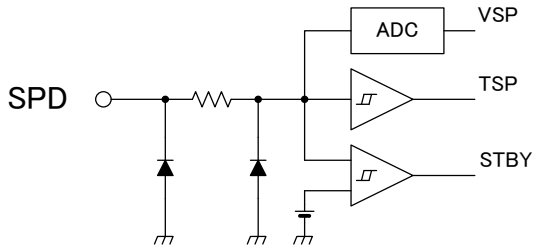
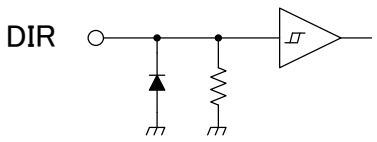
8. Pin Description

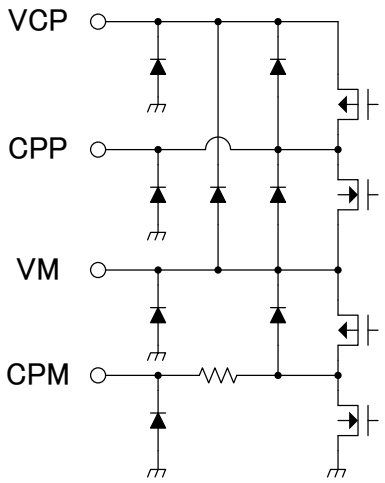
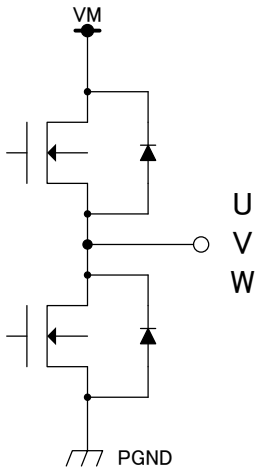
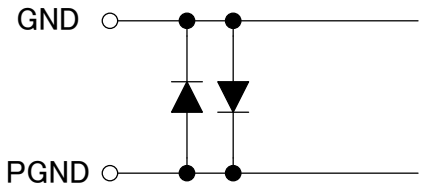
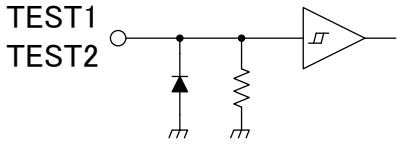
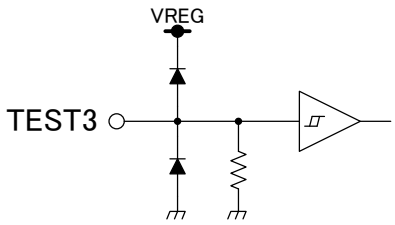
Table 8.1 Pin Description

Pin No.	Pin name	Input / output	Pin description
1	GND	—	GND pin
2	SPD	IN	Input pin for speed command, Serial I/F clock input pin
3	FG	I/O	Output pin for rotation number signal, Serial I/F data I/O pin
4	VREG	—	5 V reference voltage output pin
5	HP	IN	Hall signal input (+) pin
6	HM	IN	Hall signal input (-) pin
7	TEST1	—	TEST pin (50 kΩ pull-down)
8	ALERT	OUT	Output pin for alert signal, Serial I/F data output pin
9	DIR	IN	Rotation direction set pin (50 kΩ pull-down)
10	TEST2	—	TEST pin (50 kΩ pull-down)
11	TEST3	—	TEST pin (50 kΩ pull-down)
12	W	OUT	W phase output pin
13	W	OUT	W phase output pin
14	PGND	—	Power GND pin
15	V	OUT	V phase output pin
16	V	OUT	V phase output pin
17	PGND	—	Power GND pin
18	U	OUT	U phase output pin
19	U	OUT	U phase output pin
20	VM	—	Power supply pin
21	VM	—	Power supply pin
22	VCP	—	Connect pin for accumulation capacitor of charge pump
23	CPP	—	Connect pin for pumping capacitor of charge pump
24	CPM	—	Connect pin for pumping capacitor of charge pump

Note: TEST pin must be connected to GND.
Note: SPD pin should not be left open state.
Note: Though GND and PGND pins are connected through bidirectional diodes in the IC, each pin should be connected to the GND line. Please refer to “Reference Layout” for details.
Note: Because each U, V, W and VM signal has two pins, short out these two pins at the external pattern respectively.

9. I/O Equivalent Circuits

Pin name	Description	Equivalent circuit
HP HM	Hall signal input pin	
VREG	5 V reference voltage output pin	
ALERT	Output pin for alert signal Open drain Serial I/F data output pin	
FG	Output pin for rotation number signal Open drain Serial I/F data I/O pin	
SPD	Input pin for speed command Serial I/F clock input pin	
DIR	Input pin for rotation direction signal 50 kΩ pull-down	

Pin name	Description	Equivalent circuit
VCP CPP CPM	Charge pump	
U V W	Motor output pin	
GND PGND	GND pin	
TEST1 TEST2	TEST pin 50 kΩ pull-down	
TEST3	TEST pin 50 kΩ pull-down	

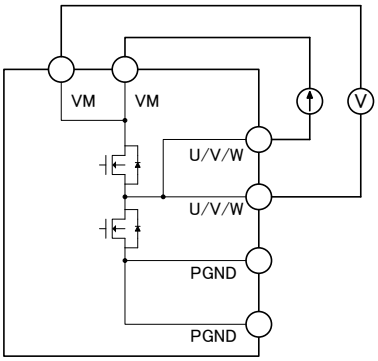
10. Electrical Characteristics

Table 10.1 Electrical Characteristics (Unless otherwise specified, VM = 12 V and T_a = 25°C)

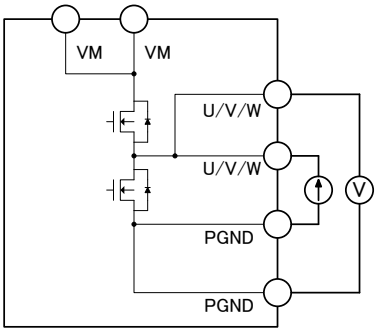
Characteristics		Symbol	Test conditions	Min	Typ.	Max	Unit
Power supply current		I_{VM}	VM=12 V, VREG=OPEN Hall signal input=100 Hz, Output=OPEN	—	10	12	mA
		I_{STBY}	VM=12 V, Standby mode	—	0.33	0.5	
VREG pin voltage		V_{REG}	VM=12 V, I_{VREG}=0 to 10 mA	4.5	5	5.5	V
Change pump voltage		—	VM=12 V, VCP-VM	4.2	4.7	5.0	V
Hall input signal	Common phase input voltage range	V_{HCMR}	—	0.1	—	V_{REG} -2.0	V
	Input amplitude range	V_H	—	40	—	—	mV
	Input current	I_{HIN}	—	—	—	1	μA
	Hysteresis(+) voltage	V_{HHYS+}	—	—	8	—	mV
	Hysteresis (-) voltage	V_{HHYS-}	—	—	-8	—	
SPD pin	Standby mode control voltage	$V_{STBY(L)}$	Standby mode switching voltage	1	1.15	—	V
		$V_{STBY(H)}$	Standby mode releasing voltage	—	1.25	1.4	V
		$V_{STBY(hys)}$	Hysteresis voltage	—	100	—	mV
	Input current	I_{SPD}	V_{SPD}=0 to V_{REG}	—	—	1	μA
SPD pin During PWM duty input	Input voltage	$V_{TSP(H)}$	High voltage	2.0	—	5.5	V
		$V_{TSP(L)}$	Low voltage	-0.3	—	1.0	V
		$V_{TSP(hys)}$	Hysteresis voltage	—	200	—	mV
	Input frequency	f_{TSP}	—	1	—	100	kHz
	100 % duty detection time	$T_{duty(100)}$	—	—	1.5	—	ms
	0 % duty detection time	$T_{duty(0)}$	—	—	100	—	
SPD pin During analog voltage input	Input voltage	$V_{VSP(H)}$	ADC=512 (100 %)	3.9	4.0	4.1	V
		$V_{VSP(L)}$	ADC=0 (0 %)	1.4	1.5	1.6	V
	ADC response time	t_{ADC}	—	—	—	10	ms
DIR pin	Input voltage	$V_{DIR(H)}$	High voltage	2.0	—	5.5	V
		$V_{DIR(L)}$	Low voltage	-0.3	—	1.0	V
		$V_{DIR(hys)}$	Hysteresis voltage	—	200	—	mV
	Input current	$I_{SPD(H)}$	V_{DIR}=5 V	80	100	120	μA
		$I_{SPD(L)}$	V_{DIR}=0 V	—	—	1	
Output-on-resistance		$R_{DS(H+L)}$	I_{OUT}=0.2 A, T_j=25 to 105°C (Note)	—	0.2	0.3	Ω
Internal OSC frequency		f_{OSC}	—	11.64	12	12.36	MHz
Output PWM frequency		$f_{PWM(1)}$	f_{OSC}=12 MHz, PWMSEL[2:0]=000	—	23.4	—	kHz
		$f_{PWM(2)}$	f_{OSC}=12 MHz, PWMSEL[2:0]=011	—	187.5	—	kHz
FG pin	Output low voltage	—	I_{FG}=5 mA	—	0.15	0.3	V
	Output leakage current	—	V_{FG}=18 V	—	1.5	5	μA
ALERT pin	Output low voltage	—	I_{ALERT}=5 mA	—	0.15	0.3	V
	Output leakage current	—	V_{ALERT}=18 V	—	—	1	μA
Output current limit		I_{OCL}	In setting the current of 1.5 A, Difference to the target.	-20	—	20	%
Over current protection	Shutdown current	I_{ISD}	(Design value)	4.5	5.5	6.5	A

Characteristics		Symbol	Test conditions	Min	Typ.	Max	Unit
Thermal shutdown	Shutdown temperature	T_{TSD}	In rising temperature (Design value)	—	170	—	°C
	Release hysteresis temperature	ΔT_{TSD}	In falling temperature (Design value)	—	40	—	°C
	Release temperature	—	In falling temperature (Design value)	—	130	—	°C
Over voltage protection	Switching voltage (from sine-wave drive to 150° commutation)	—	In VM rising	16.5	17.2	17.9	V
	Recovery hysteresis voltage (from 150° commutation to sine-wave drive)	—	In VM falling	—	400	—	mV
	Recovery voltage (from 150° commutation to sine-wave drive)	—	In VM falling	16.1	16.8	17.5	V
Under voltage protection	UVLO operating voltage	—	In VM falling	3.7	3.9	4.1	V
	UVLO hysteresis voltage	—	In VM rising	—	300	—	mV
	UVLO release voltage	—	In VM rising	4.0	4.2	4.4	V
	UVLO operating voltage	—	In VREG falling	—	3.7	—	V
	UVLO hysteresis voltage	—	In VREG rising	—	300	—	mV
	UVLO release voltage	—	In VREG rising	—	4.0	—	V
Under voltage protection for charge pump	Under voltage protection operating voltage	—	In the voltage between VCP pin and VM pin falling	—	3.3	—	V
	Under voltage protection hysteresis voltage	—	In the voltage between VCP pin and VM pin rising	—	300	—	mV
	Under voltage protection release voltage	—	In the voltage between VCP pin and VM pin rising	—	3.6	—	V

Note: Test circuit for output on resistance.



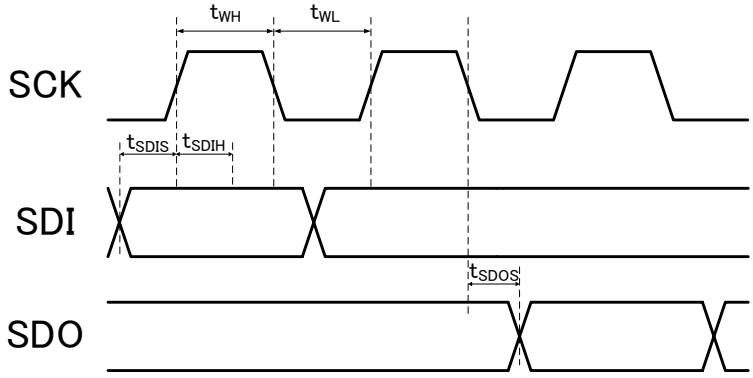
High-side test circuit



Low-side test circuit

Table 10.2 Serial Interface (Unless otherwise specified, VM = 12 V and T_a = 25°C)

Characteristics		Symbol	Test conditions	Min	Typ.	Max	Unit
SCK	Input voltage	$V_{SCK(H)}$	High voltage	2.0	—	5.5	V
		$V_{SCK(L)}$	Low voltage	-0.3	—	1.0	V
		$V_{SCK(hys)}$	Hysteresis voltage	—	100	—	mV
	Input frequency	f_{SCK}	—	15	—	500	kHz
	High period	t_{WH}	—	1	—	—	μs
	Low period	t_{WL}	—	1	—	—	
SDI	Setup period	t_{SDIS}	—	1	—	—	μs
	Hold period	t_{SDIH}	—	500	—	—	ns
SDO	Setup period	t_{SDOS}	—	—	—	500	ns



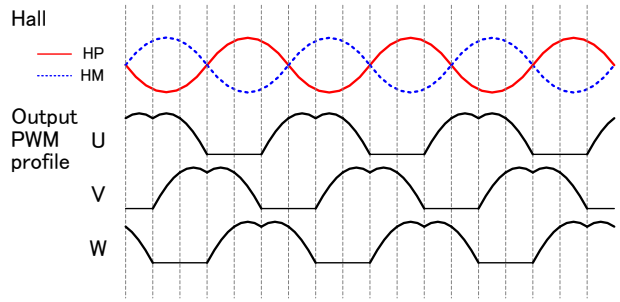
11. Functional Description

11.1. Basic Operation

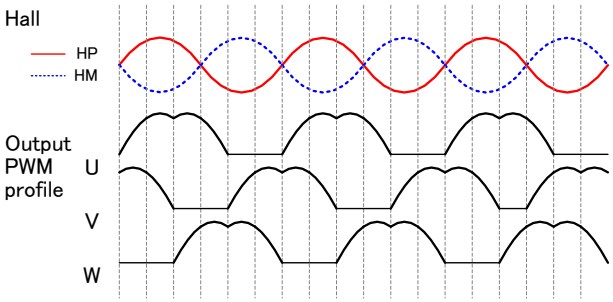
The TC78B025FTG can be operated by 1-hall sine-wave commutation and 1-hall 150° commutation. Also, a closed loop speed control function is implemented without using an external microcomputer. Motor rotation speed can be controlled by inputting PWM duty signal or applying analog voltage to the SPD pin.

The operation moves to the standby mode when a zero cross of the hall signal is not detected for a lock detection period after the voltage of $V_{STBY(L)}$ or less is applied to the SPD pin. In the standby mode, the IC power consumption is reduced by powering off its internal 5-V regulator. In case that the hall element is power supplied by the IC's 5-V regulator, the power consumption of the whole motor system can be reduced. In case that motor is configured as not stop when the voltage of SPD pin is $V_{STBY(L)}$ or less, standby mode is disabled.

1-hall sine-wave drive

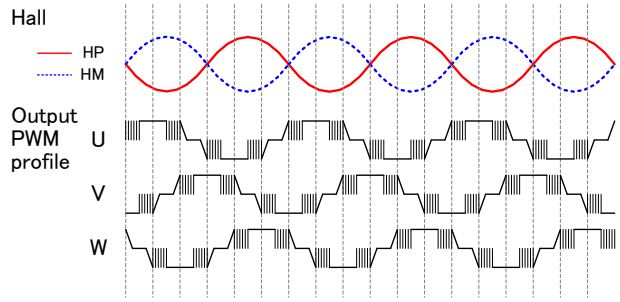


CW lead angle=0°

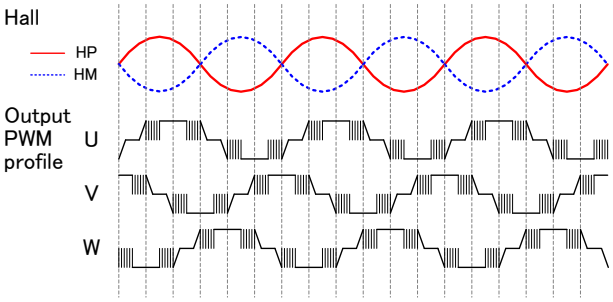


CCW lead angle=0°

1-hall 150°drive



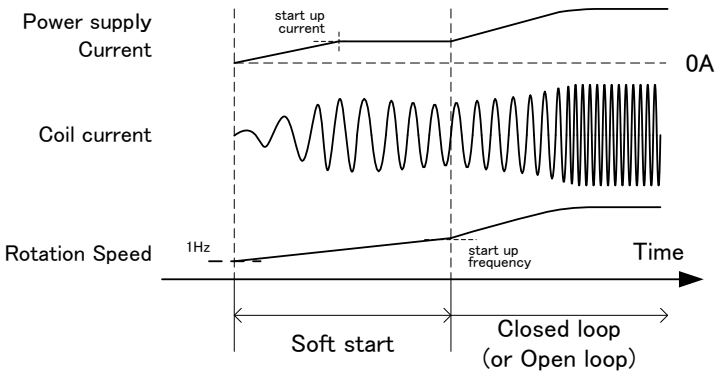
CW lead angle=0°



CCW lead angle=0°

11.2. Soft Start

Soft start operates when the motor starts from the stop state to prevent rush current. Soft start increases the output duty gradually from 0 % until the output current reaches the startup current. The rotation frequency increases from 1 Hz. Soft start is finished and switches to the closed loop speed control or the open loop speed control when the rotation frequency reaches the switching frequency (startup frequency).



11.3. Input/Output Signals

11.3.1. SPD

SPD pin controls the motor start, the motor stop, and the rotation speed.
PWM duty signal input or analog voltage signal input can be configured by the register. Also, the polarity of the signal can be configured by the register.
In case of analog voltage input, the resolution is 9 bits in the voltage range of $V_{VSP(L)}$ to $V_{VSP(H)}$.
In case of PWM duty input, its frequency range is from 1 kHz to 100 kHz. When the frequency range is from 1 kHz to 20 kHz, the resolution is 9 bits. And when it is 20 kHz or more, the resolution decreases. For example, in case of 40 kHz, the resolution is 8 bits, and in case of 100 kHz, it becomes 7 bits.
In addition, the SPD pin can be also used as the clock input pin for the serial interface (for SCK signal).

11.3.2. DIR

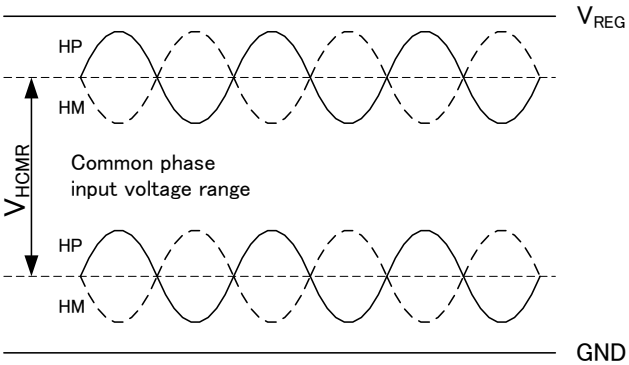
DIR pin controls the motor rotation direction; forward rotation (CW) and reverse rotation (CCW).
Relation of DIR pin polarity and the rotation direction is configured by the register.

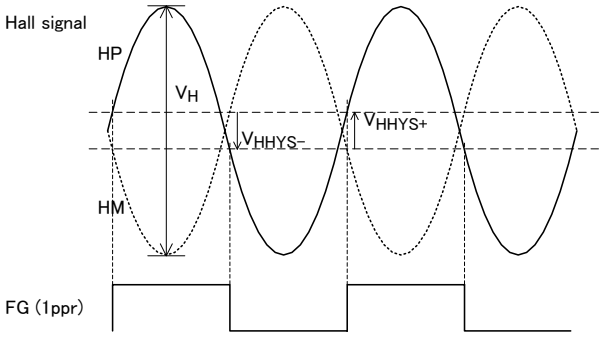
11.3.3. ALERT

ALERT pin is an open drain type output pin. When an abnormal state (over current, over temperature, motor lock, or under voltage for charge pump) is detected, this pin outputs low level signal.
In addition, this pin can be also used as the data output pin for serial interface (for SDO signal).

11.3.4. HP, HM

Pins of HP and HM input hall signals.
In case of using hall element, please input signals whose characteristics are shown below.

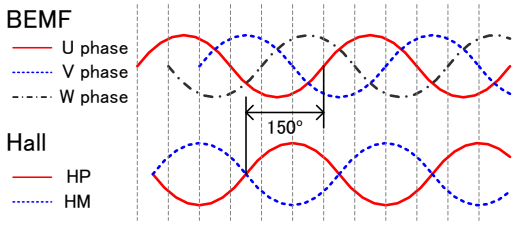




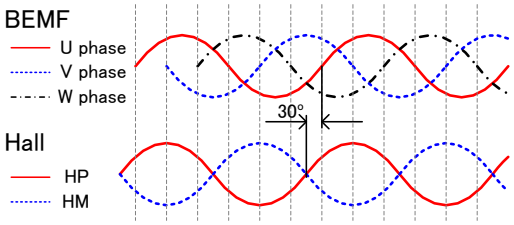
In case of using hall IC, always input the hall signal to HP pin. Voltage of HM pin should be fixed.

As default, please align the hall sensor so that the relationship between hall signals and induced voltage is as below charts.

Forward rotation (CW)



Reverse rotation (CCW)



When the hall sensor is off the default position, offset is possible by using the resister.

11.3.5. FG

FG pin is an open drain type output pin. It outputs the rotation speed signal that is obtained from the hall signal. According to the register setting, FG pin can also output RDO signal when motor lock is detected. RDO signal is low level in motor lock detection.
In addition, FG pin can be also used as the data input or input/output pin for serial interface (for SDI or SDIO signal).

Table 11.1 Relation of FG signal setting and the number of output pulses per one motor cycle

FGSEL[2:0]	FG signal set	Number of motor poles				
		2 poles	4 poles	6 poles	8 poles	10 poles
000	1 ppr	1	2	3	4	5
001	2/3 ppr	2/3	4/3	2	8/3	10/3
010	1/2 ppr	0.5	1	1.5	2	2.5
011	2 ppr	2	4	6	8	10
100	3 ppr	3	6	9	12	15
101	2.4 ppr	2.4	4.8	7.2	9.6	12
110	1/3 ppr	1/3	2/3	1	4/3	5/3
111	Don't use					

Note: FG pin outputs the signal when the frequency of the hall signal is 1.67 Hz or more.
When the frequency of the hall signal is less than 1.67 Hz, FG signal is fixed to Hi-Z.
Note: When FG signal is set to 1 ppr, a signal synchronized with the hall signal is output.
When FG signal is set to the others, internal processed result is output.

11.4. Speed Control

11.4.1. Closed Loop

The basic speed curve (relation between SPD signal value and rotation speed) of closed loop speed control is as follows;

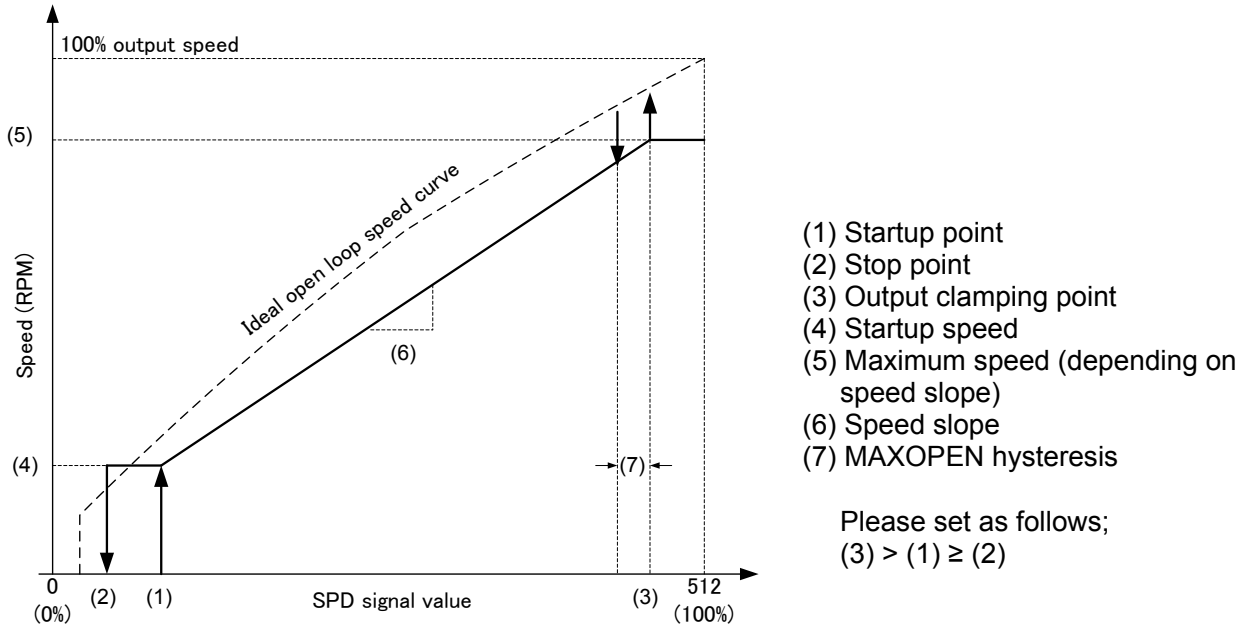


Figure 11.1 Speed Slope Example in Closed loop speed control

(1) Startup point:
Output is enabled when SPD signal value exceeds the startup threshold. The threshold range is from 0 (0 %) to 255 (49.8 %) with a 0.2 % resolution. It is set by the 8-bit register STARTDUTY.
SPD duty to enable output (%) = 100 × STARTDUTY / 512

(2) Stop point:
Output is disabled when SPD signal value decreases to the stop threshold. The threshold range is from 0 (0 %) to 254 (49.6 %) with a 0.4 % resolution. It is set by the 7-bit register STOPDUTY.
SPD duty to disable output (%) = 200 × STOPDUTY / 512

(3) Output clamping point and (7) MAXOPEN hysteresis:
In case MAXDUTY = 0: When SPD signal value exceeds the output clamping threshold, the rotation speed is fixed. The threshold range is from 257 (50.2 %) to 512 (100 %) with a 0.2 % resolution. It is set by the 8-bit register MAXDUTY.
SPD duty to clamp output (%) = 100 × (257 + MAXDUTY) / 512

In case MAXOPEN = 1: When SPD signal value exceeds the output clamping threshold, the control switches to open loop speed control. The output duty during open loop speed control corresponds to SPD signal value. The hysteresis of SPD signal value to let the control switch back to closed loop speed control range is from 2 (0.4 %) to 32 (6.25 %) with a 0.4 % resolution. It is set by the 4-bit register MAXDUTYHYS.
SPD duty hys (%) = 200×(MAXDUTYHYS + 1) / 512

(4) Startup speed:
The minimum rotation speed in startup is set by the 12-bit register STARTRPM. Setting range is from 0 to 4095 RPM with 1 RPM resolution.
Startup speed (RPM) = STARTRPM

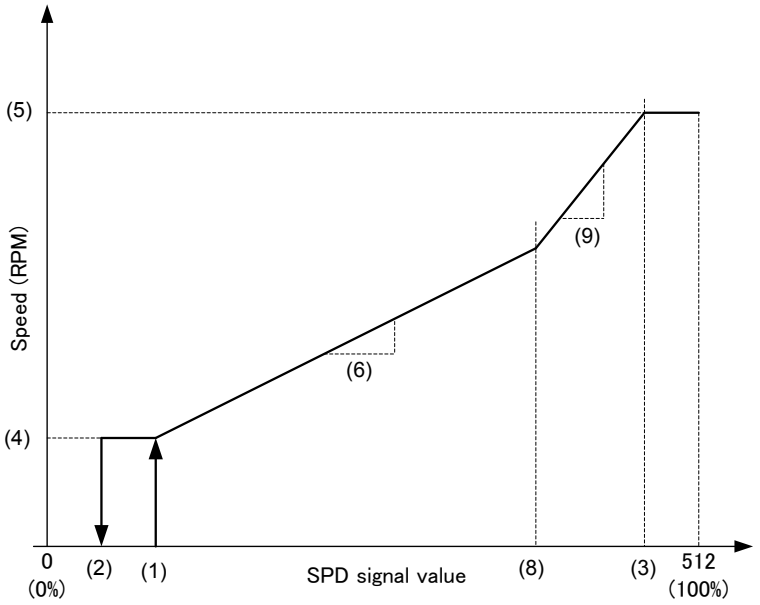
(5) Maximum speed and (6) Speed slope:
Maximum speed depends on the speed slope, which is set by the register SPEEDSLOP. It is a 14-bit register.
SPEEDSLOP = 64 × (Maximum speed – Startup speed) / (MAXDUTY + 257 – STARTDUTY)

Configurations of MAXOPEN, NOSTOP, and MAXOFF registers determine the behavior when SPD signal value is equivalent to the startup (output enabling) point or less.

Table 11.2 Rotation Behavior (SPD signal value ≤ Startup point)

MAXOPEN	NOSTOP	MAXOFF	Target speed		
			SPD = 0 %	0 % < SPD ≤ Startup point	Stop point < SPD ≤ Startup point
0	0	0	0	0	Duty up: 0 Duty down: Startup speed
	0	1	Maximum Speed	0	Duty up: 0 Duty down: Startup speed
	1	0	Startup speed	Startup speed	Startup speed
	1	1	Maximum Speed	Maximum Speed	Startup speed
1	0	0	0	0	Duty up: 0 Duty down: Startup speed
	0	1	100 % Output	0	Duty up: 0 Duty down: Startup speed
	1	0	Startup speed	Startup speed	Startup speed
	1	1	100 % Output	100 % Output	Startup speed

Adding a speed change point to the speed curve is possible.



(1) Startup point
(2) Stop point
(3) Output clamping point
(4) Startup speed
(5) Maximum speed (depending on speed slope)
(6) First speed slope
(8) Speed change point
(9) Second speed slope
Please set as follows;
(3) > (8) > (1) ≥ (2)

Figure 11.2 Speed Slope Example in Closed loop speed control (in case of adding speed change point)

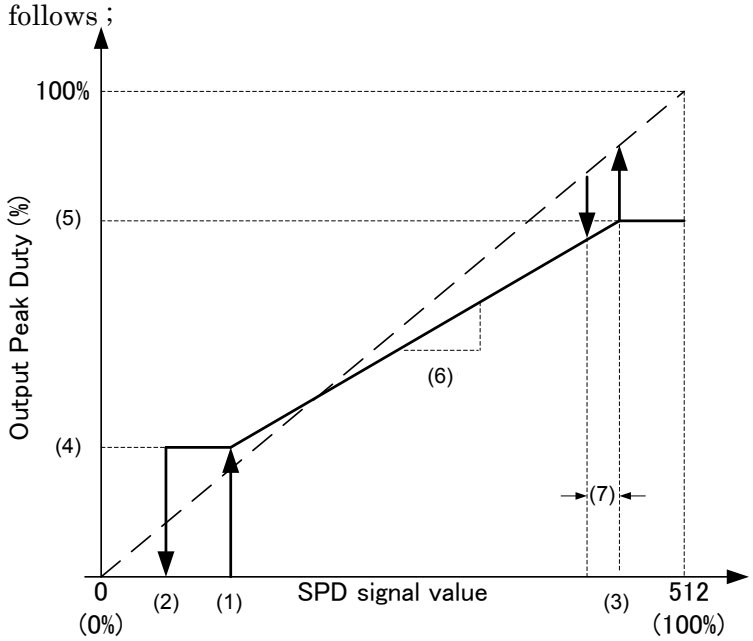
(8) Speed change point:
The SPD signal value range of the speed change point is from 0 (0.4 %) to 510 (99.6 %) with a 0.4 % resolution. It is set by the 8-bit register CHANGEDUTY.
SPD duty of change point (%) = 200 × CHANGEDUTY / 512

In case of un-using the speed change point, set CHANGEDUTY to 0.

(9) Second speed slope:
After passing the speed change point, the register SPEEDSLOP2 sets the speed slope.

11.4.2. Open Loop

The basic speed curve (relation between SPD signal value and output duty) of open loop speed control is as follows ;



(1) Startup point
(2) Stop point
(3) Output clamping point
(4) Startup output duty
(5) Maximum output duty (depending on speed slope)
(6) Speed slope
(7) MAXOPEN hysteresis

Please set as follows;
(3) > (1) ≥ (2)

Figure 11.3 Speed Slope Example in Open loop speed control

(1) Startup point:
Output is enabled when SPD signal value exceeds the startup threshold. The threshold range is from 0 (0 %) to 255 (49.8 %) with a 0.2 % resolution. It is set by the 8-bit register STARTDUTY.
SPD duty to enable output (%) = 100 × STARTDUTY / 512

(2) Stop point:
Output is disabled when SPD signal value decreases to the stop threshold. The threshold range is from 0 (0 %) to 254 (49.6 %) with a 0.4 % resolution. It is set by the 7-bit register STOPDUTY.
SPD duty to disable output (%) = 200 × STOPDUTY / 512

(3) Output clamping point and (7) MAXOPEN hysteresis:
In case MAXDUTY = 0: When SPD signal value exceeds the output clamping threshold, the output duty is fixed. The threshold range is from 257 (50.2 %) to 512 (100 %) with a 0.2 % resolution. It is set by the 8-bit register MAXDUTY.
SPD duty clamp output (%) = 100 × (257 + MAXDUTY) / 512

In case MAXOPEN = 1: When SPD signal value exceeds the output clamping threshold, the output duty becomes corresponding to SPD signal value. The hysteresis range of SPD signal value to let the output return to original speed curve is from 2 (0.4 %) to 32 (6.25 %) with a 0.4 % resolution. It is set by the 4-bit register MAXDUTYHYS.
SPD duty hys (%) = 200 × (MAXDUTYHYS + 1) / 512

(4) Startup output duty:
The minimum output duty in startup is set by an upper 8-bit of the 12-bit register STARTRPM. Setting range is from 0 (0 %) to 255 (49.8 %) with a 0.2 % resolution.
Startup output duty (%) = 100 × STARTRPM[11:4] / 512

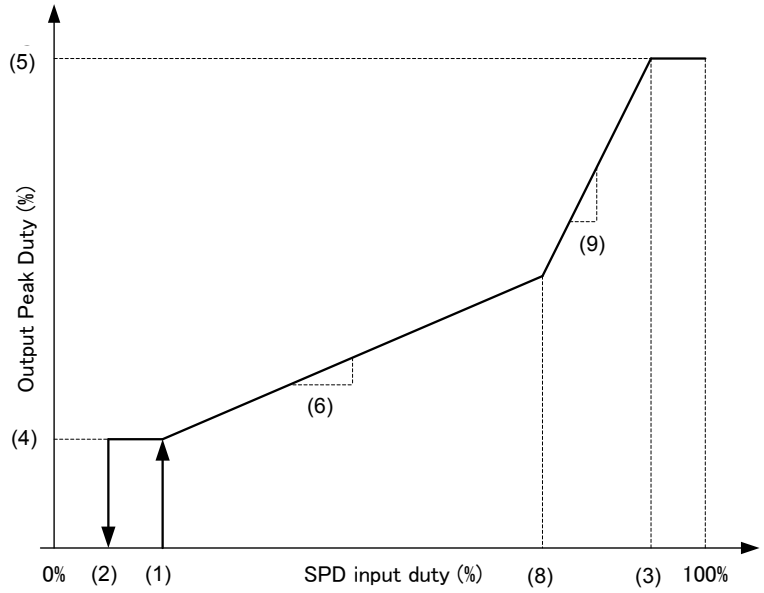
(5) Maximum output duty and (6) Speed slope:
Maximum output duty depends on the speed slope, which is set by the register SPEEDSLOP. It is a 14-bit register.
$SPEEDSLOP = 2^{19} \times (Maximum\ output\ duty(\%) - Startup\ output\ duty(\%)) / (MAXDUTY + 257 - STARTDUTY) / 100$

Configurations of MAXOPEN, NOSTOP, and MAXOFF registers determine the behavior when SPD signal value is equivalent to the startup (output enabling) point or less.

Table 11.3 Rotation Behavior (SPD signal value ≤ Startup point)

MAXOPEN	NOSTOP	MAXOFF	Output duty		
			SPD = 0 %	0 % < SPD ≤ Startup point	Stop point < SPD ≤ Startup point
0	0	0	0	0	Duty up: 0 Duty down: Startup Output
	0	1	Maximum Output	0	Duty up: 0 Duty down: Startup Output
	1	0	Startup Output	Startup Output	Startup Output
	1	1	Maximum Output	Maximum Output	Startup Output
1	0	0	0	0	Duty up: 0 Duty down: Startup Output
	0	1	100 % Output	0	Duty up: 0 Duty down: Startup Output
	1	0	Startup Output	Startup Output	Startup Output
	1	1	100 % Output	100 % Output	Startup Output

Adding a speed change point to the speed curve is possible.



(1) Startup point
(2) Stop point
(3) Output clamping point
(4) Startup output duty
(5) Maximum output duty (depending on speed slope)
(6) First speed slope
(8) Speed change point
(9) Second speed slope

Please set as follows;
(3) > (8) > (1) ≥ (2)

Figure 11.4 Speed Slope Example in Open loop speed control (in case of adding speed change point)

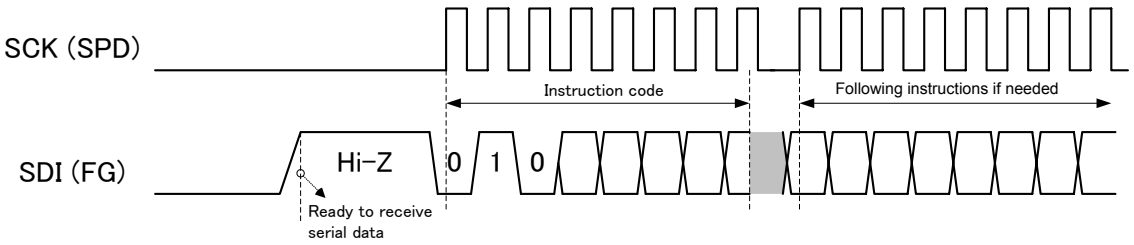
(8) Speed change point:
The SPD signal value range of the speed change point is from 0 (0.4 %) to 510 (99.6 %) with a 0.4 % resolution. It is set by the 8-bit register CHANGEDUTY.
SPD duty of change point (%) = 200 × CHANGEDUTY / 512

In case of unusing the speed change point, set CHANGEDUTY to 0.

(9) Second speed slope:
After passing the speed change point, the register SPEEDSLOP2 sets the speed slope.

11.5. Serial Interface and NVM

Data of internal registers and non-volatile memory (NVM) can be configured via serial interface. When FG signal is Hi-Z, receiving serial commands is possible.



11.5.1. Serial Commands

Table 11.4 Serial Commands

Command	Code	Description	Following data
SR_READ	010 01 001	Read status register	8-bit data out
SR_WRITE	010 01 010	Write status register	8-bit data in
REG_READ	010 10 001	Read normal register	8-bit addr in + 16-bit data out
REG_WRITE	010 10 010	Write normal register	8-bit addr in + 16-bit data in
NVM_LOAD	010 11 001	Load NVM data to normal register	No
NVM_SAVE	010 11 010	Store data of normal register to NVM	No
NVM_ABORT	010 11 100	Terminate NVM writing process forcedly	No

11.5.2. Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	—	—	CAL_ERR	NVM_WR	WIRE	ENB	BUSY

Name	Description	Detail
BUSY	State of register processing	BUSY=0: Standby BUSY=1: Under processing
ENB	Serial command enable setting	ENB=0: Only SR_READ SR_WRITE is acceptable. ENB=1: All commands are acceptable.
WIRE	Serial communication mode setting	WIRE=0: 3-wire mode (SCK=SPD, SDI=FG, and SDO=ALERT) WIRE=1: 2-wire mode (SCK=SPD and SDIO=FG)
NVM_WR	NVM mode setting	NVM_WR=0: READ enable, WRITE disable NVM_WR=1: READ disable, WRITE enable
CAL_ERR	Result of hall position detection	CAL_ERR=0: Success CAL_ERR=1: Failure

11.5.3. Normal Register

Table 11.5 Register Map

ADDR	Bit	Name	Description	Default
0	15:0	USERID[15:0]	—	0
1	15	NOSTOP	Non-stop mode (0: disable, 1: enable)	0
	14:8	STOPDUTY[6:0]	Stop duty	0
	7:0	STARTDUTY[7:0]	Startup duty	0
2	15:8	CHANGEDUTY[7:0]	Speed change point duty	0
	7:0	MAXDUTY[7:0]	Maximum duty	0
3	15:4	STARTRPM [11:0]	Rotation speed in startup	0
	3:0	MAXDUTYHYS[3:0]	Recovery hysteresis from open loop to closed loop speed control	0
4	15:2	SPEEDSLOP[13:0]	Speed slope	0
	1	MAXOPEN	Switching to open loop speed control when SPD signal value exceeds the threshold (0: disable, 1: enable)	0
	0	MAXOFF	Rotating with full speed when SPD signal value corresponds to the startup point or less. (0: disable, 1: enable)	0
5	15:2	SPEEDSLOP2[13:0]	Speed slope after passing speed change point	0
	1	REVALERT	ALERT output in reverse detection	0
	0	OPENLOOP	Open loop/Closed loop speed control (0: Closed loop, 1: Open loop)	0
6	15	KIX	To eight times the KI	0
	14:8	KI[6:0]	KI (0 to 127)	0
	7	KPX	To eight times the KP	0
	6:0	KP[6:0]	KP (0 to 127)	0
7	15	STBY	Standby mode (0: disable, 1: enable)	0
	14	DIR	Relation of DIR pin polarity and rotation direction (0: positive, 1: negative)	0
	13:11	POLEPAIR[2:0]	Pair of motor poles	0
	10:9	MAXSPEED[1:0]	Maximum rotation speed	0
	8	HALLINV	Hall signal polarity conversion (0: positive, 1: negative)	0
	7:6	HALLPOS[1:0]	Hall alignment sector	0
	5:0	HALLOFFSET[5:0]	Hall position offset	0
8	15	RDSEL	The signal selection to output FG pin (0: FG signal, 1: RDO signal)	0
	14:12	FGSEL[2:0]	FG signal type setting	0
	11	SPDSEL	SPD command type setting (0: Analog voltage input , 1: PWM duty input)	0
	10	SPDINV	SPD signal polarity conversion (0: positive, 1: negative)	0
	9	REVBRAKE	Reverse startup (0: disable, 1: enable)	0
	8	150DRV	150° commutation (0: sine-wave drive, 1:150° commutation)	0
	7	ISDLATCH	ISD latch (0: disable, 1:enable)	0
	6	OCPMASK	Masking period for current limit	0
	5	OCPDIS	Disable current limit (0: OCP enable, 1: OCP disable)	0
	4:3	OCPLEVEL[1:0]	Current limit threshold setting	0
	2:0	PWMSEL[2:0]	Output PWM frequency setting	0

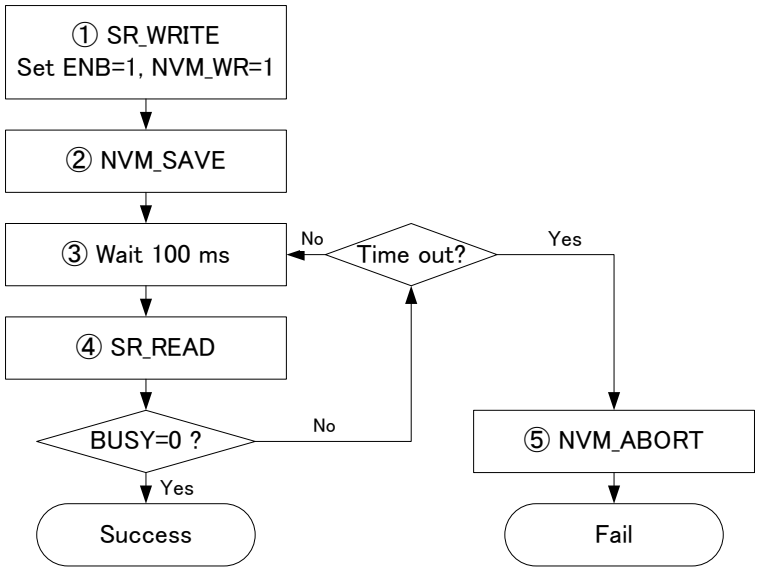
ADDR	Bit	Name	Description	Default
9	15	TON	Lock detection ON period	0
	14	TOFF	Lock detection OFF period	0
	13	LOCKDIS	Disable lock detection	0
	12:10	DUTYCHGLIMIT[2:0]	Duty changing limit	0
	9:8	STARTFREQ[1:0]	Startup switching frequency	0
	7:6	STARTCURRENT[1:0]	Startup current limit	0
	5	LASEL	Lead angle selection	0
	4:0	LATABLE[4:0]	Lead angle table	0
10	15:6	Trq_duty[9:0]	SPD command	0
	5	Unused	Don't care	0
	4:3	Hall off.Freq[1:0]	Hall position detection (Forced commutation frequency)	0
	2:1	Hall cal.Freq[1:0]	Hall position detection (Detection starting frequency)	0
	0	Hall cal.	Hall position detection	0

Note: Data of ADDR 0 to 9 can be stored in NVM.

ADDR	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	USERID [15:0]															
1	NOSTOP	STOPDUTY [6:0]							STARTDUTY [7:0]							
2	CHANGEDUTY [7:0]								MAXDUTY [7:0]							
3	STARTRPM [11:0]												MAXDUTYHYS [3:0]			
4	SPEEDSLOP[13:0]														MAXOPEN	MAXOFF
5	SPEEDSLOP2[13:0]														REVALERT	OPENLOOP
6	KIX	KI [6:0]							KPX	KP [6:0]						
7	STBY	DIR	POLEPAIR [2:0]			MAXSPEED [1:0]		HALLINV	HALLPOS [1:0]		HALLOFFSET [5:0]					
8	RDSEL	FGSEL [2:0]			SPDSEL	SPDINV	REVBRAKE	150DRV	ISDLATCH	OCPMASK	OCPDIS	OCPLEVEL [1:0]		PWMSEL [2:0]		
9	TON	TOFF	LOCKDIS	DUTYCHGLIMIT [2:0]			STARTFREQ [1:0]		STARTCURRENT[1:0]		LASEL	LATABLE [4:0]				
10	Trq_duty[9:0]											Hall off. Freq [1:0]		Hall cal. Freq [1:0]		Hall cal.

11.5.4. Write Non-Volatile Memory (NVM)

Flow chart of NVM write is as follows;



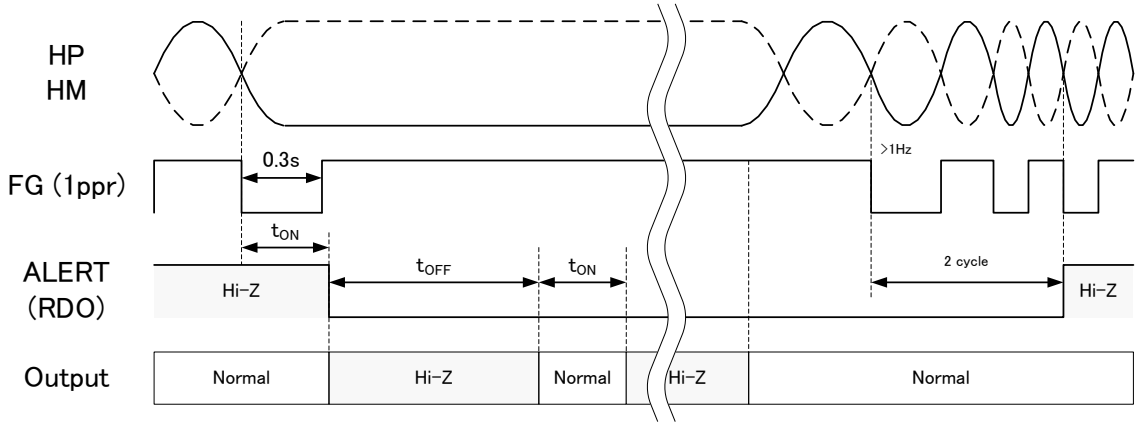
Writing period may be longer according to the operating conditions. In case BUSY does not return to 0 over 1 s, it is supposed to be a writing error. Please terminate the writing process forcedly by NVM_ABORT command.

After NVM writing process has completed, always return NVM_WR setting to 0.

11.6. Protection Functions

11.6.1. Lock Detection Protection

It is recognized as a lock state if the zero cross of the hall signal is not detected for a certain period (t_{ON}). While this function is activated, ALERT pin outputs a low level signal. In this case, the output is turned off for a certain period (t_{OFF}). Then, the IC output is recovered automatically. During output OFF period, the FG signal is fixed to Hi-Z state. Lock detection period and output OFF period can be configured by registers.



11.6.2. Output Current Limit Protection (OCP)

This function is incorporated to limit the motor current. It monitors the current of the IC's output stage without using an external shunt resistor.
In case of sine-wave drive, when the output current exceeds the current limit detection threshold, driving mode is switched from sine-wave drive (synchronous rectification) to 150° commutation (upper PWM drive). After switching to 150° commutation, the current is limited for every PWM cycle. Current limit control value is 500 mA lower than the current limit detection threshold. After no more current hits the current limit control value, 150° commutation will continue 2 more cycles before driving mode returns to the sine-wave drive.
In case of 150° commutation mode, the current limit detection threshold is as same as the current limit control value. Current is limited for every PWM cycle.

OCPLEVEL [1:0]	Sine-wave drive mode		150° commutation mode	
	Current limit detection threshold	Current limit control value	Current limit detection threshold	Current limit control value
00	1.5 A	1 A	1 A	1 A
01	2 A	1.5 A	1.5 A	1.5 A
10	2.5 A	2 A	2 A	2 A
11	3.5 A	3 A	3 A	3 A

11.6.3. Over Voltage Protection (OVP)

This function is incorporated to prevent VM voltage from rising during motor deceleration. In case of sine-wave drive, driving mode is switched from sine-wave drive (synchronous rectification) to 150° commutation (upper PWM drive) when the VM voltage becomes 17.2 V (typ.) or more. After VM voltage falls to 16.8 V (typ.) or less, 150° commutation continues 2 more cycles before driving mode is switched back to the sine-wave drive.
In case of 150° commutation mode, the over voltage protection is invalid.

11.6.4. Under Voltage Lockout (UVLO)

When the power supply voltage is less than the IC operation voltage, this function turns off the IC operation to avoid malfunction.
It monitors both VM voltage and VREG voltage. When VM voltage is 3.9 V (typ.) or less, or VREG voltage is 3.7 V (typ.) or less, this function is activated. It has a hysteresis of 0.3 V (typ.). IC is resumed to normal operation when VM voltage is over 4.2 V (typ.), and VREG voltage is over 4.0 V (typ.).

11.6.5. Under Voltage Protection for Charge Pump

When the voltage difference between VCP and VM is 3.3 V (typ.) or less, motor outputs are turned off (as high impedance state). It has a hysteresis of 0.3 V (typ.). Motor is resumed to the normal operation when the voltage difference is over 3.6 V (typ.). While this function operates, ALERT pin outputs a low level signal.

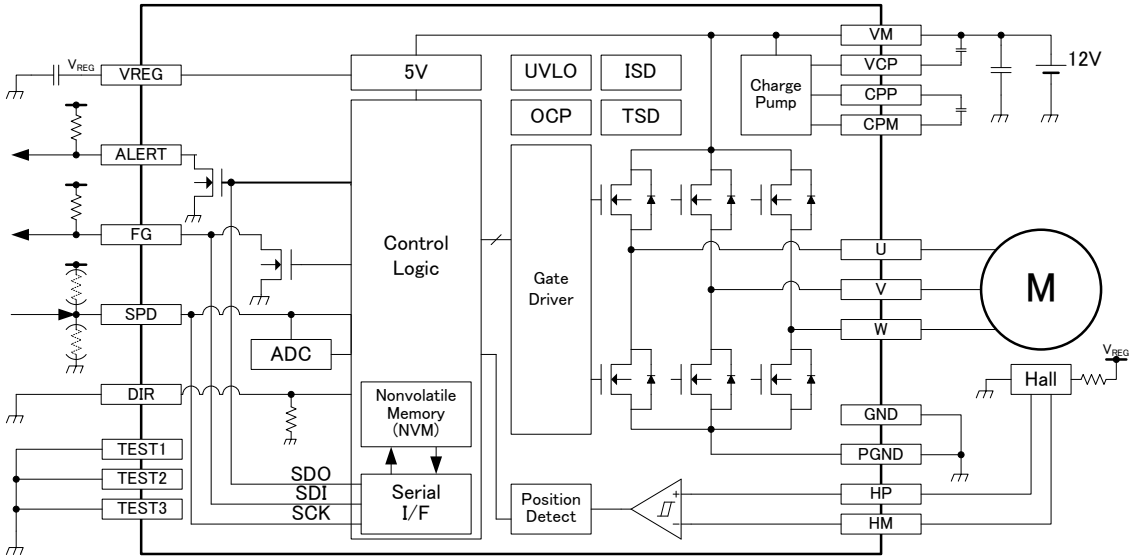
11.6.6. Over Current Protection (ISD)

This function monitors the current of the output power transistor individually and turns off all output stages when the current value exceeds the detection threshold. It prevents the IC from flowing over current continuously. While this function is activated, ALERT pin outputs a low level signal.
Automatic recovery or latch can be selected by using the register. In the case of automatic recovery, output resumes automatically after the output OFF period (t_{OFF}) has passed. If the over current condition continues, the protection cycle repeats. If it repeats 8 times in a row, output will not recover, and all output power transistors keep in off-state. This state is released by re-applying SPD signal or turning on the power again.
In the case of the latch method, output power transistors keep in the off-state after the over current is detected. This state is released by re-applying SPD signal or turning on the power again.

11.6.7. Thermal shutdown (TSD)

Thermal shut down (TSD) is incorporated.
It operates when IC's junction temperature (Tj) exceeds 170°C (typ.). All outputs are turned off. It has a hysteresis of 40°C (typ.). When IC's junction temperature becomes 130°C (typ.) or less, the operation returns automatically. While this function is activated, ALERT pin outputs a low level signal.

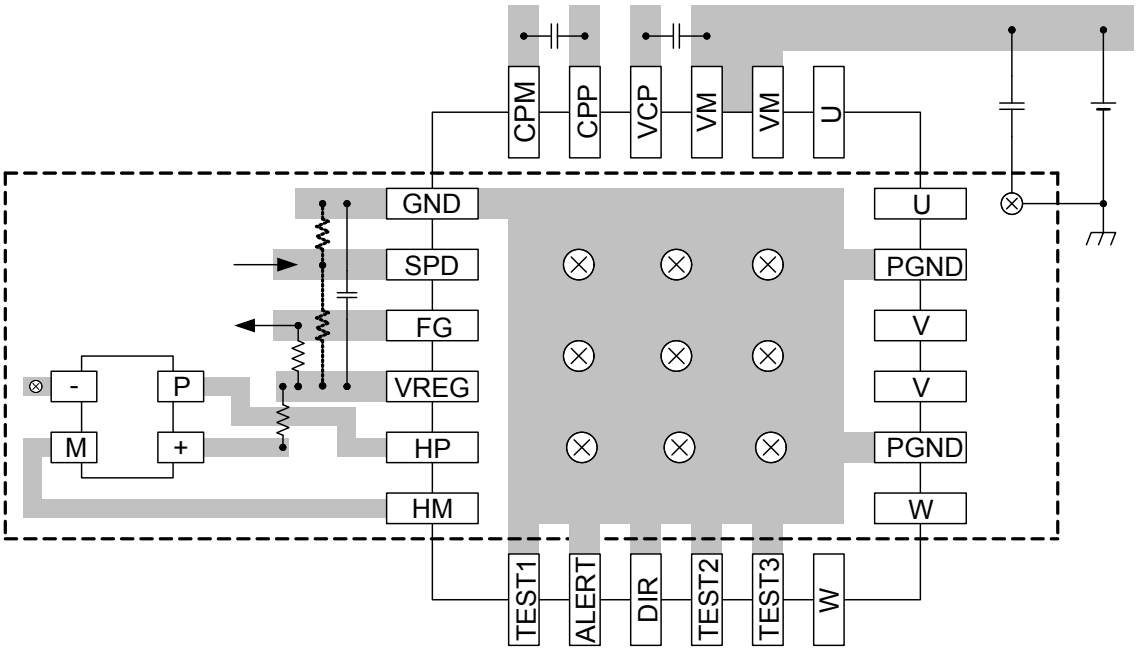
12. Application Circuit Example



Note: TEST pin should be connected to GND pin.
Note: SPD pin should never be left open.
Note: PGND pin and GND pin should be connected to the GND line on the board.
Please refer to “Reference Layout” for details.
Note: A ceramic capacitor of 0.1 μF to 1 μF should be connected to VREG pin. 0.1 μF is recommended.
Note: Recommended capacitor between CPP pin and CPM pin: Ceramic capacitor of 0.01 μF.
Recommended capacitor between VCP pin and VM pin: Ceramic capacitor of 0.1 μF.

Figure 12.1 Application Circuit Example

13. Reference Layout

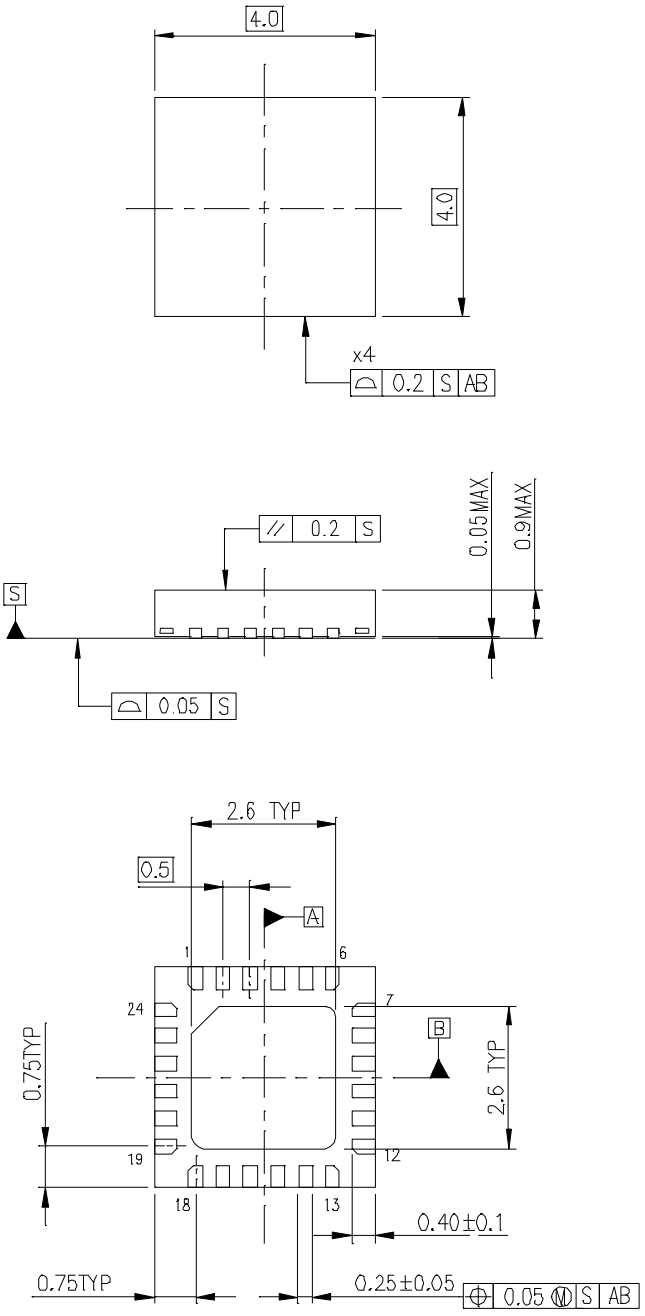


Note: example of ALERT pin is not used

Figure 13.1 Reference Layout

14. Package Dimensions

P-VQFN24-0404-0.50-002 Unit: mm



Weight: 0.04 g (typ.)

Figure 14.1 Package Dimensions

15. IC Usage Considerations

15.1. Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

15.2. Points to remember on handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the over current protection circuits operate against the over current, clear the over current status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Others

Utmost care is necessary in the design of power supply line, GND line, and output line since the IC may be destroyed and occur smoke and fire in some cases by short-circuiting between outputs, to the power supply or ground, or between contiguous pins.

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**