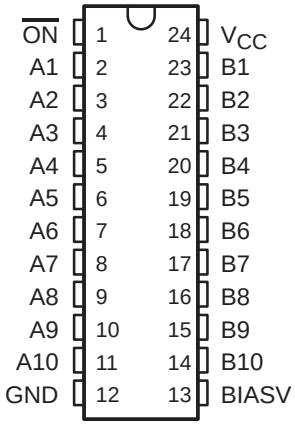
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion**
- **Package Options Include Plastic Shrink Small-Outline (DB, DBQ), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages**

DB, DBQ, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT6800 provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

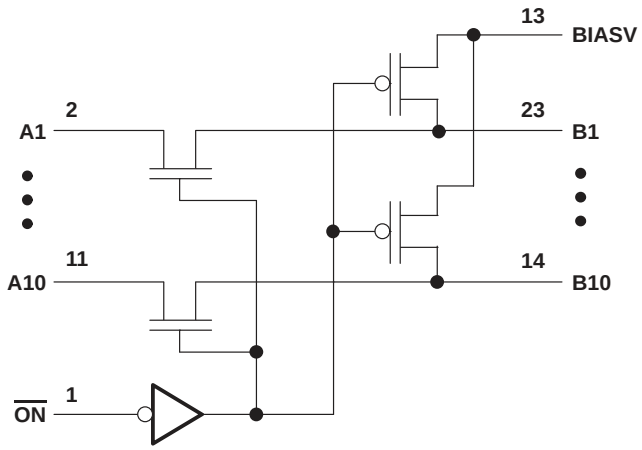
The SN74CBT6800 is organized as one 10-bit switch with a single enable ($\overline{ON}$) input. When $\overline{ON}$ is low, the switch is on and port A is connected to port B. When $\overline{ON}$ is high, the switch between port A and port B is open and the B port is precharged to BIASV through the equivalent of a 10-kΩ resistor.

The SN74CBT6800 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

$\overline{ON}$	B1–B10	FUNCTION
L	A1–A10	Connect
H	BIASV	Precharge

logic diagram (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Bias voltage range, BIASV . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Continuous channel current . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . . 104°C/W
DBQ package . . . . . 103°C/W
DW package . . . . . 81°C/W
PW package . . . . . 120°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
BIASV	Supply voltage	1.3	V_{CC}	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±5	µA
I_O		V_{CC} = 4.5 V,	BIASV = 2.4 V,	V_O= 0	0.25			mA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			50	µA
ΔI_{CC}§	Control inputs	V_{CC} = 3.6 V,	One input at 2.7 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3.5		pF
$C_{o(OFF)}$		V_O = 3 V or 0,	Switch off			4.5		pF
r_{on}¶		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	Ω
				I_I = 30 mA		5	7	Ω
			V_I = 2.4 V,	I_I = 15 mA		10	15	Ω

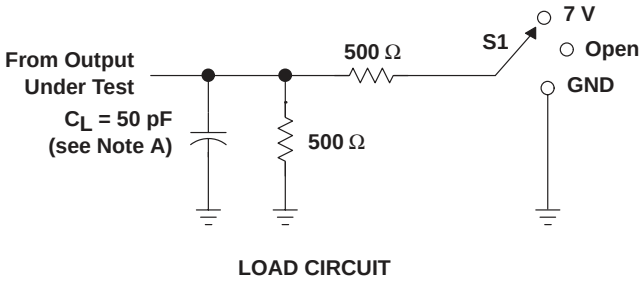
‡ All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}†		A or B	B or A		0.35		0.25	ns
t_{PZH}	BIASV = GND	$\overline{ON}$	A or B		9.1	3.1	8.1	ns
t_{PZL}	BIASV = 3 V				9.6	3.6	8.6	
t_{PHZ}	BIASV = GND	$\overline{ON}$	A or B		5.9	2.7	6.1	ns
t_{PLZ}	BIASV = 3 V				6.4	3	7.3	

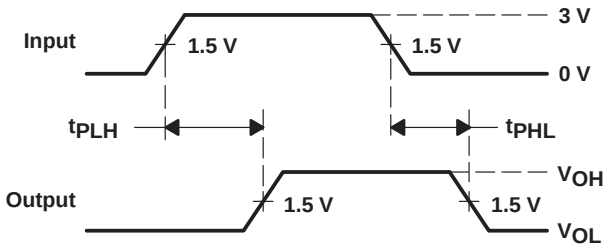
† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

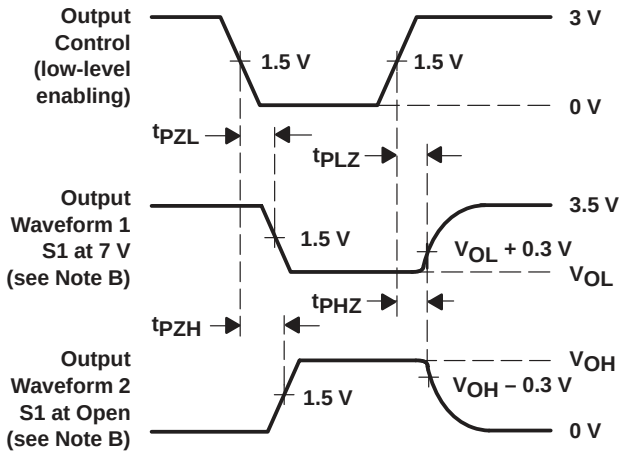


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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PRODUCT FOLDER | PRODUCT INFO: FEATURES | DESCRIPTION | DATASHEETS | PRICING/AVAILABILITY | SAMPLES | APPLICATION NOTES | RELATED DOCUMENTS

PRODUCT SUPPORT: TRAINING

SN74CBT6800, 10-Bit FET Bus Switch With Precharged Outputs For Live Insertion

DEVICE STATUS: ACTIVE

PARAMETER NAME	SN74CBT6800
Voltage Nodes (V)	5
Vcc range (V)	4.0 to 5.5
No. of Bits	10
ron(max) (ohms)	7
tpd(max) (ns)	0.25

FEATURES

Back to Top

- 5- Ω Switch Connection Between Two Ports
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DESCRIPTION

Back to Top

The SN74CBT6800 provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

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TECHNICAL DOCUMENTS

Back to Top

To view the following documents, Acrobat Reader 3.x is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

Back to Top

Full datasheet in Acrobat PDF: scds005j.pdf (61 KB) (Updated: 12/14/1998)
Full datasheet in Zipped PostScript: scds005j.psz (61 KB)

APPLICATION NOTES

Back to Top

View Application Reports for Digital Logic

- 5-V To 3.3-V Translation With The SN74CBTD3384 (SCDA003B - Updated: 03/01/1997)
- Flexible Voltage-Level Translation With CBT Family Devices (SCDA006 - Updated: 07/20/1999)
- Implications of Slow or Floating CMOS Inputs (SCBA004C - Updated: 02/01/1998)
- Low-Voltage Bus-Switch Technology And Applications (SCDA005 - Updated: 12/01/1997)
- Migration From 3.3-V To 2.5-V Power Supplies For Logic Devices (SCEA005 - Updated: 12/01/1997)
- SN74CBTS3384 Bus Switches Provide Fast Connection And Ensure Isolation (SCDA002A - Updated: 08/01/1996)
- TI Logic Solutions for Memory Interleaving With the Intel440BX Chipset (SCCA001 - Updated: 04/08/1999)
- Texas Instruments Crossbar Switches (SCDA001A - Updated: 06/01/1995)
- Texas Instruments Solution for Undershoot Protection for Bus Switches (SCDA007 - Updated: 04/13/2000)
- Understanding Advanced Bus-Interface Products Design Guide (SCAA029, 253 KB - Updated: 05/01/1996)

RELATED DOCUMENTS

Back to Top

- Documentation Rules (SAP) And Ordering Information (SZZU001B, 4 KB - Updated: 05/06/1999)
- Logic Selection Guide Second Half 2000 (SDYU001N, 5035 KB - Updated: 04/17/2000)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- More Power In Less Space - Technical Article (SCAU001A, 850 KB - Updated: 03/01/1996)

SAMPLES

Back to Top

ORDERABLE DEVICE	PACKAGE	PINS	TEMP (ºC)	STATUS	SAMPLES
SN74CBT6800DW	DW	24	-40 TO 85	ACTIVE	Request Samples
SN74CBT6800PWLE	PW	24	-40 TO 85	OBSOLETE	

PRICING/AVAILABILITY

Back to Top

ORDERABLE DEVICE	PACKAGE	PINS	TEMP (ºC)	STATUS	BUDGETARY PRICE US$/UNIT QTY=1000+	PACK QTY	PRICING/AVAILABILITY
SN74CBT6800DBLE	DB	24	-40 TO 85	OBSOLETE			
SN74CBT6800DBQR	DBQ	24	-40 TO 85	ACTIVE	1.09	2500	Check stock or order

SN74CBT6800DBR	DB	24	-40 TO 85	ACTIVE	1.09	2000	Check stock or order
SN74CBT6800DGVR	DGV	24	-40 TO 85	ACTIVE	1.25	2000	Check stock or order
SN74CBT6800DW	DW	24	-40 TO 85	ACTIVE	1.09	25	Check stock or order
SN74CBT6800DWR	DW	24	-40 TO 85	ACTIVE	1.15	2000	Check stock or order
SN74CBT6800PWLE	PW	24	-40 TO 85	OBSOLETE			
SN74CBT6800PWR	PW	24	-40 TO 85	ACTIVE	1.09	2000	Check stock or order

Table Data Updated on: 11/ 15/ 2000