A4963

Sensorless BLDC Controller

FEATURES AND BENEFITS

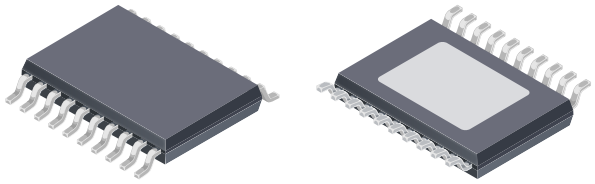
- Three-phase sensorless BLDC motor control FET driver
- Logic level P-N gate drive (P high-side, N low-side)
- 4.2 to 50 V supply range
- Simple block commutation for maximum torque
- Sensorless (bemf sensing) startup and commutation
- Programmable operating modes:
  - □ Integrated speed control
  - □ PWM duty cycle control
  - □ Current mode control
- Cross-conduction prevention
- Wide speed range capability
- Peak current limiting
- Single low-frequency PWM control input
- Single open-drain fault output
- SPI-compatible interface providing:
  - □ Configuration and control
  - □ Programmable dead time
  - □ Programmable phase advance
  - □ Detailed diagnostic reporting

APPLICATIONS

- Pumps
- Fans
- Blowers

PACKAGE:

20-Pin eTSSOP with Exposed Thermal Pad (suffix LP)



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DESCRIPTION

The A4963 is a three-phase, sensorless, brushless DC (BLDC) motor controller for use with external complementary P-channel and N-channel power MOSFETs.

The A4963 can be used as a stand-alone controller communicating directly with an electronic control unit (ECU) or it can be used in a close-coupled system with a local microcontroller (MCU).

The motor is driven using block commutation (trapezoidal drive) where phase commutation is determined, without the need for independent position sensors, by monitoring the motor back-EMF (bemf). The sensorless startup scheme allows the A4963 to operate over a wide range of motor and load combinations.

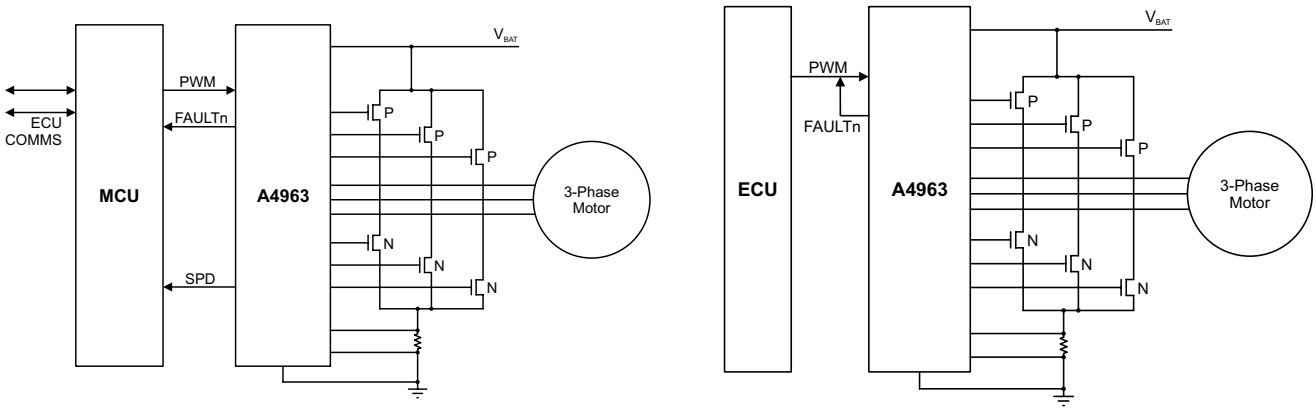
Dedicated circuits allow the A4963 to operate over a wide range of motor speeds, from less than 100 rpm to in excess of 30,000 rpm, depending on the supply voltage and motor capability.

Several operational modes are available including duty-cycle (voltage) control, current (torque limit) control, and closed-loop speed control. Operating mode and control parameters can be altered through an SPI-compatible serial interface.

Motor operation is controlled by a programmable PWM input that can be used to define the motor operating state and provide the proportional input for the selected operating mode.

Integrated diagnostics provide indication of undervoltage, overtemperature, and power bridge faults and can protect the power switches under most short-circuit conditions. Faults are indicated by a single open-drain output than can be used to pull the PWM input low.

The A4963 is provided in a small, thermally enhanced 20-pin TSSOP with exposed thermal pad.



Typical Application – Functional Block Diagrams

SELECTION GUIDE

Part Number	Packing	Package
A4963GLPTR-T	4000 pieces per reel	6.5 mm × 4.4 mm, 1.2 mm nominal height 20-pin TSSOP with exposed thermal pad

Table of Contents

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}		–0.3 to 50	V
Battery-Compliant Inputs		PWM	–0.3 to 50	V
Battery-Compliant Outputs		FAULTn, SPD	–0.3 to 50	V
Logic Inputs		STRn, SCK, SDI	–0.3 to 6.5	V
Logic Outputs		SDO	–0.3 to 6.5	V
Pins GHA, GHB, GHC			V_{BB} – 18 to V_{BB} + 0.3	V
Pins SA, SB, SC			–4 to 51	V
Pins GLA, GLB, GLC			–0.3 to 18	V
Sense Amplifier Inputs	V_{CSI}	CSP, CSM	–4 to 6.5	V
Ambient Operating Temperature Range	T_A		–25 to 150	°C
Maximum Continuous Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

*With respect to GND

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	23*	°C/W
		2-layer PCB with 3 in.^{2} copper each side	44*	°C/W
	$R_{\theta JT}$		2*	°C/W

*Additional thermal information available on the Allegro website.

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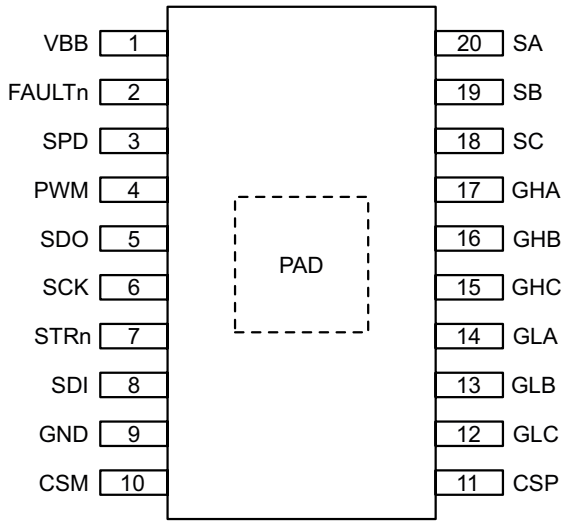
PINOUT DIAGRAM AND TERMINAL LIST TABLE



Package LP, 20-Pin eTSSOP with Exposed Thermal Pad

Terminal List

Name	Number	Function
CSM	10	Sense amp. negative input
CSP	11	Sense amp. positive input
FAULTn	2	Fault output open drain
GHA	17	Phase A HS FET gate drive
GHB	16	Phase B HS FET gate drive
GHC	15	Phase C HS FET gate drive
GLA	14	Phase A LS FET gate drive
GLB	13	Phase B LS FET gate drive
GLA	12	Phase C LS FET gate drive
GND	9	Ground
PWM	4	PWM input, pulled low for fault

Name	Number	Function
SA	20	Phase A motor phase
SB	19	Phase B motor phase
SC	18	Phase C motor phase
SCK	6	Serial clock
SDI	8	Serial data input
SDO	5	Serial data output
SPD	3	Speed output
STRn	7	Serial strobe (chip select) input
VBB	1	Main supply
Pad	–	Connect to ground

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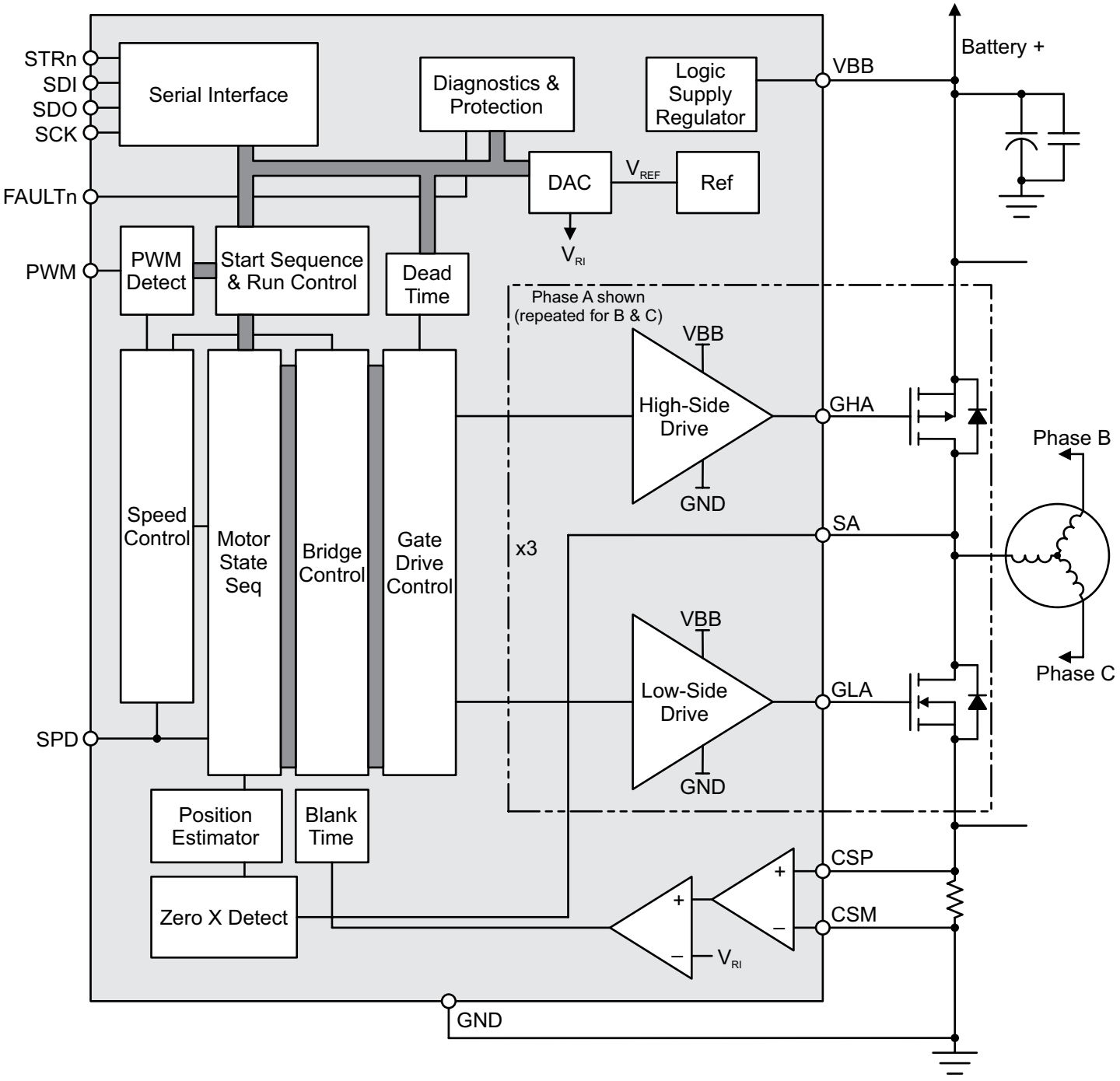

Functional Block Diagram

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ELECTRICAL CHARACTERISTICS: Valid at T_A= 25°C, V_{BB} = 4.2 to 28 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE						
VBB Functional Operating Range [1]	V_{BB}	Operating; outputs active	4.2	–	50	V
		Operating; outputs disabled	4.0	–	50	V
		No unsafe states	0	–	50	V
VBB Quiescent Current	I_{BBQ}	PWM = inactive, V_{BB} = 12 V	–	12	18	mA
System Clock Period	t_{OSC}		47.5	50	52.5	ns
GATE OUTPUT DRIVE						
Turn-On Time	t_r	C_{LOAD} = 500 pF, 20% to 80%, V_{BB} = 12 V	–	200	–	ns
Turn-Off Time	t_f	C_{LOAD} = 500 pF, 20% to 80%, V_{BB} = 12 V	–	200	–	ns
GHx Pull-Up On Resistance	R_{GHUP}	T_J = 25°C, I_{GHx} = –40 mA [2]	12	17	26	Ω
		T_J = 150°C, I_{GHx} = –40 mA [2]	–	26	–	Ω
GHx Pull-Up Current Limit	$I_{GHLIMUP}$		–	300	–	mA
GHx Pull-Down On Resistance	R_{GHDN}	T_J = 25°C, I_{GHx} = 40 mA, V_{BB} = 10 V	23	28	33	Ω
		T_J = 150°C, I_{GHx} = 40 mA, V_{BB} = 10 V	–	40	–	Ω
GHx Pull-Down Current Limit	$I_{GHLIMDN}$		–	100	–	mA
GHx Output Voltage High (Off)	V_{GHH}	–10 µA < I_{GH} < 10 µA	V_{BB} – 0.2	–	–	V
GHx Output Voltage Low (Active)	V_{GHL}	I_{GH} = 10 mA, V_{BB} = 14.5 V	0.9	–	2.6	V
		–10 µA < I_{GH} < 10 µA, V_{BB} ≥ 14.1 V	V_{BB} – 14.1	–	V_{BB} – 11.3	V
		–10 µA < I_{GH} < 10 µA, 9.6 ≤ V_{BB} < 14.1 V	0	–	V_{BB} – 9.4	V
		–10 µA < I_{GH} < 10 µA, V_{BB} < 9.6 V	0	–	0.2	V
GLx Pull-Up On Resistance	R_{GLUP}	T_J = 25°C, I_{GLx} = –40 mA [2], V_{BB} = 10 V	17	24	31	Ω
		T_J = 150°C, I_{GLx} = –40 mA [2], V_{BB} = 10 V	–	38	–	Ω
GLx Pull-Up Current Limit	$I_{GLLIMUP}$		–	140	–	mA
GLx Pull-Down On Resistance	R_{GLDN}	T_J = 25°C, I_{GLx} = 40 mA	15	20	25	Ω
		T_J = 150°C, I_{GLx} = 40 mA	30	40	50	Ω
GLx Pull-Down Current Limit	$I_{GLLIMDN}$		–	160	–	mA
GLx Output Voltage High (Active)	V_{GLH}	–10 µA < I_{GL} < 10 µA, V_{BB} < 8.6 V	V_{BB} – 0.2	–	V_{BB}	V
		–10 µA < I_{GL} < 10 µA, 8.6 ≤ V_{BB} < 13.7 V	8.4	–	V_{BB}	V
		–10 µA < I_{GL} < 10 µA, V_{BB} ≥ 13.7 V	11.2	–	13.7	V
		I_{GL} = –10 mA, V_{BB} = 14.5 V	10.7	–	13.5	V
GLx Output Voltage Low (Off)	V_{GLL}	–10 µA < I_{GL} < 10 µA	–	–	0.2	V
GHx Passive Pull-Down	R_{GHPD}	V_{BB} = 0 V, V_{GH} > –0.1 V	–	500	–	kΩ
GLx Passive Pull-Down	R_{GLPD}	V_{BB} = 0 V, V_{GL} < 0.1 V	–	500	–	kΩ
Turn-Off Propagation Delay [3]	$t_{P(off)}$	Input Change to unloaded Gate output change; Direct mode	200	250	400	ns
Turn-On Propagation Delay [3]	$t_{P(on)}$	Input Change to unloaded Gate output change; Direct mode	200	250	400	ns
Dead Time (Turn-Off to Turn-On Delay) [3]	t_{DEAD}	Default power-up value	0.9	1.0	1.1	µs

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_A= 25°C, V_{BB} = 4.2 to 28 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC INPUTS AND OUTPUTS						
Input Low Voltage	V_{IL}		–	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	–	V
Input Hysteresis	V_{Ihys}		150	550	–	mV
Input Pull-Down Resistor (PWM, SDI, SCK)	R_{PD}		30	50	70	kΩ
Input Pull-Up Resistor (STRn)	R_{PU}		30	50	70	kΩ
Output Low Voltage (SDO)	V_{OL}	I_{OL} = 1 mA	–	0.2	0.4	V
Output High Voltage (SDO)	V_{OH}	I_{OL} = 1 mA[2]	2.4	3.0	–	V
Output Leakage[2] (SDO)	I_O	0 V < V_O < 3.3 V, STRn = 1	–1	–	1	µA
Output Low Voltage (FAULTn, SPD)	V_{OL}	I_{OL} = 4 mA, FAULTn active	–	0.2	0.4	V
Output Current Limit (FAULTn, SPD)	I_{OLIM}	0 V < V_O < 15 V, FAULTn active	–	10	15	mA
		15 V ≤ V_O < 50 V, FAULTn active	–	–	2	mA
Output Leakage[2] (FAULTn, SPD)	I_O	0 V < V_O < 12 V, FAULTn inactive	–1	–	1	µA
		12 V ≤ V_O < 50 V, FAULTn inactive	–	–	1.7	mA
LOGIC I/O – TIMING PARAMETERS						
PWM Duty Detect Frequency Range	f_{PWD}		5	–	1000	Hz
PWM Brake Time	t_{BRK}		500	–	–	µs
SERIAL INTERFACE – TIMING PARAMETERS						
Clock High Time	t_{SCKH}	A in Figure 1	50	–	–	ns
Clock Low Time	t_{SCKL}	B in Figure 1	50	–	–	ns
Strobe Lead Time	t_{STLD}	C in Figure 1	30	–	–	ns
Strobe Lag Time	t_{STLG}	D in Figure 1	30	–	–	ns
Strobe High Time	t_{STRH}	E in Figure 1	300	–	–	ns
Data Out Enable Time	t_{SDOE}	F in Figure 1	–	–	40	ns
Data Out Disable Time	t_{SDOD}	G in Figure 1	–	–	30	ns
Data Out Valid Time from Clock Falling	t_{SDOV}	H in Figure 1	–	–	40	ns
Data Out Hold Time from Clock Falling	t_{SDOH}	I in Figure 1	5	–	–	ns
Data In Setup Time to Clock Rising	t_{SDIS}	J in Figure 1	15	–	–	ns
Data In Hold Time from Clock Rising	t_{SDIH}	K in Figure 1	10	–	–	ns
MOTOR STARTUP PARAMETERS						
Hold Duty Cycle	D_H	Default power-up value	35.5	37.5	39.5	%
Hold Time	t_{HOLD}	Default power-up value	15.2	16	16.8	ms
Start Speed	f_{ST}	Default power-up value	7.6	8	8.4	Hz
Start Duty Cycle	D_{ST}	Default power-up value	47.5	50	52.5	%

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_A= 25°C, V_{BB} = 4.2 to 28 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
MOTOR RUN PARAMETERS						
Phase Advance (in Electrical Degrees)	θ_{ADV}	Default power-up value	14	15	16	°
Position Control Proportional Gain	K_{CP}	Default power-up value	–	1	–	–
Position Control Integral Gain	K_{CI}	Default power-up value	–	1	–	–
Speed Control Proportional Gain	K_{SP}	Default power-up value	–	1	–	–
Speed Control Integral Gain	K_{SI}	Default power-up value	–	1	–	–
Maximum Control Speed	f_{MX}	Default power-up value	3112.9	3276.7	3440.5	Hz
Speed Error	Ef_{CCMX}		–5	–	5	%
CURRENT LIMITING						
Current Limit Threshold Voltage Range	V_{ILIM}	$V_{ILIM} = V_{CSP} – V_{CSM}$	12.5	–	200	mV
Current Limit Threshold Voltage	V_{ILIM}	Default power-up value	–	200	–	mV
Current Limit Threshold Voltage Error [7]	E_{ILIM}	V_{ILIM} = 200 mV	–5%	–	5%	%FS
Fixed Off-Time	t_{PW}	Default power-up value	47.9	50.4	52.9	µs
Blank Time	t_{BL}	Default power-up value	3.04	3.2	3.36	µs
PROTECTION						
VBB Undervoltage Lockout	V_{BBON}	V_{BB} rising	4.2	4.4	4.6	V
	V_{BBOFF}	V_{BB} falling	3.8	4.0	4.2	V
VBB POR Voltage	V_{BBR}	V_{BB} falling	–	3.2	3.5	V
VBB POR Voltage Hysteresis	V_{BBRHys}		–	100	–	mV
VDS Threshold	V_{DST}	Default power-up value	1325	1550	1705	mV
VDS Threshold Max, High Side	V_{DST}	$V_{BB} \geq 6$ V	–	–	1705	mV
		5 V ≤ V_{BB} < 6 V	–	–	500	mV
VDS Threshold Max, Low Side	V_{DST}	$V_{BB} \geq 4.2$ V	–	–	1705	mV
VDS Threshold Offset [4][5]	V_{DSTO}	$V_{DST} \geq 1$ V	–	±100	–	mV
		$V_{DST} \leq 1$ V	–150	±50	150	mV
Temperature Warning Threshold	T_{JWH}	Temperature increasing	125	135	145	°C
Temperature Warning Hysteresis	T_{JWHhys}		–	15	–	°C
Overtemperature Threshold	T_{JF}	Temperature increasing	170	175	180	°C
Overtemperature Hysteresis	T_{JHyst}	Recovery = $T_{JF} – T_{JHyst}$	–	15	–	°C

[1] Function is correct but parameters are not guaranteed above or below the general limits (6-28 V).
[2] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device terminal.
[3] See Figure 2 for gate drive output timing.
[4] As V_{SX} decreases, high-side fault occurs if $(V_{BAT} – V_{SX}) > (V_{DST} + V_{DSTO})$.
[5] As V_{SX} increases, low-side fault occurs if $(V_{SX}) > (V_{DST} + V_{DSTO})$.
[6] See Figures 4 and 5 for V_{DS} monitor timing.
[7] Current limit threshold voltage error is the difference between the target threshold voltage and the actual threshold voltage, referred to maximum full-scale (100%) current: $E_{ILIM} = 100 \times (V_{ILIMActual} – V_{ILIM})/200\%$ (V_{ILIM} in mV).

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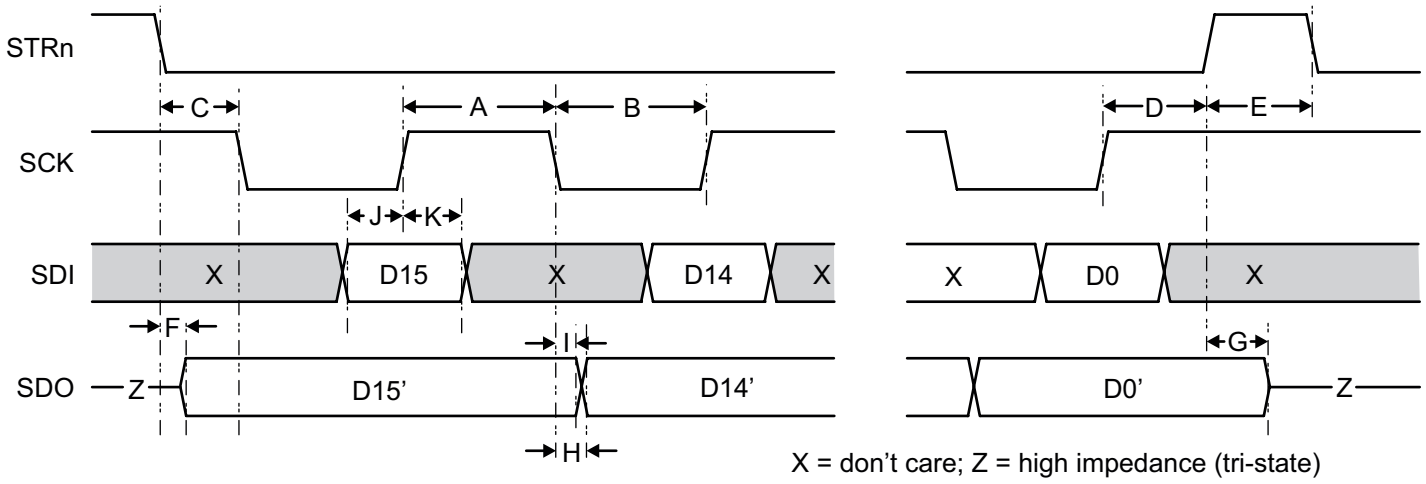

Figure 1: Serial Interface Timing

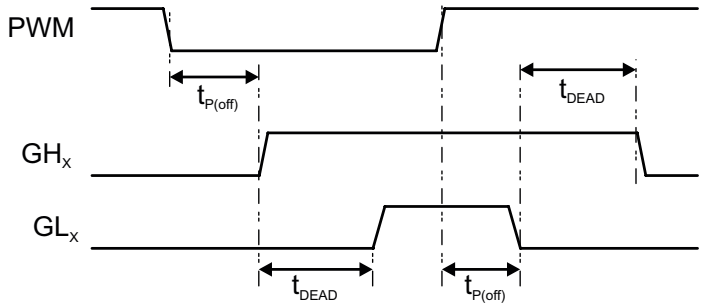

Figure 2: Gate Drive Timing

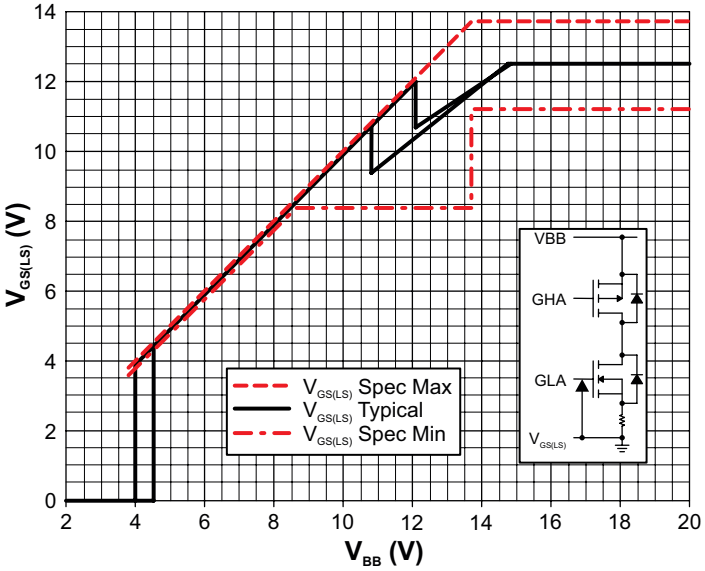

Figure 3: Typical Low-Side Gate Drive vs. V_{BB}

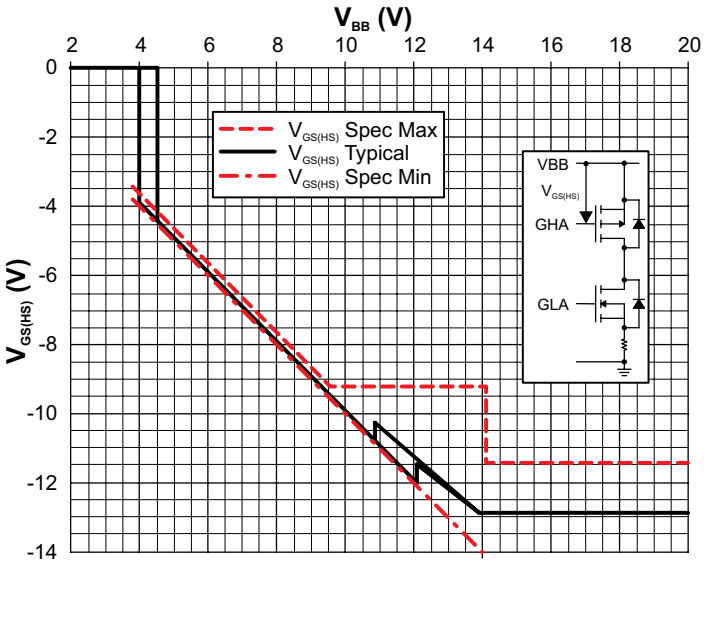

Figure 4: Typical High-Side Gate Drive vs. V_{BB}

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VDS Fault Monitor Timing Diagrams

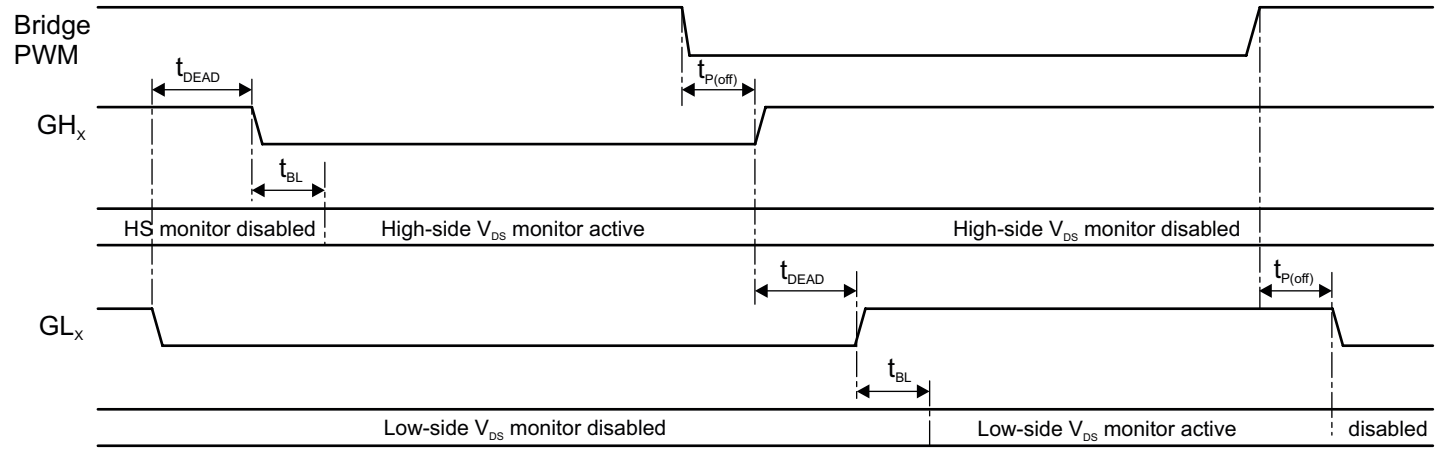

Figure 5: VDS Fault Monitor – Blank Mode Timing (VDQ = 1)

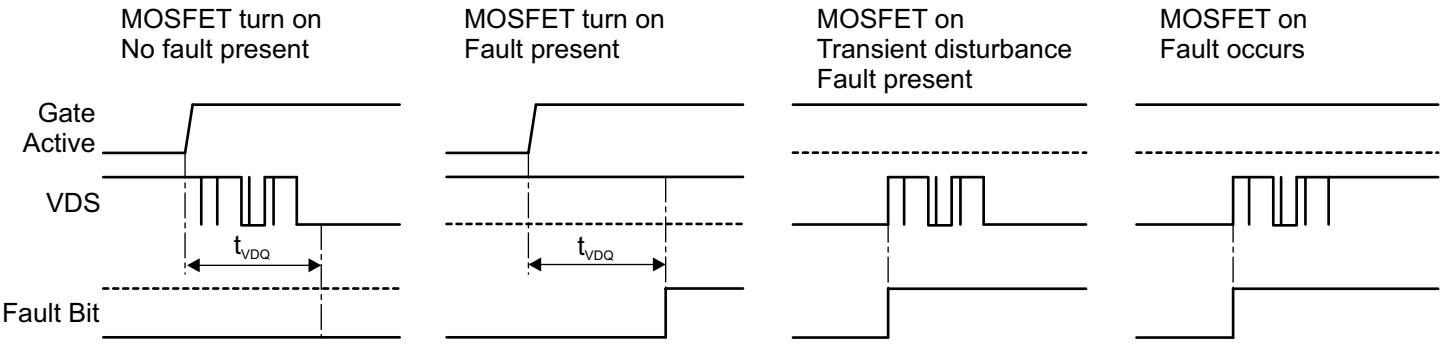

Figure 6: VDS Fault Monitor – Blank Mode Timing (VDQ = 1)

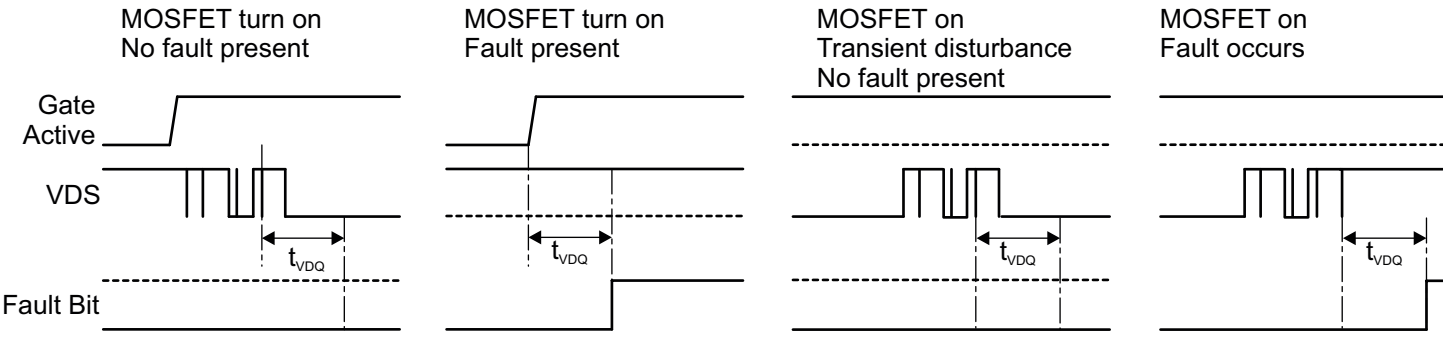

Figure 7: VDS Fault Monitor – Debounce Mode Timing (VDQ = 0)

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Closed-Loop Control Diagrams

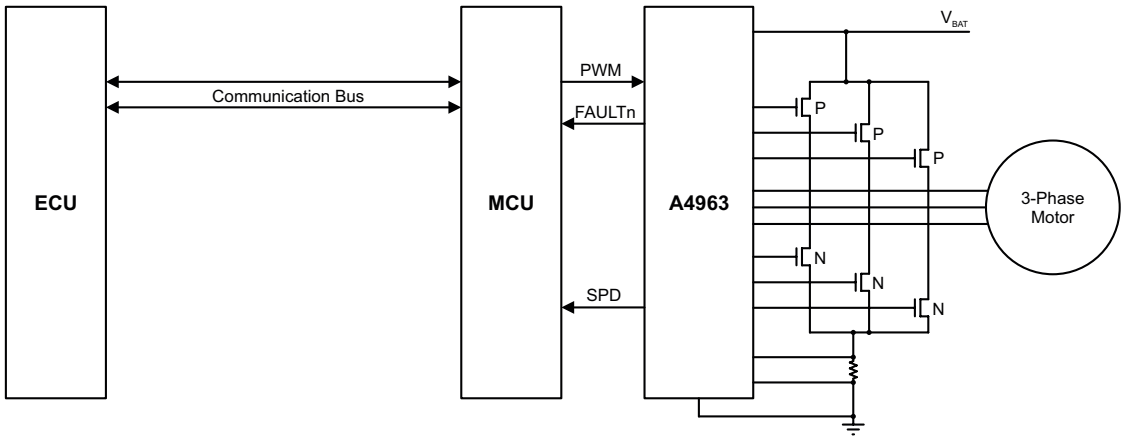

Figure 8: Local Closed-Loop Control with High Level ECU Communications

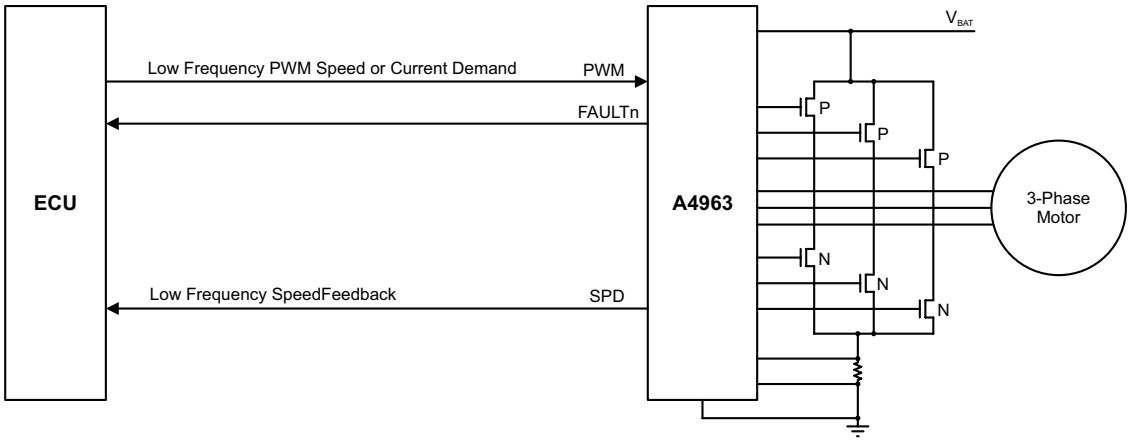

Figure 9: Remote Closed-Loop Control

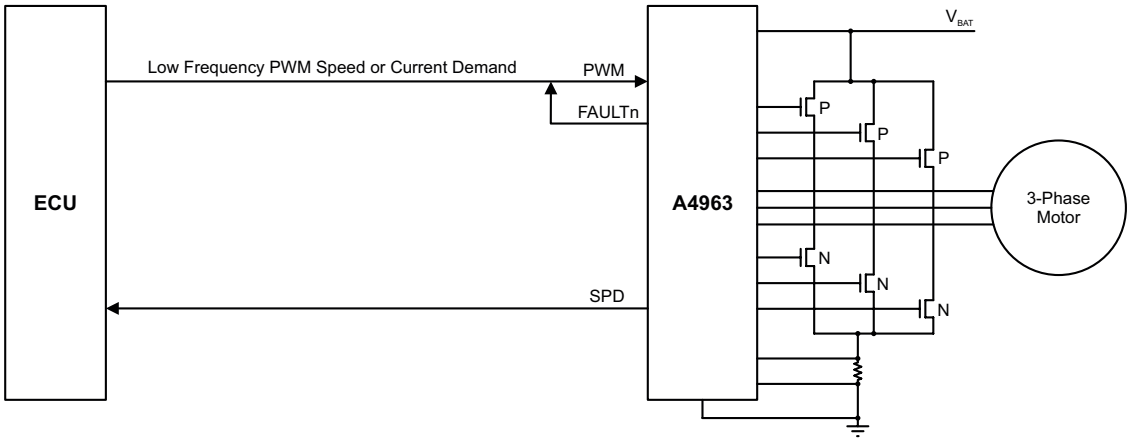

Figure 10: Remote Single-Wire Command with Integrated Closed-Loop Control

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FUNCTIONAL DESCRIPTION

The A4963 is a three-phase, sensorless, brushless DC (BLDC) motor controller for use with external complementary P-channel and N-channel power MOSFETs. The motor is driven using block commutation (trapezoidal drive), where phase commutation is determined by a proprietary, motor back-emf (bemf) sensing technique. The motor bemf is sensed to determine the rotor position without the need for independent position sensors. An integrated sensorless startup scheme allows a wide range of motor and load combinations.

Motor current is provided by six external power MOSFETs arranged as a three-phase bridge with three N-channel low-side MOSFETs and three P-channel high-side MOSFETS. The A4963 provides six high current gate drives, three high-side and three low-side, capable of driving a wide range of MOSFETs. The maximum MOSFET drive voltage is internally limited under all supply conditions to protect the MOSFET from excessive gate-source voltage without the need for an external clamp circuit. The minimum MOSFET drive voltage is determined by the supply voltage allowing operation at very low voltage by using logic-level MOSFETs.

Three basic operational modes are available: open-loop speed (voltage) control, closed-loop torque (current) control, and closed-loop speed control. Operating mode and control parameters can be altered through an SPI-compatible serial interface.

Motor operation is controlled by a single, low-frequency PWM input that determines the motor operating state and provides proportional input for the selected operating mode.

Startup (inrush) current and peak motor current are limited by an integrated fixed off-time PWM current limiter. The maximum current limit is set by a single external sense resistor, and the active current limit can be modified through the serial interface.

Integrated diagnostics provide indication of undervoltage, overtemperature, and power bridge faults and can be configured to protect the power FETs under most short-circuit conditions. A single FAULT flag is provided, and detailed diagnostics are available through the serial interface.

Specific functions are described more fully in following sections.

Input and Output Terminal Functions

VBB: Main power supply for internal regulators and charge pump. The main power supply should be connected to VBB through a reverse voltage protection circuit and should be decoupled with ceramic capacitors connected close to the supply and ground terminals.

GND: Analog reference, Digital and power ground. Connect to supply ground—see layout recommendations.

GHA, GHB, GHC: High-side, gate drive outputs for external P-channel MOSFETs.

SA, SB, SC: Motor phase connections. These terminals sense the voltages switched across the load.

GLA, GLB, GLC: Low-side, gate drive outputs for external N-channel MOSFETs.

CSP, CSM: Differential current sense amplifier inputs. Connect directly to each end of the sense resistor using separate PCB traces.

PWM: Programmable PWM input to control the motor operating mode and the proportional duty cycle input for the selected control mode. Can be shorted to ground or VBB without damage.

SPD: Open-drain speed output indicator. Output frequency is programmable. It can be the commutation frequency (TACHO) or the electrical cycle frequency (FG). Can be shorted to ground or VBB without damage.

FAULTn: Open-drain active-low fault indicator. Can be connected to PWM input to provide single wire interface to a controlling ECU. Can be shorted to ground or VBB without damage.

SDI: Serial data input. 16-bit serial word input msb first.

SDO: Serial data output. High impedance when STRn is high. Outputs bit 15 of the diagnostic register, the fault flag, as soon as STRn goes low.

SCK: Serial clock. Data is latched in from SDI on the rising edge of CLK. There must be 16-rising edges per write and SCK must be held high when STRn changes.

STRn: Serial data strobe and serial access enable. When STRn is high, any activity on SCK or SDI is ignored and SDO is high impedance, allowing multiple SDI slaves to have common SDI, SCK, and SDO connections.

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Motor Drive System

The motor drive system consists of three half-bridge gate drive outputs, each driving one leg of an external 3-phase MOSFET power bridge. The state of the gate drive outputs is determined by a state sequencer with six possible states. These states are shown in Table 1 and change in a set sequence. The effect of these states on the motor phase voltage is illustrated in Figure 11. This sequence creates a moving magnetic field in the poles of the stator, against which the permanent magnets in the rotor can react to produce torque at the motor output shaft.

The point at which the state of the gate outputs change is defined as the commutation point and must occur each time the magnetic poles of the rotor reach a specific point in relation to the poles of the stator. This point is determined by a closed-loop commutation controller consisting of a position estimator and commutation timer. This controller uses the output of a complete self-contained bemf sensing scheme to determine the actual position of the motor and adjust the estimated position and commutation frequency to synchronize with the rotor poles in the motor.

The motor speed can be determined by monitoring the SPD output. There are two options for the signal available at the SPD terminal selected via the serial interface. The default is a signal, defined as FG, at the frequency of the complete electrical cycle (the 6-state sequence in Table 1). FG goes high on entering state 1 and goes low on entering state 4. The alternative is a square wave signal, defined as TACHO, at the commutation frequency with the falling edge synchronized to the commutation point. FG and TACHO are shown in Figure 11.

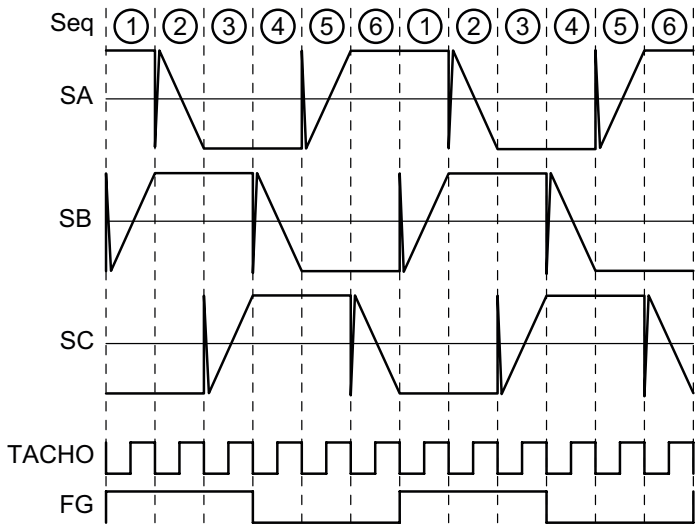

Figure 11: Motor Phase State Sequence

In the A4963, motor speed is always defined as the frequency of the electrical cycle, f_S. This is the same frequency as the FG signal, if selected, on the SPD output.

The actual mechanical speed of the motor, ω, will depend on the number of pole pairs, N_{PP}, and is determined by:

$$\omega = \frac{60 \times f_s}{N_{PP}}$$

where f_S is in Hz and ω is in rpm (mechanical revolutions per minute).

Table 1: Control and Phase Sequence

Control Bits				State	Motor Phase			Gate Drive Outputs						Mode
RUN	BRK	DIR=1	DIR0		SA	SB	SC	GHA	GLA	GHB	GLB	GHC	GLC	
1	0	↑	↓	1	HI	Z	LO	ON	OFF	OFF	OFF	OFF	ON	Run
1	0			2	Z	HI	LO	OFF	OFF	ON	OFF	OFF	ON	
1	0			3	LO	HI	Z	OFF	ON	ON	OFF	OFF	OFF	
1	0			4	LO	Z	HI	OFF	ON	OFF	OFF	ON	OFF	
1	0			5	Z	LO	HI	OFF	OFF	OFF	ON	ON	OFF	
1	0			6	HI	LO	Z	ON	OFF	OFF	ON	OFF	OFF	
0	x	x	x	x	Z	Z	Z	OFF	OFF	OFF	OFF	OFF	OFF	Coast
1	1	x	x	x	LO	LO	LO	OFF	ON	OFF	ON	OFF	ON	Brake

x ≡ don't care, HI ≡ high-side FET active, LO ≡ low-side FET active, Z ≡ high impedance, both FETs off
ON ≡ high-side output (GHx) low, low-side output (GLx) high
OFF ≡ high-side output (GHx) high, low-side output (GLx) low

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Rotor Position Sensing Using Motor bemf

A key element of the controller is the back-emf zero crossing detector. Determining the rotor position using direct bemf sensing relies on the accurate comparison of the voltage on the undriven (tri-state) motor phase (indicated by Z in Table 1) to the voltage at the center tap of the motor, approximated using an internally generated reference voltage. The bemf zero crossing—the point where the voltage of the undriven motor winding crosses the reference voltage—occurs when a pole of the rotor is in alignment with a pole of the stator and is used as a positional reference for the commutation controller.

The internally generated zero crossing reference voltage follows the bridge drive voltage levels to allow bemf crossing detection during both PWM-on and PWM-off states. The comparator adds hysteresis to the reference voltage in order to reduce the effect of low-level noise on the comparison. The effects of large signal noise, such as switching transients, are removed by digital filtering.

When the motor is running at a constant speed, with no phase advance, this zero crossing should occur approximately halfway through one commutation period. The commutation controller compares the expected zero crossing point to the detected zero crossing point and adjusts the phase and frequency of the position estimator and commutation timer to minimize the difference between the expected and actual crossing points over a number of commutation periods.

The controller also allows the commutated magnetic field of the stator to be out of phase with the rotor. The expected zero crossing point is adjusted to be later in the commutation period, and the controller modifies the commutation timing to minimize the difference between the estimated and measured bemf zero-crossing points. This is known as phase advance, and the amount of phase advance in electrical degrees is set (up to 28°) by the contents of the PA[3:0] variable.

In any electric motor, a force is produced by the interaction of rotor magnetic poles and stator magnetic field. The motor and the commutation system are designed such that a portion of this force is tangential to the rotor and will produce a rotational torque. Applying phase advance will have the effect of changing the direction of force vector relative to the rotor and will increase the tangential component of the force. This will increase the effectiveness of the torque produced by the stator field and permit a higher motor speed than for no phase advance at the same input demand.

The controller uses proportional and integral feedback (PI control) to provide a fast response with good long-term accuracy. The amount of proportional and integral feedback can be adjusted independently by setting the CP[3:0] and CI[3:0] variables respectively, through the serial interface. This allows the dynamic response to be tuned to different system conditions if required; however, the default values for CP and CI will achieve optimum results in most applications.

The control method used is tolerant to missing bemf zero crossing detections and will simply change the speed of the applied commutation sequence by an amount determined by the proportional gain of the control loop. This results in a much more stable system that does not lose synchronization due to impulse perturbations in the motor load torque. It also means that real loss of synchronization cannot be determined by missing bemf zero crossing detection and has to be determined in a different way.

In the extreme case, when a motor stalls due to excessive load on the output, there will be no bemf zero crossing detection, and the frequency of the commutation sequence will be reduced each commutation point to try and regain synchronization. If the resulting speed reduces below the low speed threshold, then the controller will enter the loss of synchronization state and either stop or attempt to restart the motor. The low speed threshold will be 25% of the start speed set by the value of the SS[3:0] variable.

In some cases, rather than a complete stall, it is also possible for the motor to vibrate at a whole fraction (subharmonic) of the commutation frequency produced by the controller. In this case, the controller will still detect the bemf zero crossing, but at a rate much higher than the motor is capable of running. If the resulting speed increases above the overspeed threshold, then the controller will enter the loss of synchronization state and either stop or attempt to restart the motor. The overspeed threshold is determined by the product of the maximum limit ratio and the maximum speed. The maximum limit ratio is set by the value of the SH[1:0] variable, and the maximum speed is by set the value of the SMX[2:0] variable.

The maximum speed, defined by SMX, determines the motor speed for 100% input when operating in the closed-loop speed control mode. However, it must still be set to a suitable level to provide an appropriate overspeed threshold for all other operating modes.

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Startup

To correctly detect the zero crossing, the changing motor bemf on any phase must be detectable when that phase is not being driven. When the motor is running at a relatively constant speed, this is ensured by the commutation scheme used. However, during startup, the motor must be accelerated from rest in such a way that the bemf zero crossing can be detected. Initially, as the motor is started, there is no rotor position information from the bemf sensor circuits, and the motor must be driven using forced commutation.

To ensure that the motor startup and sensorless bemf capture is consistent, the start sequencer always forces the motor to a known hold position and for a programmable hold time by driving phase C low and applying a programmable duty cycle PWM signal to phase A. The hold time is defined by the contents of the HT[3:0] variable and the hold duty cycle by the contents of the HD[3:0] variable.

Following the hold time, the motor phases are commutated to the next state to force the motor to start in the required direction, and the PWM duty cycle is changed to the startup duty cycle set by the contents of the SD[3:0] variable. For the forwards direction when DIR = 0, phase C will be held low, and the startup duty cycle is applied to phase B. For the reverse direction when DIR = 1, phase B will be held low, and the startup duty cycle is applied to phase A. The duration of the first commutation period is determined by the start speed set by the value of the SS[3:0] variable. This value is also used as the starting speed for the closed-loop commutation controller and for the speed controller if selected.

At the end of the second commutation period, control is passed to the closed-loop commutation controller, and the start sequencer is reset. The SPD terminal will immediately output FG or TACHO as selected by the SPO variable.

During the start sequence, it is possible for the motor to be rotating out of synchronization with the commutated field, as sequenced by the A4963. In some cases, it is possible for the motor bemf produce a voltage that reinforces, rather than opposes, the supply voltage. If this occurs, then the slow decay mode used during running will not be able to maintain control of the motor current during the PWM off-time, and the current may rise uncontrollably. To overcome this effect, the A4963 uses a mixed decay mode PWM during startup to keep the current under control. Mixed decay is where the bridge is first switched into fast decay mode then into slow decay after a portion of the PWM period. This applies a reverse voltage to the motor phase winding and counteracts the effect of the out-of-phase bemf voltage.

The portion of the PWM period during which fast decay is used is called percent fast decay (PFD). Two values of PFD—12.5% or 25%—can be selected by the PFD variable in configuration register 1. Mixed decay is applied automatically for the first sixteen full electrical cycles (96 commutation periods).

Following the start sequence, the commutation controller is expected to attain synchronization with the motor and stabilize at a running frequency to match the control input demand. If synchronization is not achieved, the commutation controller will either reduce the resulting motor frequency below the low-speed limit or increase it above the overspeed limit. If this happens, the A4963 will indicate a loss of synchronization condition by repeatedly pulling the FAULTn output active low for three PWM periods and inactive for three periods.

If a loss of synchronization occurs, the RUN and RSC bits are set to 1, and the PWM signal applied to the PWM input terminal is not 0% (or is not less than 25% for closed-loop speed control mode) then the FAULTn output will go active low for three PWM periods, inactive for three periods, then repeat this sequence before the start sequencer is reset and the start sequence initiated as shown in Figure 4. This cycle will continue until stopped by holding the PWM terminal in the inactive state or setting either RUN bit or the RSC bit to 0.

If a loss of synchronization occurs and RSC = 0, the FAULTn output will continue to indicate loss of synchronization until the PWM signal applied to the PWM input terminal is 0% (or <25% for closed-loop speed control mode) or the RUN bit is set to 0.

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Motor Control

The running state, direction, and speed of the motor are controlled by a combination of commands through the serial interface and by the signal on the PWM terminal.

The serial interface provides three control bits: RUN, DIR, and BRK.

When RUN = 1, the A4963 is allowed to run the motor or to commence the startup sequence. When RUN = 0, all gate drive outputs go low, no commutation takes place, and the motor is allowed to coast. RUN = 0 overrides all other control inputs.

The DIR bit determines the direction of rotation. Forward is defined as DIR = 0, and the phase state sequence increments as defined in Table 1. Reverse is when DIR = 1, and the phase state sequence decrements.The BRK bit can be set to apply an electrodynamic brake which will decelerate a rotating motor. It will also provide some holding torque for a stationary motor. When RUN = 1, BRK = 1, and the PWM is inactive for longer than the PWM brake time, all low-side MOSFETs will be turned on, and all high-side MOSFETs turned off, effectively applying a short between the motor windings. This allows the reverse voltage generated by the rotation of the motor (motor bemf) to set up a current in the motor phase windings that will produce a braking torque. This braking torque will always oppose the direction of rotation of the motor. The strength of the braking or holding torque will depend on the motor parameters. No commutation takes place during braking, and no current control is available. Care must be taken to ensure that the braking current does not exceed the capability of the low-side MOSFETs.

There are three motor control methods included in the A4963. These are:

- open-loop speed (voltage) control
- closed-loop torque (current) control
- closed-loop speed control

In addition, the open-loop speed control can be regulated using direct or indirect PWM duty cycle control.

PWM Control Input

The PWM control input can be used to provide a proportional demand input to the A4963 for the selected control mode. It can be driven between ground and VBB and has hysteresis and a noise filter to improve noise performance.

The sense of the PWM input can be changed from active high to active low by changing the IPI variable in configuration register 1. When IPI is 0, the default value, then the PWM input is active high. When IPI is 1, then the PWM input is inverted and active low. This applies to all operating modes and input modes.

In the direct open-loop speed control mode, when IPI is 0, the signal on the PWM terminal is applied directly to the power bridge. When IPI is 1 in direct mode, the the signal on the PWM terminal is inverted before being applied directly to the power bridge.

In indirect mode, a low-frequency signal between 5 Hz and 1 kHz is applied to the PWM terminal. The duty cycle of this signal is measured with an 8-bit counter system giving better than 0.5% resolution in duty cycle. When IPI is 0, the duty cycle is the ratio of the PWM high duration to the PWM period measured between falling edges of the PWM input signal. When IPI is 1, the duty cycle is the ratio of the PWM low duration to the PWM period measured between rising edges of the PWM input signal. The measured duty cycle is then used to set the bridge PWM duty cycle for the open-loop speed control mode or to provide the torque (current) reference or speed reference for the closed-loop control modes.

For systems where the operation of the A4963 is managed by a remote ECU using a single wire interface, it is also possible to connect the FAULTn terminal directly to the PWM terminal. This can be used to indicate to the ECU that a critical fault is present that has stopped the operation of the motor by the FAULTn output pulling the PWM input to ground continuously or with a variable-width pulse sequence.

Direct Open-Loop Speed (Voltage) Control

Direct access to the power bridge PWM control allows an external local microcontroller to provide application specific speed control and more advanced communications such as CAN bus or LIN bus. In this case, the microcontroller will be closely coupled to the A4963 and will vary the duty cycle of the PWM signal applied directly to the bridge in order to control the motor. The motor speed will be proportional to the duty cycle of this signal, but will also vary with the mechanical load and the supply voltage.

The A4963 will only provide current limiting using the internal closed-loop current regulator. The motor speed can be determined by monitoring the SPD output terminal. This output can be configured to provide a square wave at the commutation frequency or at the electrical cycle frequency.

The signal input to the PWM terminal must be at the required

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PWM frequency for the motor and operating parameters. Typically, this will be between 10 and 20 kHz for most motors. For some very high-speed motors, this may have to be increased significantly.

When the PWM input is in the inactive state (low when IPI = 0, high when IPI = 1), the three-phase bridge is switched to one of three current decay recirculation modes depending on the value of the RM[2:0] variable. Slow decay synchronous recirculation can be high-side, low-side, or auto, which is a combination of the two controlled by the commutation state. The bridge can also be driven in fast decay mode without synchronous rectification. These modes are described further in the Gate Drive and Bridge PWM section below. During startup, mixed decay is always used as described in the Startup section above.

To avoid undesirable interaction between the external PWM signal applied to the PWM terminal and the internal current regulator PWM, it is necessary to set the internal PWM off-time, defined by the value of PW[4:0], to be longer than the external PWM period. This will ensure that the internal current regulator can only ever switch to PWM off and will avoid additional bridge switching and current ripple.

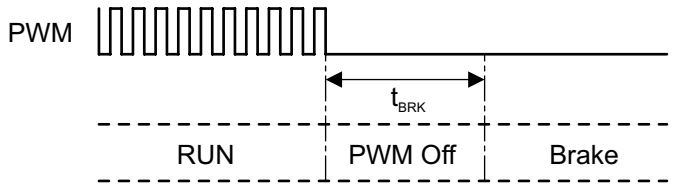

Figure 12: PWM Brake Timing – Direct Mode PWM

When operating in the direct mode, holding the PWM terminal inactive for longer than the PWM brake time (t_{BRK}), as shown, for IPI = 0 in Figure 12, will force a brake condition if BRK = 1 and RUN = 1.

In most cases, when PWM terminal is held inactive, the motor current will decay to zero before the end of the brake time, and the motor will coast with no drive or brake torque present before the brake condition is enabled. Once the brake condition is enabled, all low-side MOSFETs in the bridge will be switched on to short the motor phase windings to each other. If the motor is still running at high speed, this will produce a very high braking current in the windings and in the MOSFETs. It is critical that the MOSFETs are selected to be able to handle this current without damage.

In cases where there is a high inertial load, and the motor cannot be allowed to coast to a stop, it is advisable to first reduce the motor speed by decreasing the demand to the A4963 by reducing the PWM input duty cycle. This will slow the motor faster than coasting but not as fast as a brake condition. Once the motor speed has be reduced to a safe level, then the brake condition can be applied.

Once enabled, the brake condition will be held until the PWM terminal is changed to its active state. At this point, if the motor operation is enabled, with RUN = 1 and BRK = 0, then the A4963 will initiate a start sequence. During the start sequence, the duty cycle of the signal on the PWM terminal is ignored, unless it is held inactive for longer than t_{BRK}. If this happens, then the start sequence will terminate, and the brake condition will be enabled as above.

If the motor speed drops below the low speed threshold (25% of the start speed set by SS), then the A4963 will indicate the loss of synchronization condition by pulling the FAULTn output active low.

If the RUN and RSC bits are set to 1 and the PWM signal applied to the PWM input terminal is not 0%, then the start sequencer will reset and retry, and the FAULTn output will remain low until the completion of six full commutation periods following the hold time. This cycle will continue until stopped by holding the PWM terminal inactive or by setting RUN to 0 or RSC to 0.

If RSC = 0, the FAULTn output will continue to indicate loss of synchronization until the PWM signal applied to the PWM input terminal is 0% or RUN is set to 0.

Indirect Open-Loop Speed (Voltage) Control

In some motor control systems, the central ECU is used to provide application-specific speed control. In these systems, the ECU may be remote from the motor driver. It is therefore desirable in these systems to use a low-frequency PWM signal between the ECU and the motor controller to minimize EMC issues with the control signal. This is particularly relevant to systems where a brush DC motor is being replaced by a BLDC motor. The A4963 includes an indirect open-loop control option that will accept a low-frequency PWM input and provide all the detailed motor commutation and control independently from the ECU.

When operating in the indirect mode, the A4963 measures the duty cycle of the low-frequency signal (5 Hz to 1 kHz) applied to the PWM terminal and applies the same duty cycle to the power bridge at a higher fixed-frequency, as shown in Figure 13. The frequency of the PWM signal applied to the power

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bridge is determined by the value of the PW[4:0] variable. The A4963 will also provide current limiting using the internal fixed off-time closed-loop current regulator synchronized with the bridge PWM control signal. The fixed off-time of the current control circuit will be the same as the programmed bridge PWM period defined by the value of PW[4:0]. This will ensure that the currrent control circuit does not cause excessive PWM switching and can only switch the bridge into the PWM-on state when 100% duty cycle is required and the motor torque is at the limit.

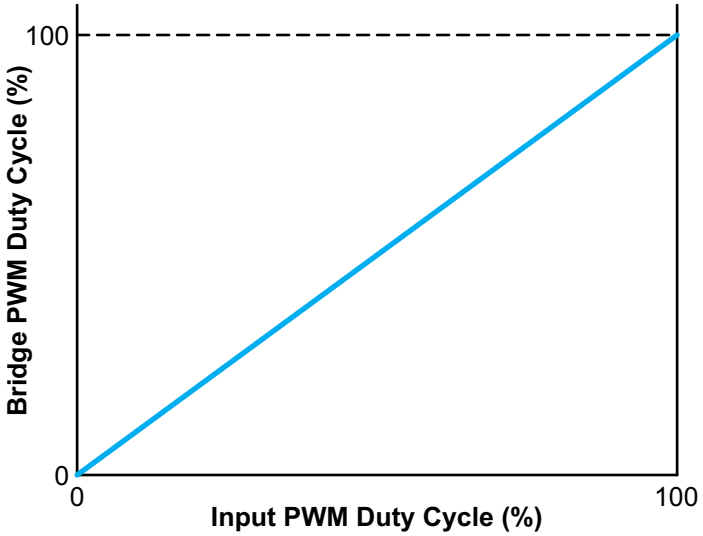

Figure 13: Bridge PWM vs. Input PWM

The A4963 does not limit the minimum or maximum duty cycle applied to the bridge. The PWM signal applied to the PWM terminal can have any value between 0 and 100%. At 100%, the motor will be running at full speed as determined by the load and the applied voltage. At very low duty cycles, there may not be sufficient current flowing in the motor to maintain sufficient speed for sensorless operation; however, the A4963 will not limit the minimum applied duty cycle to provide full flexibility for the speed control ECU to manage the motor operation. If the motor speed drops below the low speed threshold (25% of the start speed set by SS), then the A4963 will indicate the loss of synchronization condition by repeatedly pulling the FAULTn output active low for three PWM periods and inactive for three periods.

If a loss of synchronization occurs, the RUN and RSC bits are set to 1, and the PWM signal applied to the PWM input terminal is not 0%, then the FAULTn output will go active low for three PWM periods, inactive for three periods, then repeat this sequence before the start sequencer is reset and the start sequence initiated as shown in Figure 14. This cycle will continue until stopped by holding the PWM terminal inactive or setting either the RUN bit or the RSC bit to 0.

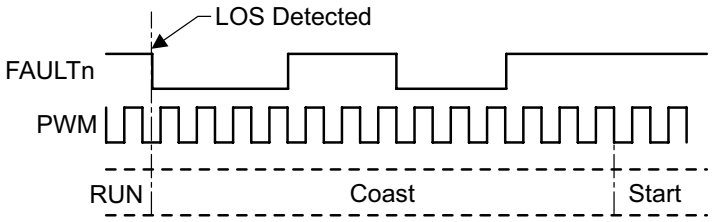

Figure 14: LOS Fault Reporting – Indirect Mode PWM

If a loss of synchronization occurs and RSC = 0, the FAULTn output will continue to indicate loss of synchronization until the PWM signal applied to the PWM input terminal is 0% or the RUN bit is set to 0. The A4963 is capable of measuring the duty cycle of any PWM signal from 5 Hz to 1 kHz. It can also accept slight variation in the PWM frequency from cycle to cycle. However, any variation will be translated to a duty cycle error. If the PWM signal remains in the inactive state for more than twice the length of time of the last measured period then the A4963 will put the bridge into the PWM-off state permanently and allow the motor current to decay. Holding the PWM signal inactive for a further PWM period, as shown in Figure 15, will force a brake condition if BRK = 1 and RUN = 1.

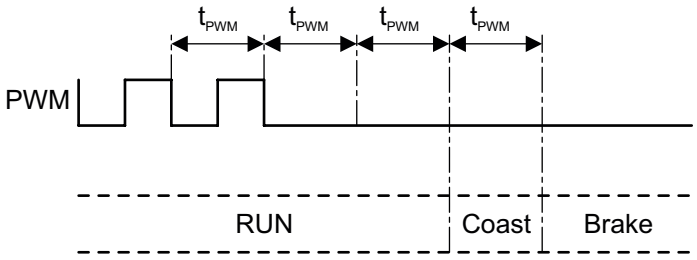

Figure 15: PWM Brake Timing – Indirect Mode PWM

Once enabled, the brake condition will be held until the PWM terminal is changed to its active state. If the motor operation is enabled, with RUN = 1 and BRK = 0, then the A4963 will initiate a start sequence. Once the start sequence is initiated, the duty cycle of the signal on the PWM terminal is monitored as above but not passed to the bridge drive circuits until the completion of six full commutation periods (one electrical cycle) following the hold time. During the start sequence, if the PWM signal is held inactive as described above, then the start sequence will be terminated and the brake condition will be forced.

Closed-Loop Torque (Current) Control

The A4963 provides a fixed off-time current limiting system that can operate with an applied PWM or in a standalone mode. By

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disabling all other control modes, this current limit can be used to provide closed-loop torque limited motor control.

At the start of the cycle, the bridge is enabled to force current from the supply through the load to ground. This is the PWM-on state. The current flows through a ground-referenced sense resistor which provides a voltage proportional to the current. This voltage is monitored using a differential sense amplifier, where the output is compared to a threshold voltage (V_{ILIM}) representing the peak current limit in the load. When the sensed current exceeds the limit, the bridge is switched to the PWM-off state. The PWM-off state is held for the duration of the fixed off-time defined by the value stored in PW[4:0]. This allows the current in the load to decay below the reference limit. At the end of the fixed off-time, the bridge is switched back to the PWM-on state to force the current to rise again. This sequence repeats and produces a ripple current, where the peak current is limited to a controlled level, and the amplitude of the ripple is determined by the motor parameters and the fixed off-time.

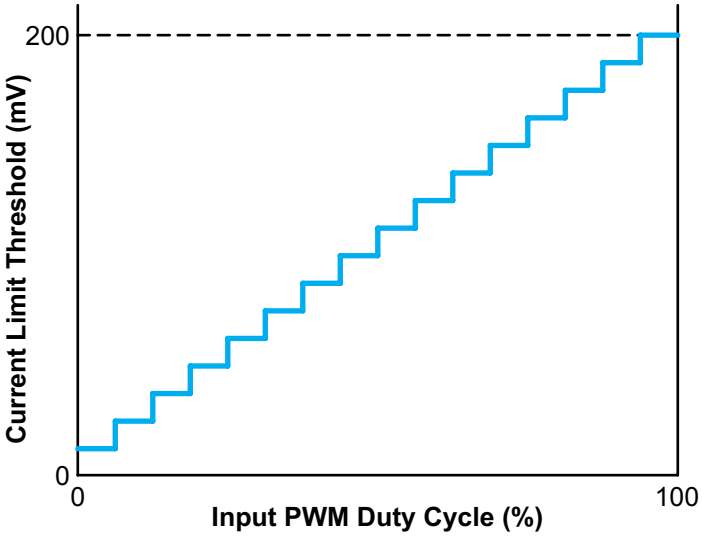

Figure 16: Current Demand vs. Input PWM

In the closed-loop torque control mode, the current limit threshold voltage is adjusted using a PWM signal or optionally via the serial interface. As in the indirect open-loop speed control mode, the PWM signal applied to the PWM terminal is monitored. In this case the duty cycle ratio of the applied PWM signal is translated to the current limit threshold voltage (V_{ILIM}) which is proportional to the PWM duty cycle. The duty cycle of the signal on the PWM input terminal is measured to 8-bit resolution, and the most significant 4 bits are used to set the value of V_{ILIM}. The relationship between the input duty cycle and V_{ILIM} is shown in Figure 16.

The applied PWM signal can have a frequency from 5 Hz to 1 kHz. It can also accept slight variation in the PWM frequency from cycle to cycle; however, any variation will be translated to a duty cycle error which will cause a disturbance in the current reference. If the PWM signal remains in the inactive state for more than twice the length of time of the last measured period, then the A4963 will put the bridge into the PWM-off state permanently and allow the motor current to decay. Holding the PWM signal inactive for a further PWM period will force a brake condition if BRK = 1 and RUN = 1.

Once enabled, the brake condition will be held until the PWM terminal is changed to its active state. If the motor operation is enabled, with RUN = 1 and BRK = 0, then the A4963 will initiate a start sequence.

After the start sequence is initiated, the duty cycle of the signal on the PWM terminal is monitored as above, but the resulting current reference level is ignored until the completion of six full commutation periods (one electrical cycle) following the hold time. During the start sequence, if the PWM signal is held inactive as described above, then the start sequence will be terminated and the brake condition will be forced.

If the motor speed drops below the low speed threshold (25% of the start speed set by SS), then the A4963 will indicate the loss of synchronization condition by repeatedly pulling the FAULTn output active low for three PWM periods and inactive for three periods.

If a loss of synchronization occurs, the RUN and RSC bits are set to 1, and the PWM signal applied to the PWM input terminal is not 0%, then the FAULTn output will go active low for three PWM periods, inactive for three periods, then repeat this sequence before the start sequencer is reset and the start sequence initiated as shown in Figure 14. This cycle will continue until stopped by holding the PWM terminal inactive or setting either the RUN bit or the RSC bit to 0.

If a loss of synchronization occurs, and RSC = 0, the FAULTn output will continue to indicate loss of synchronization until the PWM signal applied to the PWM input terminal is 0% or the RUN bit is set to 0.

Closed-Loop Speed Control

For systems where closed-loop speed control is required and no external controller is available, the A4963 includes a full PI (proportional/integral) speed control loop. The motor state and speed are determined by the duty cycle input to the PWM terminal or optionally via the serial interface. The speed demand

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reference to the PI control loop is determined by the duty cycle of the PWM input signal as a percentage of the maximum speed (f_{MAX}). This is set by the value in the SMX[2:0] variable as:

$$f_{MAX} = 0.1 \times (2^{(SMX + 8)} - 1)\ Hz$$

f_{MAX} for each value of SMX is listed in Table 2. This also shows the equivalent motor speed (in rpm) for several motor pole-pair options.

Table 2: Max Speed

SMX	f_{MAX} (Hz)	Motor Pole Pairs (Speed in rpm)				
		1	2	3	4	6
0	25.5	1530	765	510	383	255
1	51.1	3066	1533	1022	767	511
2	102.3	6138	3069	2046	1535	1023
3	204.7	12282	6141	4094	3071	2047
4	409.5	24570	12285	8190	6143	4095
5	819.1	49146	24573	16382	12287	8191
6	1638.3	98298	49149	32766	24575	16383
7	3276.7	196602	98301	65534	49151	32767

The closed-loop speed controller compares the speed demand, represented by the duty cycle of signal applied to the PWM input terminal, to the motor speed represented by the electrical cycle frequency. It then sets the duty cycle of the internal, higher-frequency bridge PWM signal to adjust the motor speed. The frequency of the PWM signal applied to the power bridge is determined by the value of the PW[4:0] variable. The A4963 will also provide current limiting using the internal fixed off-time closed-loop current regulator synchronized with the bridge PWM control signal. The fixed off-time of the current control circuit will be the same as the programmed bridge PWM period defined by the value of PW[4:0]. This will ensure that the current control circuit does not cause excessive PWM switching and can only switch the bridge into the PWM-on state when 100% duty cycle is required and the motor torque is at the limit.

The dynamic response of the speed controller can be tuned to the motor and load dynamics by independently setting the gains for the proportional and the integral paths in the closed-loop speed controller. The proportional gain is set by the contents of the SP[2:0] variable and the integral gain by the contents of the SI[2:0] variable.

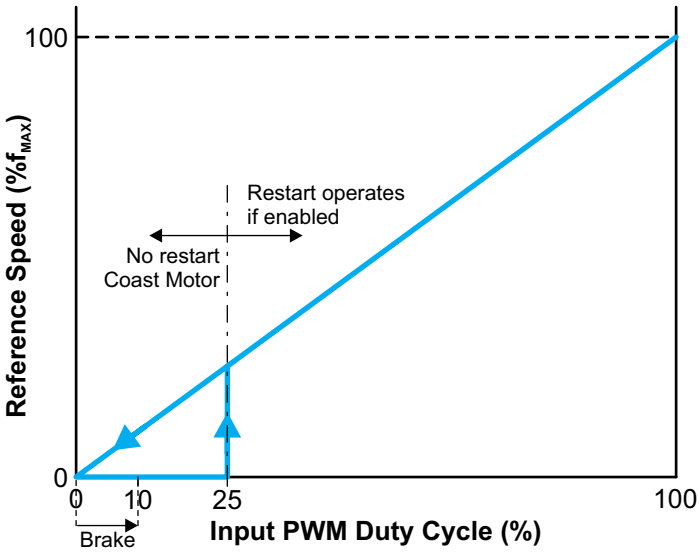

Figure 17: Speed vs. Input PWM

The PWM signal applied to the PWM terminal can have a frequency from 5 Hz to 1 kHz. It can also accept slight variation in the PWM frequency from cycle to cycle; however, any variation will be translated to a duty cycle error which will cause a disturbance in the speed reference.

If the PWM signal remains in the inactive state for more than twice the length of time of the last measured period, then the A4963 will put the bridge into the PWM-off state and allow the motor current to decay. Holding the PWM signal inactive for a further PWM period will force a brake condition if BRK = 1 and RUN = 1.

Once enabled, or following a power-on-reset, the brake condition will be held, if BRK = 1 and RUN = 1, until the duty cycle of the PWM signal is greater than 10%. When BRK = 0, braking is disabled regardless of the PWM input. The brake condition can only be applied when the PWM signal rises from 0% and remains under 10%. The brake condition is not applied if the motor has been running and the PWM signal remains greater than 0% even if it is less than 10%.

Following a brake condition, when the motor is not running, a duty cycle between 10% and 25% on the PWM signal disables the bridge drive and allows the motor to coast. When the duty cycle of the PWM signal exceeds 25%, the A4963 initiates a start sequence, and the motor is allowed to run.

After the start sequence is initiated, the duty cycle of the signal on the PWM terminal is monitored, but the resulting speed

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demand reference level is ignored until the completion of two commutation periods following the hold time. During the start sequence, if the PWM signal is held inactive as described above, then the start sequence will be terminated, and the brake condition will be forced.

Once sensorless operation is achieved, the motor speed will change to match the speed demand reference determined by the duty cycle of the input PWM signal. The speed then continues to match the demand without being affected by varying supply voltage or load, up to the torque limit imposed by either the peak current limiter or effective applied voltage limited by the motor bemf.

As the duty cycle of the PWM signal reduces, the motor speed will follow until the speed is either too low to maintain sensorless operation or the demand is less than the low speed threshold. The low speed threshold is 25% of the start speed set by SS. At this point, the A4963 will turn off all bridge MOSFETs allowing the motor to coast. The A4963 will then indicate a loss of synchronization condition by repeatedly pulling the FAULTn output active low for three PWM periods and inactive for three periods.

If a loss of synchronization occurs, the RUN and RSC bits are set to 1, and the PWM signal applied to the PWM input terminal is greater than 25%, then the FAULTn output will go active low for three PWM periods, inactive for three periods, then repeat this sequence before the start sequencer is reset and the start sequence initiated as shown in Figure 14. This cycle will continue until stopped by holding the PWM terminal inactive or setting either the RUN bit or the RSC bit to 0.

If a loss of synchronization occurs and RSC = 0, the FAULTn output will continue to indicate loss of synchronization until the PWM signal applied to the PWM input terminal is less than 25% or the RUN bit is set to 0.

Power Supplies

A single power supply voltage is required. This directly supplies the analog and output drive sections. An internal regulator provides a lower fixed logic supply. TTL threshold logic inputs allow the inputs to be driven from a 3.3 or 5 V logic interface.

The A4963 can operate over a wide supply voltage range. Electrical parameters are fully defined from 6 to 28 V; however, it will function correctly up to 50 V during load dump conditions and will achieve full operation down to 4.2 V during cold crank conditions. Below 6 V and above 28 V, some parameters may marginally exceed the limits specified for the normal supply voltage range. The A4963 will function correctly with a VBB supply down to 4.2 V; however, full sensorless startup may not be possible below 5 V, as the motor bemf may be too low to allow correct operation, and there may be insufficient torque to allow correct startup. In this case, assuming the control conditions allow motor start, the A4963 will continue to force the motor phases to commutate in a repeating start sequence.

The main power supply should be connected to VBB through a reverse voltage protection circuit and should be decoupled with ceramic capacitors connected close to the supply and ground terminals. The supply to the MOSFET bridge should include large electrolytic capacitors that are rated to provide the motor ripple current.

Gate Drive and Bridge PWM

The A4963 is designed to drive external, low on-resistance, power n-channel (low-side) and p-channel (high-side) MOSFETs. It supplies the large transient currents necessary to quickly charge and discharge the external FET gate capacitance to reduce dissipation in the FET during switching. The charge and discharge rate can be controlled using an external resistor in series with the connection to the gate of the FET.

Gate Drive Voltage Regulation

The gate drives are powered directly from the VBB supply, but each drive output incorporates an internal regulator which limits the voltage to the drive outputs and therefore the maximum gate-source voltage applied to the external MOSFETs.

Low-Side Gate Drive

The low-side, gate drive outputs on GLA, GLB, and GLC are referenced to the GND terminal. These outputs are designed to drive external N-channel power MOSFETs. External resistors between the gate drive output and the gate connection to the MOSFET (as close as possible to the MOSFET) can be used to control the slew rate seen at the gate, thereby providing some control of the di/dt and dv/dt of the voltage at the SA/SB/SC terminals.

GLx = ON means that the upper half of the driver is turned on, and it will source current to the gate of the low-side external MOSFET turning it on.

GLx = OFF means that the lower half of the driver is turned on, and it will sink current from the gate of the external MOSFET turning it off.

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High-Side Gate Drive

The high-side, gate drive outputs on GHA, GHB, and GHC are referenced to the VBB terminal. These outputs are designed to drive external P-channel power MOSFETs. External resistors between the gate drive output and the gate connection to the MOSFET (as close as possible to the MOSFET) can be used to control the slew rate seen at the gate, thereby controlling the di/dt and dv/dt of the voltage at the SA/SB/SC terminals.

GHx = ON (or "low") means that the lower half of the driver is turned on, and it will sink current from the gate of high-side external MOSFET turning it on.

GHx = OFF (or "high") means that the upper half of the driver is turned on, and it will source current to the gate of the high-side MOSFET turning it off.

The SA, SB, and SC terminals are connected directly to the motor phase connections. These terminals sense the voltages switched across the load. These inputs are referred to elsewhere as the Sx inputs where x is replaced by A, B, or C depending on the phase. These terminals also provide the phase voltage feedback used to determine the rotor position.

Dead Time

To prevent cross-conduction (shoot through) in any phase of the power MOSFET bridge, it is necessary to have a dead-time delay between a high- or low-side turn off and the next complementary turn-on event. The potential for cross-conduction occurs when any complimentary high-side and low-side pair of MOSFETs is switched at the same time, for example, at the PWM switch point. In the A4963, the dead time for all three phases is set by the contents of the DT[5:0] bits in configuration register 0. These six bits contain a positive integer that determines the dead time by division from the system clock.

The dead time is defined as:

$$t_{DEAD} = n \times 50\ ns$$

where n is a positive integer defined by DT[5:0] and t_{DEAD} has a minimum value of 100 ns.

For example, when DT[5:0] contains [01 1000] (= 24 in decimal), then t_{DEAD} = 1.2 µs, typically. The accuracy of t_{DEAD} is determined by the accuracy of the system clock as defined in the Electrical Characteristics table. A value of 0, 1, or 2 in DT[5:0] will set the minimum dead time of 100 ns.

Synchronous Rectification

The default operation of the bridge PWM mode is to use synchronous rectification, where the MOSFETs in the phase of the bridge to which PWM is applied are switched in anti-phase as described in the Dead Time section above. This provides slow decay of the phase current during the PWM off-time and helps to minimize the power dissipation by passing the recirculating load current through an active MOSFET channel rather than the higher resistance of the MOSFET body diode.

Non-Synchronous Rectification

In some cases, it may be desirable to switch off the synchronous rectification operation and allow diode conduction to reduce the number of switching events in each PWM period. The A4963 can be configured to use non-synchronous rectification where all MOSFETs are switched off during the PWM off-time. This produces fast decay of the phase current during the PWM off-time and can result in higher phase current ripple.

Recirculation Mode Selection to Improve bemf Detection

The bemf zero crossing detection can be affected by the recirculation path used during the PWM off-time. The bemf voltage that is generated in the undriven phase is measured at the phase connection but is referenced to the common point, or center tap, of the three motor phases, inside the motor. The bemf voltage will swing from negative to positive or from positive to negative with respect to the center tap voltage. The point of interest for the commutation controller is when this voltage crosses zero and changes polarity. Therefore, the center-tap voltage used is the reference input to the zero-crossing comparator.

Although the center-tap voltage is not usually available, the A4963 develops an approximation to this voltage using an internal resistor network connected to the motor phase terminals, SA, SB, and SC. During the PWM on-time, the phase voltage of one of the two active phases will be at the supply voltage (V_{BB}) and the other will be at ground. The resulting center-tap voltage will be approximately half of the supply voltage. During the PWM off-time, the phase voltage of the two active phases and the resulting center-tap voltage will be close to ground, if low-side recirculation is selected or close to V_{BB} if high-side recirculation is selected.

This means that if low-side recirculation is selected (RM[1:0] = 10) and the bemf voltage is negative, then the voltage at the undriven phase terminal, during the PWM off-time should be negative with respect to ground. However, the undriven phase is

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connected to an inactive low-side MOSFET and will be clamped to ground by the bode diode of that MOSFET. The resulting voltage will therefore only be below ground by the forward voltage of the body diode of the low-side MOSFET and will not start to rise until close to the zero crossing point as shown in Figure 18a. During the PWM off-time, the differential input voltage to the bemf comparator used for bemf zero crossing will be limited to the forward voltage of the MOSFET body diode, and the common mode of the input will be below ground until the bemf voltage is positive. This low differential voltage and negative common mode voltage will make the comparator more susceptible to noise and can result in false zero-crossing detection. Although the output of the comparator is digitally filtered, the additional noise can reduce the precision of the zero-crossing detection and the accuracy of the commutation controller.

A similar situation arises, as shown in Figure 18c, after zero-crossing detection, if low-side recirculation is used and the bemf voltage is falling.

A complementary situation also arises when high-side recirculation is used (RM[1:0] = 01) as shown in Figure 18b. In this case, the bemf voltage generated in the undriven phase will be clamped to the positive supply voltage by the body diode of the undriven high side MOSFET. The differential input voltage to the bemf comparator will be limited to the forward voltage of the body diode of the high-side MOSFET and the common mode of the differential input to the bemf comparator will be above the positive supply voltage.

To overcome this effect and reduce the number of false zero-crossing detections due to noise, the A4963 provides an additional automatic mixed recirculation mode (RM[1:0] = 00) as shown in Figure 18d. In this mode, the recirculation is switched between high-side and low-side depending on the expected bemf voltage. If the bemf voltage in the undriven phase is expected to be falling, then low-side recirculation is used for the start of the commutation period and high-side recirculation is used after the zero-crossing point. If the bemf voltage in the undriven phase is expected to be rising, then high-side recirculation is used for the start of the commutation period and low-side recirculation is used after the zero-crossing point. This ensures that the zero-crossing comparator is driven with the optimum conditions to minimize the effects of noise on the performance of the A4963.

If non-synchronous rectification is selected (RM[1:0]=11), then, during the PWM-off time, one phase voltage will be above VBB by the forward voltage of the body diode of the high-side MOSFET and the other will be below ground by the forward voltage of the body diode of the low-side MOSFET. During the PWM

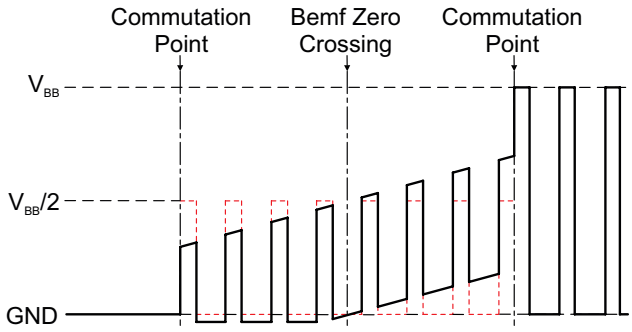

Figure 18a: Low-Side Recirculation, bemf Rising

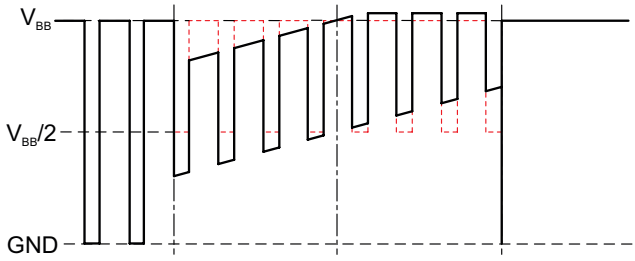

Figure 18b: High-Side Recirculation, bemf Rising

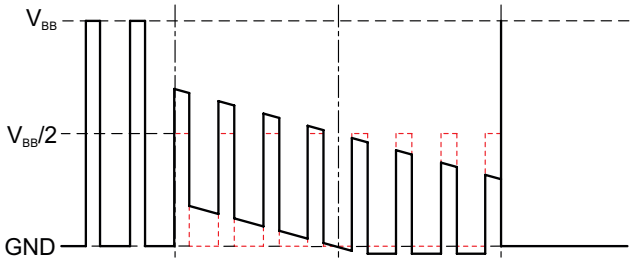

Figure 18c: Low-Side Recirculation, bemf Falling

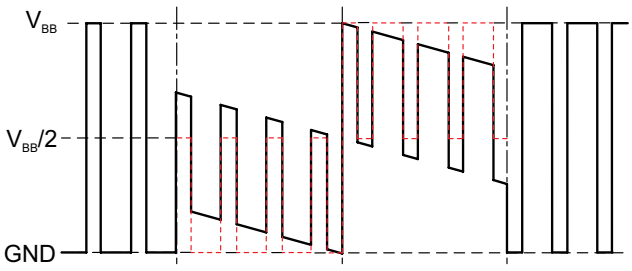

Figure 18d: Auto Mixed Recirculation, bemf Falling

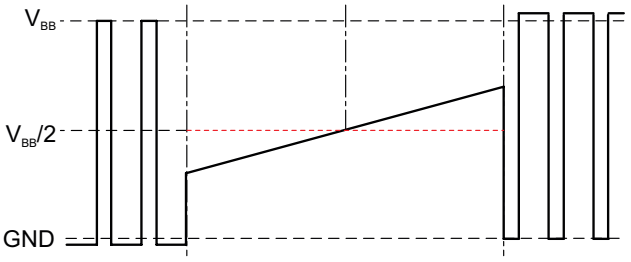

Figure 18e: Non-Synchronous Fast Decay

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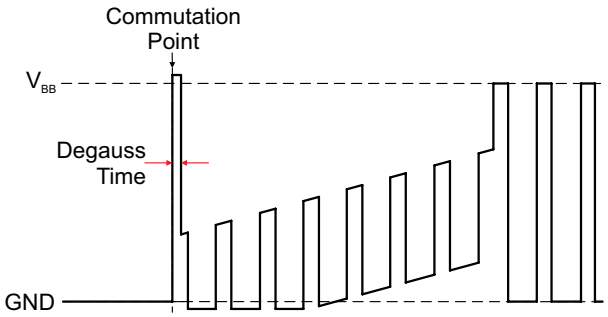

Figure 19a: Short Degauss Time

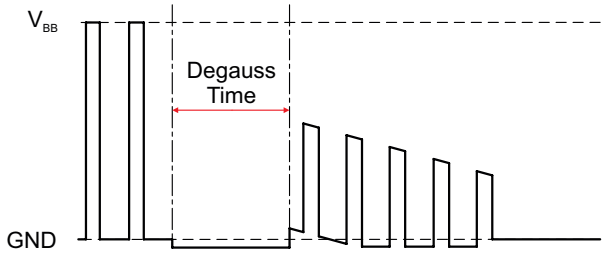

Figure 19b: Long Degauss Time

on-time, one phase will be close to ground and the other close to VBB. The resulting center-tap voltage will remain at half the supply voltage during both PWM on- and PWM off-times, and the comparator will perform as well as in the automatic mixed recirculation mode.

Degauss Compensation

At the end of a commutation period, the current in one phase winding will be reduced to zero. As the phase winding is an inductor, the current in the winding cannot be reduced to zero immediately but will reduce at a rate defined approximately by:

$$\frac{dI}{dt} = -\frac{V}{L}$$

where dI/dt is the rate of change of current, V is the voltage applied to reduce the current, and L is the inductance of the winding. Rearranging this gives the time required to reduce the current in the winding to zero as approximately:

$$t = \frac{L \times I}{V}$$

where I is the initial current in the winding and t is the time for that current to reach zero. This is commonly referred to as the degauss time or the de-energization time for the phase switching to zero current. This is the time that the voltage must be applied to the winding in order to redue the current to zero. The applied voltage is usually defined by the supply voltage plus the forward voltage of either the high-side or the low-side MOSFET depending on the current direction.

The degauss time will be seen as a period when the voltage on the undriven phase is clamped high or low as shown in Figure 19.

From the equation above, it is clear that the degauss time will increase as the current or winding inductance increases and as the applied voltage decreases. For most motors with normal dynamic response, the phase inductance is small, and the degauss time is correspondingly small, as shown in Figure 19a. In fact, the motor inductance is usually inversely proportional to the peak motor current.

There are, however, some low-noise motors with low dynamic performance requirements where the phase inductance is disproportionately high to ensure very low current ripple.

These motors will exhibit an extended degauss time as shown in Figure 19b.

An extended degauss time can adversely affect the digital filter that is applied to the zero-crossing comparator output and can cause the zero-crossing point to be detected in a false position. The commutation controller will continue to operate, but this effect will usually appear as a phase shift between the motor and the A4963 controller. To overcome this effect, if it presents a problem, the A4963 can provide automatic compensation for the degauss time by setting the degauss compensation bit, DGC, to 1.

Current Limit

An integrated fixed off-time PWM current control circuit is provided to limit the motor current during periods where the torque demand exceeds the normal operating range and to provide a variable current limit circuit in the closed-loop current control mode.

When using indirect voltage-mode control or closed-loop speed control, off-time of the current control circuit is set to be the same as the programmed bridge PWM period defined by the value of PW[4:0].

For direct voltage-mode control, the PWM frequency is determined by the applied PWM signal, and the fixed off-time is defined directly by the value of PW. In this case, the fixed off-time should be set to the same or longer than the period of the externally applied PWM signal.

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When the closed-loop current control mode is selected, then the fixed off-time alone will determine the PWM frequency when the A4963 is operating in current limit. The fixed off-time is defined directly by the value of PW.

The phase current is measured as a voltage (V_{SENSE}) across a sense resistor (R_{SENSE}) placed between the supply ground and the common connection to the sources of the low-side MOSFETs in the three-phase power bridge. A sense amplifier with high common-mode rejection and a fast response time is provided to convert the differential current sense voltage, directly across the sense resistor, to a ground-referenced voltage and remove any common-mode noise.

The output of the sense amplifier is compared to a current limit threshold voltage (V_{ILIM}) to indicate to the PWM control circuit when the bridge current is greater than the current limit threshold.

The current limit threshold is therefore defined by:

$$I_{LIM} = \frac{V_{ILIM}}{R_{SENSE}}$$

where V_{ILIM} is the current limit threshold voltage and R_{SENSE} is the value of the sense resistor.

The value of V_{ILIM} can be set in two ways, depending on the motor control method selected.

When the closed-loop current control mode is selected, V_{ILIM} is determined by the duty cycle of the signal on the PWM input terminal. The duty cycle ratio of the PWM signal is used to set the required value of V_{ILIM} as a ratio of the maximum value of V_{ILIM}, typically 200 mV. For example, when the duty cycle ratio of the signal on the PWM input terminal is 40%, then V_{ILIM} will be 80 mV.

In all other motor control modes, the value of V_{ILIM} is determined by the contents of the VIL[3:0] variable. This allows control of the maximum current limit via the serial interface.

When programmed through the serial interface, V_{ILIM} can have a value between 12.5 mV and 200 mV defined as:

$$V_{ILIM} = (n + 1) \times 12.5\ mV$$

For example, when VIL[3:0] contains [1011] (= 11 in decimal), then V_{ILIM} =150 mV.

In closed-loop current-control mode, the duty cycle of the signal on the PWM input terminal is measured to 8-bit resolution, and the most significant 4 bits are used in place of VIL to set the value of V_{ILIM}.

At the start of a PWM cycle, the MOSFETs in the bridge are turned on, such that current increases in a motor winding and in the sense resistor until the voltage across the sense resistor (V_{SENSE}) reaches the current limit threshold voltage (V_{ILIM}).

When V_{SENSE} rises above V_{ILIM}, the bridge switches from a drive configuration, where the current is forced to increase, into a recirculation configuration, where the motor inductance causes the current to recirculate for a fixed duration, defined as the off-time. The recirculation configuration mode is determined by the value in the RM[1:0] variable.

When RM[1:0] = 01, the recirculation will always be high-side with slow decay. When RM = 10, the recirculation will always be low-side with slow decay. When RM = 00, the default value, then the current decay will be slow, but the recirculation path will be determined by the A4963 commutation controller depending on the expected direction of the back emf voltage in the undriven phase. When RM = 11, no synchronous rectification takes place, and fast current decay will take place.

Fixed Off-Time

In the direct duty-cycle control mode and the closed-loop current control mode, the length of the fixed off-time is set by the user-programmed contents of the PW[4:0] bits in configuration register 2. The five bits of PW contain a positive integer that determines the off-time derived by division from the system clock.

The off-time is defined as:

$$t_{PW} = 20\ \mu s + (n \times 1.6\ \mu s)$$

where n is a positive integer defined by PW[4:0].

For example, when PW[4:0] contains [1 0011] (= 19 in decimal), then t_{PW} = 50.4 µs, typically.

The accuracy of t_{PW} is determined by the accuracy of the system clock as defined in the Electrical Characteristics table. A value of 0 in PW will set the minimum off time of 20 µs.

Fixed Frequency

In the indirect duty-cycle control mode and the closed-loop speed control mode, t_{PW} is used as the fixed PWM period to set the fixed frequency of the bridge PWM signal. In these modes, the fixed off-time used for current limiting is automatically set to be the same as the resulting PWM period.

For example, when PW[4:0] contains [1 0110] (= 22 in decimal), then t_{PW} = 55.2 µs and the PWM frequency is 18.1 kHz.

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Blank Time

When the bridge is switched into the drive configuration, a current spike occurs due to the reverse-recovery currents of the clamp diodes and switching transients related to distributed capacitance in the load. To prevent this current spike from being detected as a current limit trip, the current-control comparator output is blanked for a short period of time when the source driver is turned on. The length of the blanking time is set by the contents of the BT[3:0] bits in configuration register 0. These four bits contain a positive integer that determines the blank time derived by division from the system clock.

The blank time is defined as:

$$t_{BL} = n \times 400\ ns$$

where n is a positive integer defined by BT[3:0].

For example, when BT[3:0] contains [1011] (= 11 in decimal), then t_{BL} = 4.4 µs, typically.

The blank time is also used with the MOSFET drain-source monitors, which are used to determine MOSFET short faults. The blank time is used in these circuits, as shown in Figures 5 through 7, to mask the effect of any voltage or current transients caused by any PWM switching action.

The user must ensure that blank time is long enough to mask any current transient seen by the internal sense amplifier and mask any voltage transients seen by the drain-source monitors.

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DIAGNOSTICS

Several diagnostic features are integrated into the A4963 to provide indication of fault conditions. In addition to system wide faults such as undervoltage and overtemperature, the A4963 integrates individual drain-source monitors for each external MOSFET, to provide short-circuit detection. The fault status is available from two sources, the FAULTn output terminal and the serial interface.

FAULTn Output

The FAULTn terminal is an active-low open-drain output, which is high impedance when no faults are present, and either pulls low or pulses low when faults are detected. The status of the FAULTn output during a fault condition or once a fault has been detected is shown in Table 3 and Figures 20 to 22.

In the direct duty-cycle mode, the FAULTn output will be low when a fault is present or when a fault has been latched.

In all three indirect control modes, the action of the FAULTn output depends on the specific fault condition and the status of the Enable Stop On Fault bit (ESF) in the run register. The FAULTn output will only remain low when a fault is present that stops the motor from being able to run. For transient fault conditions, including loss of synchronization and short faults, the FAULTn output produces a low pulse, which is low for a duration determined by the period of the controlling PWM input signal and the specific fault. This allows the FAULTn terminal to be connected directly to the PWM terminal to provide a single wire control with fault feedback.

There are three pulse durations indicating three different fault groups. In each case, the FAULTn output will go active-low as soon as the fault is detected and remain low for the remainder of the period of the PWM signal applied to the PWM input terminal. It will then remain active for a further two, three, or four periods depending on the fault condition. In Table 3 and Figures 20 to 22, these are referred to as Pulse2, Pulse3, and Pulse4 respectively. The FAULTn output will then return to the inactive (high impedance) state. Some fault conditions require that the fault signal is repeated for the duration of the fault condition or latched fault state. This is indicated by an R at the end of the pulse description: Pulse2R, Pulse3R, or Pulse4R. In these cases, following the active state, the FAULTn output returns to the inactive state for the same number of PWM periods before repeating the sequence.

This pulse mode of fault reporting allows the signal applied to the combined PWM and FAULTn connection to continue controlling the action of the A4963 in the presence of a fault condition or latched fault state. In some cases, this will allow the motor to continue running under control. It also allows a latched fault state to be reset by the control PWM signal.

Serial Diagnostic Output

The serial interface allows detailed diagnostic information to be read from the diagnostic register at any time.

The first bit (bit 15) of the diagnostic register contains a common fault flag (FF), which will be high if any of the fault bits in the registers have been set. This allows fault condition to be detected using the serial interface by simply taking STRn low. As soon as STRn goes low, the first bit in the diagnostic register can be read to determine if a fault has been detected at any time since the last diagnostic register reset. In all cases, the fault bits in the diagnostic registers are latched and only cleared after a diagnostic register reset.

Note that FF (bit 15) does not provide the same function as the fault output on the FAULTn terminal. The fault output on the FAULTn terminal provides an indication that either a fault is present or the outputs have been disabled due to a short fault. FF provides an indication that a fault has occurred since the last fault reset and the respective fault flag has been latched. The diagnostic register is described further in the serial interface section description below.

Fault Action

The action taken when a short fault or over temperature condition is detected is determined by the state of the Enable Stop On Fault (ESF) in the run register as defined in Table 3. When ESF = 1, any short fault condition, loss of synchronization, or overtemperature condition will disable all the gate drive outputs and coast the motor. For short faults, this disabled state will be latched until the PWM input is at 0%, a serial read is completed, or a power-on-reset occurs. For undervoltage fault conditions, the outputs will always be disabled until the condition is removed.

When ESF = 0, any short fault condition or overtemperature condition will be indicated by the FAULTn output, but the A4963 will not disrupt continued operation and will therefore not protect the motor or the drive circuit from damage. When a fault occurs, it is imperative that the master control circuit or an external circuit takes any necessary action to prevent damage to components.

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Table 3: Fault Response Actions

Fault Description	Disable Outputs		FAULTn Output			Latched	Reset
			Direct	Indirect			
	ESF = 0	ESF = 1		ESF = 0	ESF = 1		
No Fault	No	No	Z	Z	Z	N/A	N/A
Serial Transmission Error	No	No	Z	Z	Z	No	Condition Removed
VBB Power-On Reset	Yes [1]	Yes [1]	Low	Low	Low	No	Condition Removed
VBB Undervoltage	Yes [1]	Yes [1]	Low	Low	Low	No	Condition Removed
Temperature Warning	No	No	Low	Z	Pulse4 [2]	No	Condition Removed
Overtemperature	No	Yes [1]	Low	Pulse4R [2]	Low	No	Condition Removed
Lost Synchronization	Yes [1]	Yes [1]	Low	Pulse3R [2]	Pulse3R [2]	If RSC = 0	Stop or Restart
Short to Ground	Yes [3]	Yes [1]	Low	Pulse2 [2]	Pulse2R [2]	Only when ESF = 1	Stop or SPI
Short to Supply	Yes [3]	Yes [1]	Low	Pulse2 [2]	Pulse2R [2]		Stop or SPI

[1] All gate drives low, all MOSFETs off.
[2] For pulse sequence, see Figure 20 to Figure 22.
[3] Gate drive to the affected MOSFET low, only the affected MOSFET off.
Z = Open Drain High Impedance

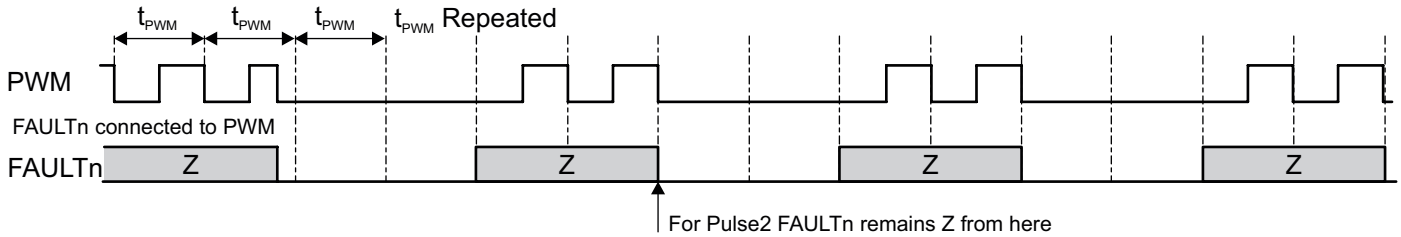

Figure 20: Indirect Mode PWM – MOSFET Short Fault Output Timing (Pulse2R) (IPI = 0)

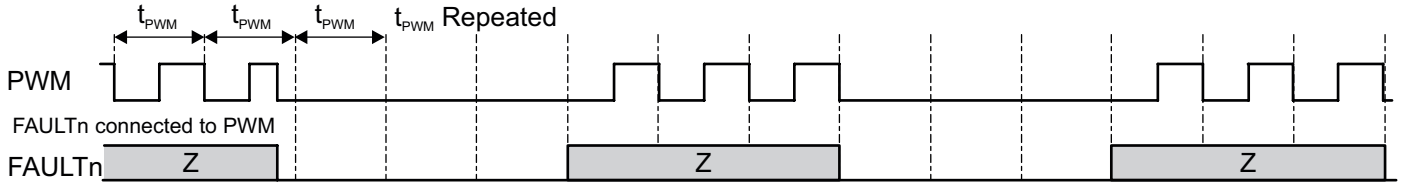

Figure 21: Indirect Mode PWM – Loss of Synchronization Fault Output Timing (Pulse3R) (IPI = 0)

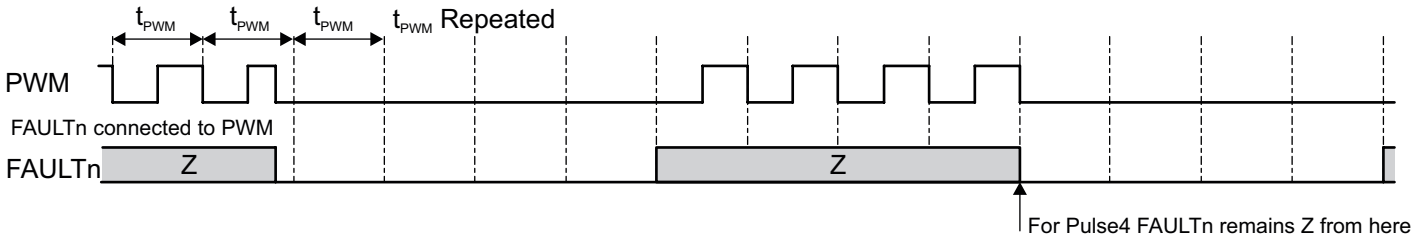

Figure 22: Indirect Mode PWM – Overtemperature Fault Output Timing (Pulse4R) (IPI = 0)

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Fault Masks

Individual diagnostics, except VDD undervoltage and serial transmission error, can be disabled by setting the corresponding bit in the mask register. VDD undervoltage detection cannot be disabled, because the diagnostics and the output control depend on VDD to operate correctly. If a bit is set to one in the mask register, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated, and no fault flags or diagnostic bits will be set. See the mask register definition for bit allocation.

Care must be taken when diagnostics are disabled to avoid potentially damaging conditions.

Chip-Level Diagnostics

Parameters critical for safe operation of the A4963 and the external MOSFETs are monitored. These include serial interface, maximum chip temperature, minimum internal logic supply voltage (V_{DD}), and the minimum motor supply voltage (V_{BB}). Faults are indicated by an active-low level or pulse on the FAULTn output terminal. Faults are latched in the diagnostic register when they occur, and the diagnostic register is only reset by a complete read of the diagnostic register or a power-on-reset. (see section below on diagnostic register serial access)

Chip Fault State: Overtemperature

Two temperature thresholds are provided: a hot warning and an overtemperature shutdown.

- If the chip temperature rises above the temperature warning threshold, T_{JW}, the thermal warning bit (TW) will be set in the diagnostic register. The state of the FAULTn output during a thermal warning fault condition will depend on the control mode and the state of the ESF bit. If direct control is in use, then FAULTn will be active. If one of the indirect control modes is in use and ESF = 1, then FAULTn will be repeatedly active-low for four PWM periods and inactive for four periods. If one of the indirect control modes is in use and ESF = 0, then FAULTn will remain inactive and the fault condition will not be detected. In all cases, no action will be taken by the A4963 when a thermal warning fault condition is present. When the temperature drops below T_{JW} by more than the hysteresis value (T_{JWHys}), the fault condition and any active-low level on FAULTn is either removed immediately, if in a permanent low state, or terminated at the end of the pulse. The thermal warning bit (TW) remains latched in the diagnostic register until reset.
- If the chip temperature rises above the overtemperature threshold (T_{JF}), the overtemperature bit (OT) will be set in the diagnostic register. The state of the FAULTn output during an overtemperature fault condition will depend on the control mode and the state of the ESF bit. If direct control is in use or if ESF = 1, then FAULTn will be permanently active until the fault condition is removed and all gate drive outputs will be off. If one of the indirect control modes is in use and ESF = 0, then FAULTn will be repeatedly active-low for four PWM periods and inactive for four periods. In all control modes, if ESF = 0, then no circuitry will be disabled during an overtemperature fault condition, and action must be taken by the user to limit the power dissipation to prevent overtemperature damage to the chip and unpredictable device operation. When the temperature drops below T_{JF} by more than the hysteresis value (T_{JFHys}), the fault condition and any active-low level on FAULTn is either removed immediately, if in a permanent low state, or terminated at the end of the pulse. The overtemperature bit (OT) remains latched in the diagnostic register until reset.

Chip Fault State: VBB Undervoltage

The main power supply to the A4963 (V_{BB}) is applied to the VBB terminal. This supply is used to provide the gate drive output voltage. It is critical to ensure that V_{BB} is sufficiently high before enabling any of the outputs, so VBB is monitored by an undervoltage detection circuit.

There are two undervoltage thresholds: V_{BBON} and V_{BBOFF} . After power is applied to the VBB terminal, and following a VBB undervoltage vault condition, V_{BB} must exceed V_{BBON} before the gate drive outputs can be enabled. When the supply voltage falls, the gate drive outputs can remain enabled until V_{BB} drops below V_{BBOFF} , at which point a VBB undervoltage fault condition will then exist. FAULTn will go active-low, and the VS bit in the diagnostic register will be set.

FAULTn is always active-low when a VBB undervoltage fault condition is present. The FAULTn output will remain active until the condition is removed. The motor cannot be run during an undervoltage condition, so the signal on the PWM input terminal will be ignored.

When the VBB undervoltage fault condition is removed, the gate drive outputs can be re-enabled, and the FAULTn output goes high impedance. The VS fault bit remains in the diagnostic register until reset.

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The VBB undervoltage monitor can be disabled by setting the VS bit in the mask register. Although not recommended, this can allow the A4963 to operate below its minimum specified supply voltage level with a severely impaired gate drive. The specified electrical parameters will not be valid in this condition.

Chip Fault State: Power-On Reset

The supply to the logic sections of the A4963 is generated by an internal regulator from V_{BB} and is monitored to ensure correct logical operation. The internal logic is guaranteed to operate with the voltage at the VBB terminal (V_{BB}) down to V_{BBR}. When V_{BB} drops below the V_{BBR}, then the logical function of the A4963 cannot be guaranteed, the outputs will be immediately disabled, and all the logic reset. The A4963 will enter a power-down state, and all internal activity, other than the logic supply voltage monitor, will be suspended. When the V_{BB} rises above the rising undervoltage threshold (V_{BBR}+V_{BBRHys}), the A4963 will exit the power-down state. All serial control registers will be reset to their power-on state, and all fault states and the general fault flag will be reset. The FF bit and the POR bit in the diagnostic register will be set to 1 to indicate that a power-on-reset has taken place. The same power-on-reset sequence occurs for initial power-on or for a VBB "brown-out", where V_{BB} only drops below V_{BBR} momentarily.

Chip Fault State: Serial Transmission Error

The data transfer into the A4963 through the serial interface is monitored. If there are more than 16 rising edges on SCK, or if STRn goes high and there are fewer than 16 rising edges on SCK, the write will be cancelled without writing data to the registers. In addition, the diagnostic register will not be reset, and the FF and SE bits will be set to indicate a data transfer error.

Loss of Synchronization

The motor operation is controlled by a closed-loop position estimator system, so it does not have any direct, immediate means of determining whether the motor is synchronized to the rotating field generated by the A4963. A loss of synchronization can only be detected if the commutation controller attempts to drive the motor too fast or too slow.

The low speed threshold is defined as 25% of the start speed set by the value of the SS[3:0] variable. For example, if the start speed is set to 32 Hz by setting SS to 15, then the low speed threshold will be set to 8 Hz.

The high speed (overspeed) threshold is determined by the product of the maximum limit ratio and the maximum speed. The maximum limit ratio is set by the value of the SH[1:0] variable, and the maximum speed is by set the value of the SMX[2:0] variable. For example, if the maximum speed is set to 1638.3 Hz by setting SMX to 6, and the limit ratio is set to 150% by setting SH to 4, then the overspeed threshold will be 2457.45 Hz.

If the commutation controller attempts to drive the motor at less than the low speed threshold or greater than the overspeed threshold, then the A4963 will indicate loss of synchronization.

In the extreme case, when a motor stalls due to excessive load on the output, there will be no bemf zero-crossing detection, and the frequency of the commutation sequence will be reduced at each expected commutation point to try and regain synchronization. The resulting speed will eventually reduce below the low speed threshold after a number of commutation cycles, and the A4963 will indicate loss of synchronization.

In some cases, rather than a complete stall, it is also possible for the motor to vibrate at a whole fraction (subharmonic) of the commutation frequency produced by the controller. In this case, the controller will still detect the bemf zero crossing, but at a rate much higher than the motor is capable of running. The commutation controller will increase the commutation rate to compensate, the resulting speed will increase above the overspeed threshold, and the A4963 will indicate loss of synchronization.

In the direct control mode, loss of synchronization is indicated by an active-low state on the FAULTn output. When using one of the indirect modes, loss of synchronization is indicated by repeatedly pulling the FAULTn output active-low for three PWM periods and inactive for three periods. In both cases, the LOS bit will be set in the diagnostic register. When loss of synchronization is detected, the controller will either stop or attempt to restart the motor depending on the state of the RUN bit, the restart control bit (RSC) in the run register, and the input demand. If the RUN and RSC bits are set to 1, and the input demand is greater than the minimum limit for the mode (see mode descriptions for detail), then the start sequencer will reset and retry, and the FAULTn output will remain low or continue the fault pulse sequence until the completion of six full commutation periods following the hold time. This cycle will continue until stopped by taking the input demand lower than the minimum limit for the mode or setting either the RUN bit or the RSC bit to 0.

If RSC = 0, the FAULTn output will continue to indicate loss of synchronization until the input demand is lower than the minimum limit for the mode or the RUN bit is set to 0.

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MOSFET Fault Detection

Faults on any external MOSFETs are determined by measuring the drain-source voltage of the MOSFET and comparing it to the drain-source overvoltage threshold (V_{DST}) defined by the VT[4:0] bits in configuration register 1. These bits provide the input to a 5-bit DAC with a least significant bit value of typically 50 mV. The output of the DAC produces V_{DST} approximately defined as:

$$V_{DST} = n \times 50\ mV$$

where n is a positive integer defined by VT[4:0].

The drain-source voltage for any low-side MOSFET is measured between the GND terminal and the appropriate Sx terminal. Any low-side current sense voltage should be taken into account when setting the V_{DST} level. The drain-source voltage for any high-side MOSFET is measured between the VBB terminal and the appropriate Sx terminal. Any voltage drop between the bridge supply to the common drain connection of the MOSFETs and the VBB terminal must be taken into account when setting the V_{DST} level.

Fault Qualification

The output from each VDS overvoltage comparator is filtered by a VDS fault qualifier circuit. This circuit uses a timer to verify that the output from the comparator is indicating a valid VDS fault. The duration of the VDS fault qualifying timer is the same as the blank time (t_{BLANK}) used by the current limit circuit, and determined by the contents of the BT[3:0] variable. t_{BLANK} is approximately defined as:

$$t_{BLANK} = n \times 400\ ns$$

where n is a positive integer defined by BT[3:0].

The qualifier can operate in one of two ways: debounce mode or blanking mode, selected by the VDQ bit.

In the default debounce mode, a timer is started each time the comparator output indicates a VDS fault detection when the corresponding MOSFET is active. This timer is reset when the comparator changes back to indicate normal operation. If the debounce timer reaches the end of the timeout period set by t_{BLANK}, then the VDS fault is considered valid and the corresponding VDS fault bit (AH, AL, BH, BL, CH, or CL) will be set in the diagnostic register and action taken to protect the MOSFET.

In the optional blanking mode, a timer is started when a gate drive is turned on. The output from the VDS overvoltage comparator for the MOSFET being switched on is ignored (blanked) for the duration of the timeout period, set by t_{BLANK}. If the comparator output indicates an overvoltage event when the MOSFET is in the on-state, and the blanking timer is not active, then the VDS fault is considered valid, and the corresponding VDS fault bit (AH, AL, BH, BL, CH, or CL) will be set in the diagnostic register and action taken to protect the MOSFET.

If a valid VDS fault is detected when ESF = 1, then this fault condition will be latched, and all MOSFETs will be immediately switched off and disabled until the fault is reset.

If a valid VDS fault is detected when ESF = 0, then the external MOSFET where the fault is detected is immediately switched off by the A4963, but the remaining MOSFETs continue to operate. The MOSFET where the fault is detected will be switched on again the next time the internal bridge control switches it from off to on.

To limit any damage to the external MOSFETs, when ESF = 0, the A4963 should either be fully disabled by setting the PWM input to 0% or by setting RUN to 0 through a serial write. Alternatively, setting the ESF bit to 1 will allow the A4963 to completely disable the MOSFETs as soon as a fault is detected.

The FAULTn output reports a VDS fault in different ways depending on the state of the ESF bit and the selected control mode.

When using the direct control mode, the FAULTn output will be active-low for the duration of the fault detection. In addition, when ESF = 1, FAULTn output will be active-low during the time when a VDS fault condition is latched.

When using any of the three indirect control modes with ESF = 0, the FAULTn output will be active-low for two PWM periods each time a VDS fault is detected. When using indirect control with ESF = 1, the FAULTn output will be repeatedly active-low for two PWM periods and inactive for two periods during the time when a VDS fault condition is latched.

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SERIAL INTERFACE

Serial Registers Definition

Table 4: Serial Registers Definition*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 0 (Blank, Dead)	0	0	0	WR	RM1	RM0	BT3	BT2	BT1	BT0	DT5	DT4	DT3	DT2	DT1	DT0
					0	0	1	0	0	0	0	1	0	1	0	0
Config 1 (V_{REF}, V_{DST})	0	0	1	WR	PFD	IPI	VIL3	VIL2	VIL1	VIL0	VDQ	VT4	VT3	VT2	VT1	VT0
					0	0	1	1	1	1	0	1	1	1	1	1
Config 2 (PWM)	0	1	0	WR	CP3	CP2	CP1	CP0	SH1	SH0	DGC	PW4	PW3	PW2	PW1	PW0
					0	1	1	1	1	0	0	1	0	0	1	1
Config 3 (Hold)	0	1	1	WR	CI3	CI2	CI1	CI0	HD3	HD2	HD1	HD0	HT3	HT2	HT1	HT0
					0	1	1	1	0	1	0	1	0	0	1	0
Config 4 (Start)	1	0	0	WR	SP3	SP2	SP1	SP0	SD3	SD2	SD1	SD0	SS3	SS2	SS1	SS0
					0	1	11	1	0	1	1	1	0	0	1	1
Config 5	1	0	1	WR	SI3	SI2	SI1	SI0	SPO	SMX2	SMX1	SMX0	PA3	PA2	PA1	PA0
					0	1	1	1	0	1	1	1	1	0	0	0
Mask	1	1	0	WR	TW	OT	LOS		VS		AH	AL	BH	BL	CH	CL
					0	0	0	0	0	0	0	0	0	0	0	0
Run	1	1	1	WR	CM1	CM0	ESF	DI4	DI3	DI2	DI1	DI0	RSC	BRK	DIR	RUN
					0	0	0	0	0	0	0	0	1	0	0	1
Diagnostic	FF	POR	SE		TW	OT	LOS		VS		AH	AL	BH	BL	CH	CL
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

*Power-on-reset value shown below each input register bit.

A three-wire synchronous serial interface, compatible with SPI, is used to control the features of the A4963. A fourth wire can be used to provide diagnostic feedback and readback of the register contents.

The A4963 can be fully controlled by the PWM input or via the serial interface. The serial interface provides access to additional control options and several programmable parameters. Application-specific settings are configured by setting the appropriate register bits through the serial interface.

The serial interface timing requirements are specified in the Electrical Characteristics table and illustrated in the Serial Interface Timing figure on page 9. Data is received on the SDI terminal and clocked through a shift register on the rising edge of the clock signal input on the SCK terminal. STRn is normally held high and is only brought low to initiate a serial transfer. No data is clocked through the shift register when STRn is high, allowing multiple slave units to use common SDI, SCK, and SDO connections. Each slave then requires an independent STRn connection.

When 16 data bits have been clocked into the shift register, STRn must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data and the diagnostic register is reset.

If there are more than 16 rising edges on SCK, or if STRn goes high and there are fewer than 16 rising edges on SCK, the write will be cancelled without writing data to the registers. In addition, the diagnostic register will not be reset, and the FF and SE bits will be set to indicate a data transfer error.

Diagnostic information or the contents of the configuration and control registers is output on the SDO terminal, msb first, while STRn is low and changes to the next bit on each falling edge of SCK. The first bit, which is always the FF bit from the diagnostic register, is output as soon as STRn goes low.

Each of the four configuration and control registers has a write bit (WR, bit 12) as the first bit after the register address. This bit must be set to one to write the subsequent bits into the selected register. If WR is zero, then the remaining data bits (bits 11 to 0) are ignored. The state of the WR bit also determines the data output on SDO. If WR is set to one, then the diagnostic register is output. If WR is set to zero, then the contents of the register selected by the first three bits are output. In all cases, the first three bits output on SDO will always be the FF bit, the POR bit, and the SE bit from the diagnostic register.

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Configuration and Control Registers

The serial data word is 16 bits, input msb first; the first three bits are defined as the register address. This provides eight writeable registers:

- Six registers are used for configuration, including blank time and dead time programming, current and voltage limits, PWM setup parameters, and motor startup and control parameters.
- The seventh register is the fault mask register providing the ability to disable individual diagnostics.
- The eighth register is the run register containing motor control inputs.

Writing to any register when the WR bit is set to one will allow the diagnostic register to be read at the SDO output.

Configuration Register 0 contains basic timing settings:

- RM[1:0], 2 bits to select the recirculation mode.
- BT[3:0], a 4-bit integer to set the blank time, t_{BL}, in 400 ns increments.
- DT[5:0], a 6-bit integer to set the dead time, t_{DEAD}, in 50 ns increments.

Configuration Register 1 contains basic voltage settings:

- PFD, 1 bit to select amount of fast decay at start.
- IPI, 1 bit to invert the sense of the PWM input.
- VIL[3:0], a 4-bit integer to set the current limit reference voltage, V_{ILIM}.
- VDQ, to select timing qualifier for the VDS monitor.
- VT[4:0], a 5-bit integer to set the drain-source threshold voltage, V_{DST}, in 50 mV increments.

Configuration Register 2:

- CP[3:0], 4 bits to set the position controller proportional gain.
- SH[1:0], 2 bits to select the overspeed limit ratio.
- DGC, 1 bit to enable degauss compensation.
- PW[4:0], a 5-bit integer to set the off time for PWM current control used to limit the motor current during startup and normal running, or to set the PWM period for the fixed frequency control options.

Configuration Register 3:

- CI[3:0], 4 bits to set the position controller integral gain.
- HD[3:0], a 4-bit integer to set the PWM duty cycle to produce the hold torque for the initial start position in increments of 6.25%.
- HT[3:0], a 4-bit integer to set the hold time of the initial start position in increments of 8 ms from 0 ms.

Configuration Register 4:

- SP[3:0], 4 bits to set the speed controller proportional gain.
- SD[3:0], a 4-bit integer to set the PWM duty cycle during forced commutation at startup in increments of 6.25%.
- SS[3:0], a 4-bit integer to set the start speed as electrical cycle frequency in increments of 2 Hz from 2 Hz.

Configuration Register 5:

- SI[3:0], 4 bits to set the speed controller integral gain.
- SPO, to select the signal output on the SPD terminal.
- SMX[2:0], a 3-bit integer to set the maximum (100% input) controlled speed as electrical cycle frequency.
- PA[3:0], a 4-bit integer to set the phase advance in increments of 1.875° (electrical)

The Mask Register contains a fault mask bit for each fault bit in the diagnostic register. If a bit is set to one in the mask register, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated, and no fault flags or diagnostic bits will be set.

The Run Register contains various bits to set running conditions:

- CM[1:0], to select the required control mode.
- ESF, the Enable Stop On Fault bit that defines the action taken when a short is detected. See diagnostics section for details of fault actions.
- DI[4:0], a 5-bit integer to allow control of the motor via the serial interface.
- RSC, the restart control bit. When set to 1, allows restart after loss of bemf synchronization of RUN is 1 and BRK is 0. When set to 0, the motor will coast to a stop when bemf synchronization is lost.
- BRK, enable brake function.
- DIR, direction control.
- RUN, enables the A4963 to start and run the motor.

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Diagnostic Register

There is one diagnostic register in addition to the eight writeable registers. Each time a register is written, the diagnostic register can be read, msb first, on the serial output terminal (SDO), as illustrated in the serial timing diagram. The diagnostic register contains fault flags for each fault condition, a general fault flag, and an overcurrent indicator. Whenever a fault occurs, the corresponding flag bit in the diagnostic register will be set and latched. The fault flags in the diagnostic register are only reset on the completion of a serial access or when a power-on-reset occurs. Resetting the diagnostic register only affects latched faults that are no longer present. For any static faults that are still present (e.g., overtemperature), the fault flag will remain set after the register reset.

At power-up or after a power-on-reset, the FF and POR bits are set, and all other bits are reset. This indicates to the external controller that a power-on-reset has taken place and all registers have been reset. Note that a power-on-reset only occurs when the VDD supply rises above its undervoltage threshold. Power-on-reset is not directly affected by the state of the VBB.

The first bit in the register is the diagnostic register flag (FF). This is high if any bits in the diagnostic register are set. When STRn goes low to start a serial write, SDO comes out of its high-impedance state and outputs the serial register fault flag. This allows the main controller to poll the A4963 through the serial interface to determine if a fault has been detected. If no faults have been detected, then the serial transfer may be terminated without generating a serial read fault by ensuring that SCK remains high while STRn is low. When STRn goes high, the transfer will be terminated, and SDO will go into its high-impedance state.

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SERIAL REGISTER REFERENCE

Table 5: Serial Register Reference*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 0	0	0	0	WR	RM1	RM0	BT3	BT2	BT1	BT0	DT5	DT4	DT3	DT2	DT1	DT0
					0	0	1	0	0	0	0	1	0	1	0	0
Config 1	0	0	1	WR	PFD	IPI	VIL3	VIL2	VIL1	VIL0	VDQ	VT4	VT3	VT2	VT1	VT0
					0	0	1	1	1	1	0	1	1	1	1	1

*Power-on-reset value shown below each input register bit.

Configuration Register 0

RM[0:1] Recirculation Mode

RM1	RM0	Recirculation Mode	Default
0	0	Auto	D
0	1	High	
1	0	Low	
1	1	Off – Non-sync Rectification	

BT[3:0] Blank Time

$$t_{BLANK} = n \times 400\ ns$$

where n is a positive integer defined by BT[3:0].

For example, for the power-on-reset condition BT[3:0] = [1000], then t_{BL}=3.2 µs.

The range of t_{BL} is 0 to 6 µs.

The accuracy of t_{BL} is determined by the system clock frequency as defined in the Electrical Characteristics table.

DT[5:0] Dead Time

$$t_{DEAD} = n \times 50\ ns$$

where n is a positive integer defined by DT[5:0].

For example, for the power-on-reset condition DT[5:0] = [01 0100] then t_{DEAD} = 1 µs.

The range of t_{DEAD} is 100 ns to 3.15 µs. Selecting a value of 0, 1, or 2 will set the dead time to 100 ns.

The accuracy of t_{DEAD} is determined by the system clock frequency as defined in the Electrical Characteristics table.

Configuration Register 1

PFD Percent Fast Decay

PFD	Percent Fast Decay (at Start)	Default
0	12.5%	D
1	25%	

IPI Invert PWM Input

IPI	PWM Input Sense	Default
0	Normal True Logic	D
1	Inverter Logic	

VIL[3:0] Current Sense Threshold Voltage for Normal Running Conditions

Typically:

$$V_{ILIM} = (n + 1) \times 12.5\ mV$$

where n is a positive integer defined by VIL[3:0].

For example, for the power-on-reset condition VIL[3:0] = [1111] then V_{ILIM} = 200 mV.

The range of V_{ILIM} is 12.5 to 200 mV.

VDQ bemf Time Qualifier

VDQ	VDS Comparator Time Qualifier	Default
0	Debounce Timer	D
1	Window Timer	

VT[4:0] VDS Threshold

Typically:

$$V_{DST} = n \times 50\ mV$$

where n is a positive integer defined by VT[4:0].

For example, for the power-on-reset condition VT[4:0] = [1 1111], then V_{DST} = 1.55 V.

The range of V_{DST} is 0 to 1.55 V.

The accuracy of V_{DST} is defined in the Electrical Characteristics table.

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Table 6: Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 2	0	1	0	WR	CP3	CP2	CP1	CP0	SH1	SH0	DGC	PW4	PW3	PW2	PW1	PW0
					0	1	1	1	1	0	0	1	0	0	1	1
Config 3	0	1	1	WR	CI3	CI2	CI1	CI0	HD3	HD2	HD1	HD0	HT3	HT2	HT1	HT0
					0	1	1	1	0	1	0	1	0	0	1	0

*Power-on-reset value shown below each input register bit.

Configuration Register 2

CP[3:0] Proportional Gain of the Position Controller

Position control proportional gain is KCP defined as:

$$K_{CP} = 2^{(n-7)}$$

where n is a positive integer defined by CP[3:0].

For example, when CP[3:0] = [1000], then $K_{CP} = 2$.

The range of K_{CP} is 1/128 to 256.

SH[0:1] Overspeed Limit Ratio

SH1	SH0	Overspeed Limit	Default
0	0	100% Max Control Speed	
0	1	125% Max Control Speed	
1	0	150% Max Control Speed	D
1	1	200% Max Control Speed	

DGC Degauss Compensation

DGC	Degauss Compensation	Default
0	Off	D
1	Active	

PW[4:0] Fixed Off-Time/Fixed Period

$$t_{PW} = 20\ \mu s + (n \times 1.6\ \mu s)$$

where n is a positive integer defined by PW[4:0].

For example, when the power-on-reset condition PW[4:0] = [1 0011], then $t_{PW} = 50.4$ µs.

The range of t_{PW} is 20 to 69.6 µs.

In fixed-frequency mode, this is equivalent to 14.4k Hz to 50 kHz.

The accuracy of t_{PW} is determined by the system clock frequency as defined in the Electrical Characteristics table.

Configuration Register 3

CI[3:0] Integral Gain of the Position Controller

Position control integral gain is K_{CI} defined as:

$$K_{CI} = 2^{(n-7)}$$

where n is a positive integer defined by CI[3:0].

For example, when CI[3:0] = [1000], then $K_{CI} = 2$.

The range of K_{CI} is 1/128 to 256.

HD[3:0] PWM Duty Cycle for Hold Torque

$$D_H = (n + 1) \times 6.25\%$$

where n is a positive integer defined by HD[3:0].

For example, where the power-on-reset condition HQ[3:0] = [0101], then $D_H = 37.5\%$.

The range of D_H is 6.25% to 100%.

HT[3:0] Hold Time

$$t_{HOLD} = n \times 8\ ms$$

where n is a positive integer defined by HT[3:0].

For example, where the power-on-reset condition HT[3:0] = [0010], then $t_{HOLD} = 16$ ms.

The range of t_{HOLD} is 0 to 120 ms.

The accuracy of t_{HOLD} is determined by the system clock frequency as defined in the Electrical Characteristics table.

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Table 7: Serial Register Reference*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 4	1	0	0	WR	SP3	SP2	SP1	SP0	SD3	SD2	SD1	SD0	SS3	SS2	SS1	SS0
					0	1	11	1	0	1	1	1	0	0	1	1
Config 5	1	0	1	WR	SI3	SI2	SI1	SI0	SPO	SMX2	SMX1	SMX0	PA3	PA2	PA1	PA0
					0	1	1	1	0	1	1	1	1	0	0	0

*Power-on-reset value shown below each input register bit.

Configuration Register 4

SP[3:0] Proportional Gain of the Speed PI Controller

Speed control proportional gain is K_{SP} defined as:

$$K_{SP} = 2^{(n-7)} \times K_{NSP}$$

where n is a positive integer defined by SP[3:0], and K_{NSP} is the nominal proportional gain of speed control.

For example, when SP[3:0] = [1000], then $K_{SP} = 2\ K_{NSP}$.

The range of K_{SP} is 1/128 to 256 K_{NSP}.

SD[3:0] PWM Duty Cycle for Torque During Forced Commutation Startup

$$D_S = (n + 1) \times 6.25\%$$

where n is a positive integer defined by SD[3:0].

For example, when the power-on-reset condition SD[3:0] = [0111], then DS = 50%.

The range of D_S is 6.25% to 100%.

The accuracy of D_S is defined in the Electrical Characteristics table.

SS[3:] Start Speed

Defined by electrical cycle frequency:

$$f_{ST} = (n + 1) \times 2\ Hz$$

where n is a positive integer defined by SS[3:0].

For example, where the power-on-reset condition SS[3:0] = [0011], then $f_{ST} = 8$ Hz.

The range of f_{ST} is 2 to 32 Hz.

The accuracy of f_{ST} is determined by the system clock frequency as defined in the Electrical Characteristics table.

Configuration Register 5

SI[3:0] Integral Gain of the Speed PI Controller

Speed control integral gain is K_{SI} defined as:

$$K_{SI} = 2^{(n-7)} \times K_{NSI}$$

where n is a positive integer defined by SI[3:0] and K_{NSI} is the nominal integral gain of speed control.

For example, when SI[3:0] = [1000], then $K_{SI} = 2\ K_{NSI}$.

The range of K_{SI} is 1/128 to 256 K_{NSI}.

SPO Speed Output Selection

SPO	Signal Output on SPD	Default
0	FG (electrical frequency)	D
1	TACHO (commutation frequency)	

SMX[2:0] Maximum Speed Setting as Maximum Electrical Cycle Frequency

$$f_{MX} = [2^{(8+n)} - 1] \times 0.1\ Hz$$

where n is a positive integer defined by SMX[2:0].

For example, where the power-on-reset condition SMX[2:0] = [101], then $f_{MX} = 819.1$ Hz.

The range of f_{MX} is 25.5 to 3,276.7 Hz.

For example, for a 6-pole pair motor this is equivalent to a default maximum speed of 8,191 rpm and maximum speed range from 255 to 32,767 rpm.

PA[3:0] Phase Advance

$$\theta_{ADV} = n \times 1.875°_{(electrical)}$$

where n is a positive integer defined by PA[3:0].

For example, where the following condition PA[3:0] = [1000], then $\theta_{ADV} = 15°$.

The range of θ_{ADV} is 0 to 28.125°$_{(electrical)}$.

The accuracy of θ_{ADV} is defined in the Electrical Characteristics table.

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Table 8: Serial Register Reference*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Run	1	1	1	WR	CM1	CM0	ESF	DI4	DI3	DI2	DI1	DI0	RSC	BRK	DIR	RUN
					0	0	0	0	0	0	0	0	1	0	0	1

*Power-on-reset value shown below each input register bit.

Run Register

CM[1:0] Selects Motor Control Mode

CM1	CM0	Motor Control Mode	Default
0	0	Indirect Speed (Duty Cycle)	D
0	1	Direct Speed (Duty Cycle)	
1	0	Closed-Loop Current	
1	1	Closed-Loop Speed	

ESF Enable Stop On Fail

ESF	Action on Fail	Default
0	No Stop on Fail; Report Fault	D
1	Stop on Fail; Report Fault	

DI[4:0] Duty Cycle Control

$$D_C = 7 + (n \times 3)\%$$

where n is a positive integer defined by DI[4:0].

For example, when DI[4:0] = 0, then serial duty cycle control is disabled and control reverts to the duty cycle of the PWM signal applied to the PWM input terminal.

The range of D_C is 10% to 100%.

RSC Restart Control

RSC	Restart	Default
0	No Restart	
1	Allow Restart after Loss of Sync	D

BRK Brake

BRK	Brake Function	Default
0	Brake Function Disabled	D
1	Brake Enabled when PWM Inactive	

DIR Direction of Rotation

DIR	Direction	Default
0	Forward (Table 1 States 1 to 6)	D
1	Reverse (Table 1 States 6 to 1)	

RUN Run Enable

RUN	Motor Activity	Default
0	Disable Outputs, Coast Motor	
1	Start and Run Motor	D

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Table 9: Serial Register Reference*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mask	1	1	0	WR	TW	OT	LOS		VS		AH	AL	BH	BL	CH	CL
					0	0	0	0	0	0	0	0	0	0	0	0
Diagnostic	FF	POR	SE		TW	OT	LOS		VS		AH	AL	BH	BL	CH	CL
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

*Power-on-reset value shown below each input register bit.

Mask Register

TW Temperature Warning
OT Overtemperature
LOS Loss of bemf Synchronization
VS VBB Undervoltage
AH Phase A High-Side V_{DS}
AL Phase A Low-Side V_{DS}
BH Phase B High-Side V_{DS}
BL Phase B Low-Side V_{DS}
CH Phase C High-Side V_{DS}
CL Phase C Low-Side V_{DS}

xx	Fault Mask	Default
0	Fault Detection Permitted	D
1	Fault Detection Disabled	

Diagnostic Register

TW High Temperature Warning
OT Overtemperature Shutdown
LOS bemf Synchronization Lost
VS Undervoltage on VBB
AH V_{DS} Fault Detected on Phase A High-Side
AL V_{DS} Fault Detected on Phase A Low-Side
BH V_{DS} Fault Detected on Phase B High-Side
BL V_{DS} Fault Detected on Phase B Low-Side
CH V_{DS} Fault Detected on Phase C High-Side
CL V_{DS} Fault Detected on Phase C Low-Side
FF Diagnostic Register Flag
POR Power-On Reset
SE Serial Transfer Error

xx	Fault Mask
0	Fault Detection Permitted
1	Fault Detection Disabled

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INPUT/OUTPUT STRUCTURES

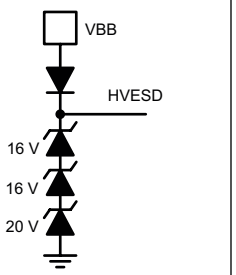

Figure 23a: Supply

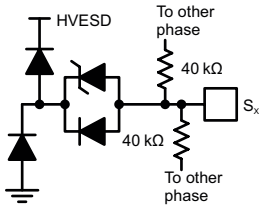

Figure 23b: Phase Inputs

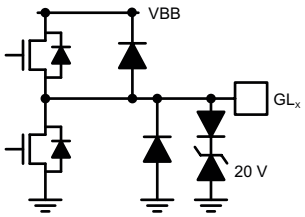

Figure 23c: LS Gate Drive

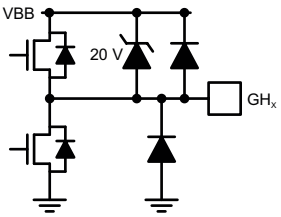

Figure 23d: HS Gate Drive

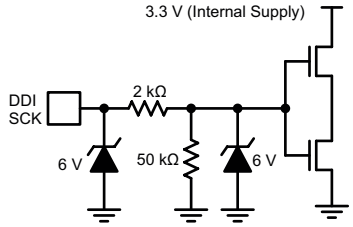

Figure 23e: SDI, SCK Inputs

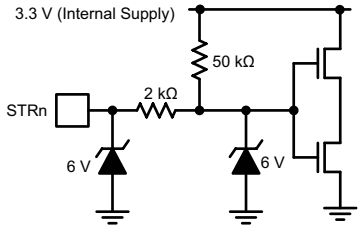

Figure 23f: STRn Input

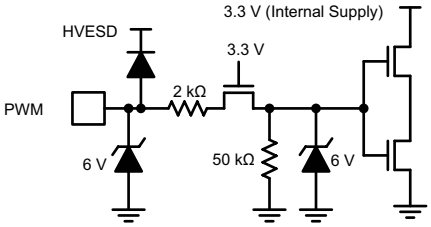

Figure 23g: PWM Input

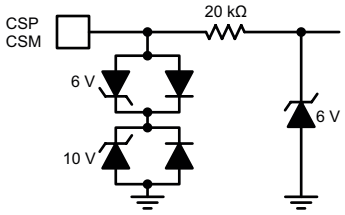

Figure 23h: Sense Inputs

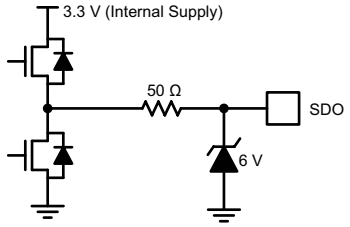

Figure 23i: SDO Output

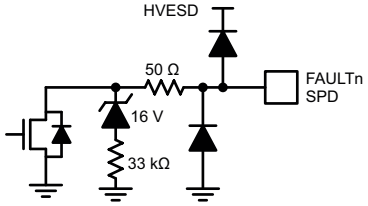

Figure 23j: FAULTn, SPD Outputs

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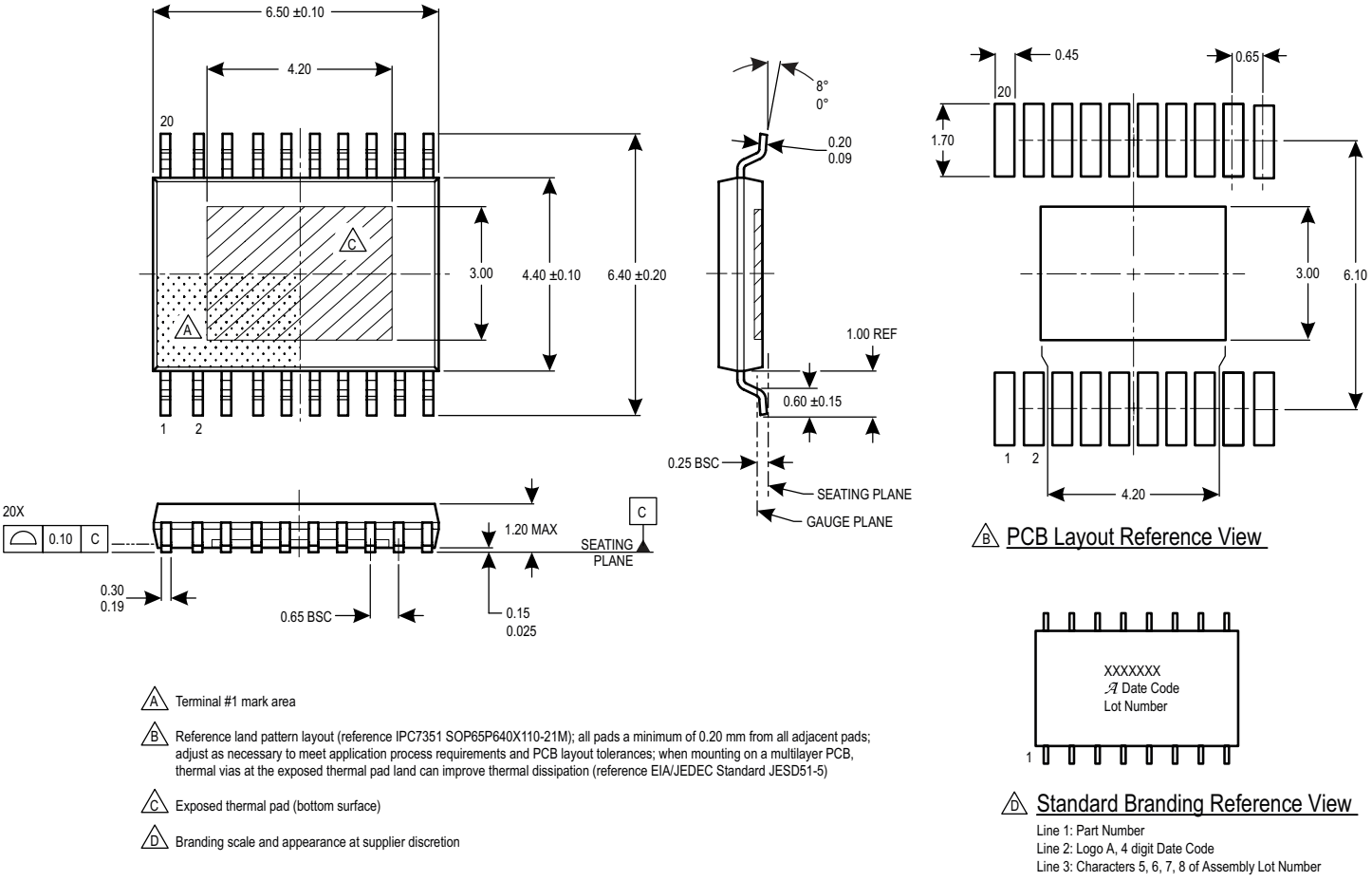
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153ACT; Allegro DWG-0000379, Rev. 3)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP65P640X110-21M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Exposed thermal pad (bottom surface)

D Branding scale and appearance at supplier discretion

Figure 24: Package LP, 20-Pin TSSOP with Exposed Pad

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REVISION HISTORY

Number	Date	Description
–	October 20, 2014	Initial release
1	November 8, 2017	Corrected Input/Output Structures (page 40)
2	November 27, 2017	Corrected Figure 23b Input/Output Structure (page 40)
3	September 11, 2018	Corrected Max Speed table (page 20)
4	September 30, 2019	Minor editorial updates
5	October 3, 2022	Updated package drawing (page 41)

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