



**FAST CMOS
20-BIT
TRANSPARENT LATCH**

IDT54/74FCT162841AT/BT/CT/ET

FEATURES:

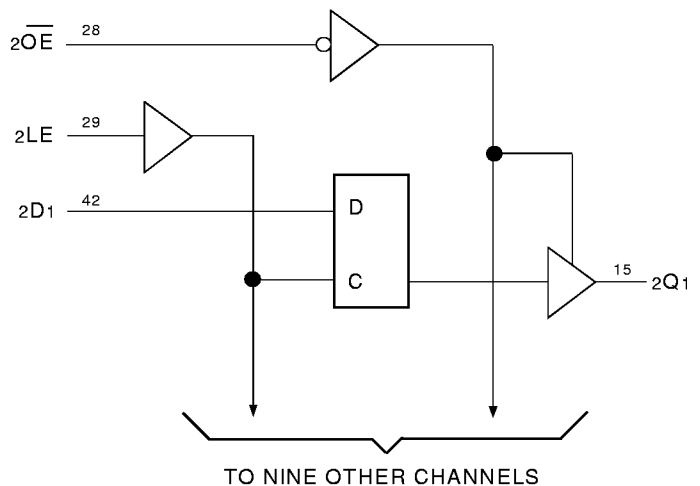
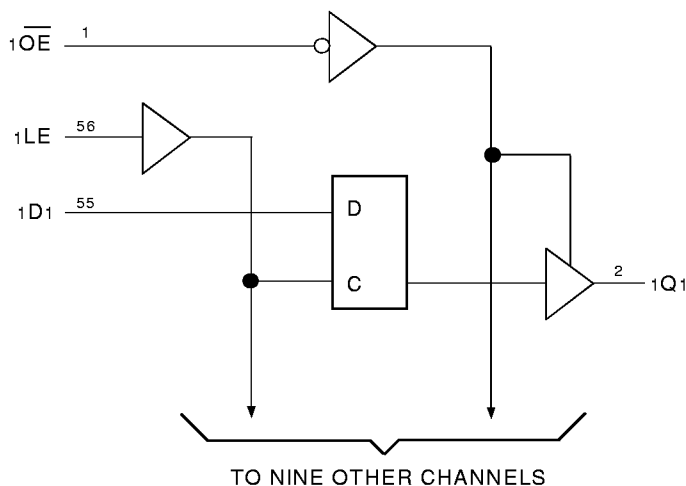
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical tsk(o) (Output Skew) < 250ps
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch CERPACK packages
- Extended commercial range of -40°C to +85°C
- Vcc = 5V $\pm 10\%$
- Balanced Output Drivers:
 - $\pm 24\text{mA}$ (commercial)
 - $\pm 16\text{mA}$ (military)
- Reduced system switching noise
- Typical VOLP (Output Ground Bounce) < 0.6V at Vcc = 5V, TA = 25°C

DESCRIPTION:

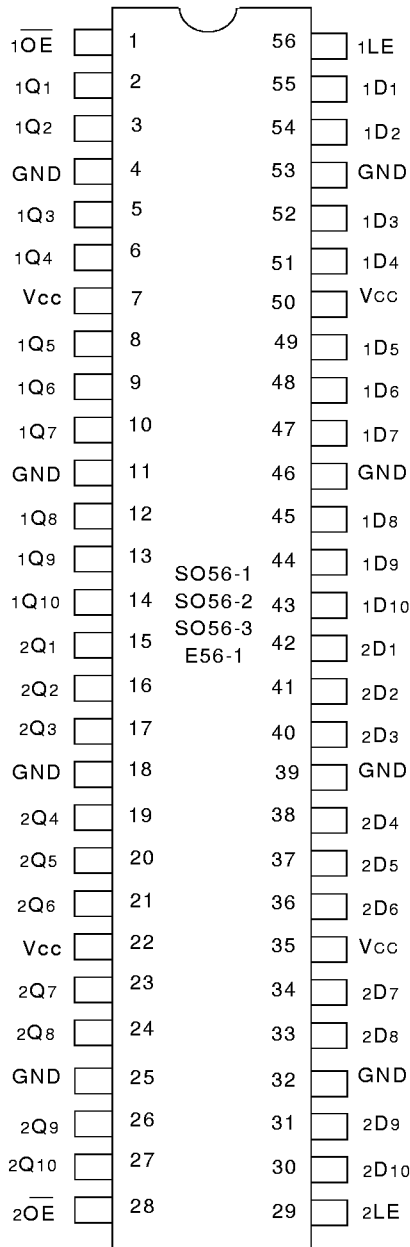
The FCT162841AT/BT/CT/ET 20-bit transparent D-type latches are built using advanced dual metal CMOS technology. These high-speed, low-power latches are ideal for temporary data storage. They can be used for implementing memory address latches, I/O ports, and bus drivers. The Output Enable ($\overline{\text{OE}}$) and Latch Enable (LE) controls are organized to operate each device as two 10-bit latches or one 20-bit latch. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT162841AT/BT/CT/ET has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The FCT162841AT/BT/CT/ET is a plug-in replacement for the FCT16841AT/BT/CT/ET and ABT16841 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP/ CERPACK
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +120	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXXXT Output and I/O terminals.
- Output and I/O terminals for FCT162XXXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	3.5	8	pF

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NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
xD _x	Data Inputs
xLE	Latch Enable Input (Active HIGH)
x \overline{OE}	Output Enable Input (Active LOW)
xQ _x	3-State Outputs

FUNCTION TABLE⁽¹⁾

Inputs			Outputs
xD _x	xLE	x \overline{OE}	xQ _x
H	H	L	H
L	H	L	L
X	L	L	Q ⁽²⁾
X	X	H	Z

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
- Output Level before xLE HIGH-to-LOW transition.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	± 1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{IL}	Input LOW Current (Input pins) ⁽⁵⁾		$V_I = \text{GND}$	—	—	± 1	
	Input LOW Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_O = 0.5\text{V}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-80	-140	-250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND or } V_{CC}$		—	5	500	μA

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OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3)}$		60	115	200	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3)}$		-60	-115	-200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -16\text{mA MIL.}$ $I_{OH} = -24\text{mA COM'L.}$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 16\text{mA MIL.}$ $I_{OL} = 24\text{mA COM'L.}$	—	0.3	0.55	V

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^\circ\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	1.5	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open $\overline{xO\bar{E}}$ = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	60	100	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _i = 10MHz 50% Duty Cycle $\overline{xO\bar{E}}$ = GND xLE = V _{CC} One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND	—	0.6	1.5	mA
			V _{IN} = 3.4V V _{IN} = GND	—	0.9	2.3	
		V _{CC} = Max. Outputs Open f _i = 2.5MHz 50% Duty Cycle $\overline{xO\bar{E}}$ = GND xLE = V _{CC} Twenty Bits Toggling	V _{IN} = V _{CC} V _{IN} = GND	—	3	5.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND	—	8	20.5 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (I}_{CCL}, I_{CCH} \text{ and } I_{CCZ})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (V}_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT162841AT				FCT162841BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay xDx to xQx (LE = HIGH)	CL = 50pF RL = 500Ω	1.5	9	1.5	10	1.5	6.5	1.5	7.5	ns
		CL = 300pF ⁽⁵⁾ RL = 500Ω	1.5	13	1.5	15	1.5	13	1.5	15	
t _{PLH} t _{PHL}	Propagation Delay xLE to xQx	CL = 50pF RL = 500Ω	1.5	12	1.5	13	1.5	8	1.5	10.5	ns
		CL = 300pF ⁽⁵⁾ RL = 500Ω	1.5	16	1.5	20	1.5	15.5	1.5	18	
t _{PZH} t _{PZL}	Output Enable Time xOE to xQx	CL = 50pF RL = 500Ω	1.5	11.5	1.5	13	1.5	8	1.5	8.5	ns
		CL = 300pF ⁽⁵⁾ RL = 500Ω	1.5	23	1.5	25	1.5	14	1.5	15	
t _{PHZ} t _{PLZ}	Output Disable Time xOE to xQx	CL = 5pF ⁽⁵⁾ RL = 500Ω	1.5	7	1.5	9	1.5	6	1.5	6.5	ns
		CL = 50pF RL = 500Ω	1.5	8	1.5	10	1.5	7	1.5	7.5	
t _{SU}	Set-Up Time HIGH or LOW, xDx to xLE	CL = 50pF RL = 500Ω	2.5	—	2.5	—	2.5	—	2.5	—	ns
t _H	Hold Time HIGH or LOW, xDx to xLE		2.5	—	3	—	2.5	—	2.5	—	ns
t _w	xLE Pulse Width HIGH		4 ⁽⁴⁾	—	5	—	4 ⁽⁴⁾	—	4 ⁽⁴⁾	—	ns
t _{SK(o)}	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.
5. This condition is guaranteed but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

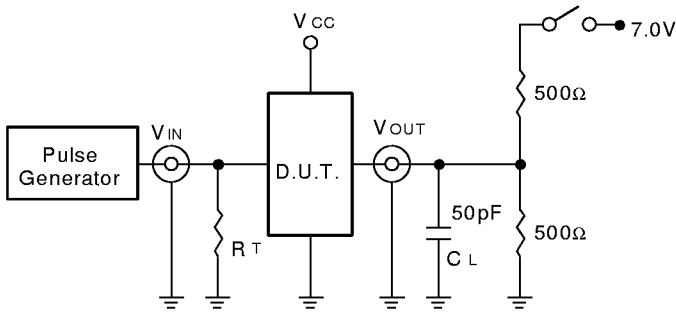
Symbol	Parameter	Condition ⁽¹⁾	FCT162841CT				FCT162841ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay xDx to xQx (LE = HIGH)	CL = 50pF RL = 500Ω	1.5	5.5	1.5	6.3	1.5	3.4	—	—	ns
		CL = 300pF ⁽⁵⁾ RL = 500Ω	1.5	13	1.5	15	1.5	7.5	—	—	
t _{PLH} t _{PHL}	Propagation Delay xLE to xQx	CL = 50pF RL = 500Ω	1.5	6.4	1.5	6.8	1.5	3.7	—	—	ns
		CL = 300pF ⁽⁵⁾ RL = 500Ω	1.5	15	1.5	16	1.5	7.5	—	—	
t _{PZH} t _{PZL}	Output Enable Time xOE to xQx	CL = 50pF RL = 500Ω	1.5	6.5	1.5	7.3	1.5	4.4	—	—	ns
		CL = 300pF ⁽⁵⁾ RL = 500Ω	1.5	12	1.5	13	1.5	9	—	—	
t _{PHZ} t _{PLZ}	Output Disable Time xOE to xQx	CL = 5pF ⁽⁵⁾ RL = 500Ω	1.5	5.7	1.5	6	1.5	3.6	—	—	ns
		CL = 50pF RL = 500Ω	1.5	6	1.5	6.3	1.5	3.6	—	—	
t _{SU}	Set-Up Time HIGH or LOW, xDx to xLE	CL = 50pF RL = 500Ω	2.5	—	2.5	—	1	—	—	—	ns
t _H	Hold Time HIGH or LOW, xDx to xLE		2.5	—	2.5	—	1	—	—	—	ns
t _W	xLE Pulse Width HIGH		4 ⁽⁴⁾	—	4 ⁽⁴⁾	—	3 ⁽⁴⁾	—	—	—	ns
t _{SK(o)}	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	—	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.
5. This condition is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

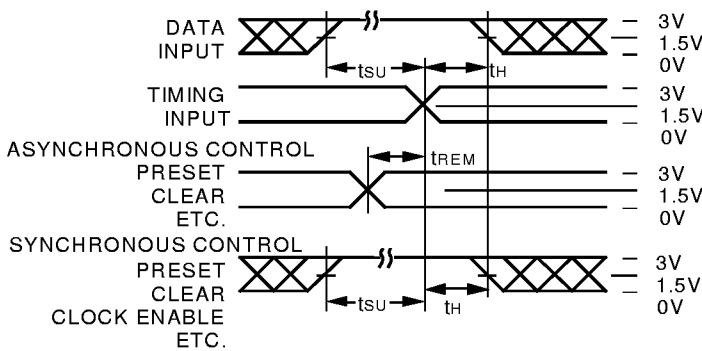
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DEFINITIONS:

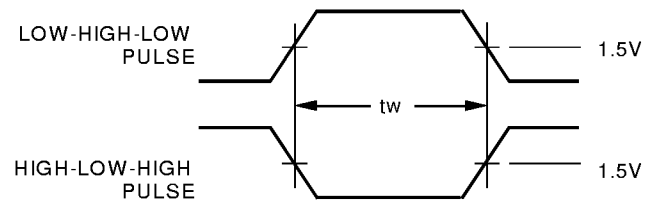
CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

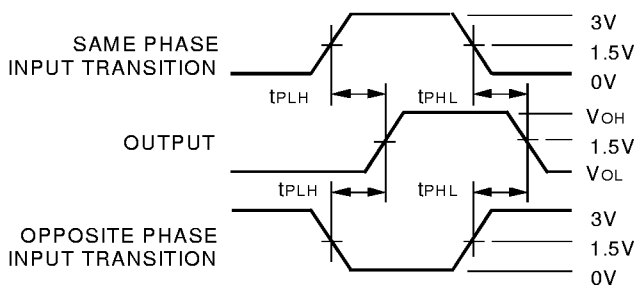
SET-UP, HOLD, AND RELEASE TIMES



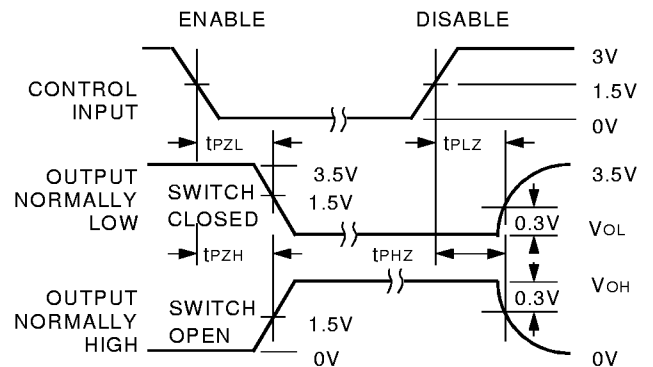
PULSE WIDTH



PROPAGATION DELAY



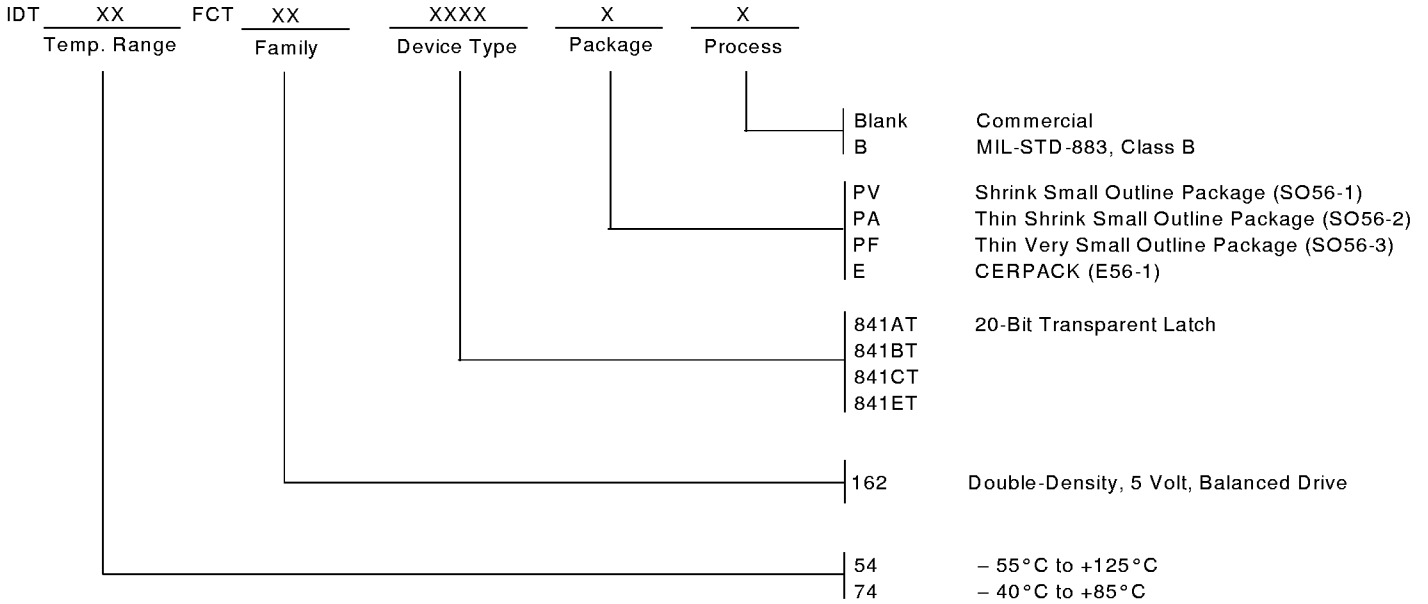
ENABLE AND DISABLE TIMES



NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate \leq 1.0MHz; $t_f \leq$ 2.5ns; $t_r \leq$ 2.5ns.

ORDERING INFORMATION



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