To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

SILICON POWER TRANSISTOR

Phase-out/Discontinued

2SA1847

PNP SILICON EPITAXIAL TRANSISTOR FOR HIGH-SPEED SWITCHING

The 2SA1847 is a power transistor developed for high-speed switching and features a high h_{FE} at low $V_{CE(sat)}$. This transistor is ideal for use as a driver in DC/DC converters and actuators.

In addition, this transistor features a package that can be auto-mounted in radial taping specifications, thus contributing to mounting cost reduction.

FEATURES

- Auto-mount possible in radial taping specifications
- Resin-molded insulation type package with power rating of 1.8 W in stand-alone conditions
- High h_{FE} and low $V_{CE(sat)}$:
  $V_{CE(sat)}$ = –0.3 V MAX. @I_C = –6.0 V, I_B = –0.3 A
  h_{FE} ≥ 100 @V_{CE} = –2.0 V, I_C = –2.0 A
- Fast switching speed

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Collector to base voltage	V_{CBO}		–150	V
Collector to emitter voltage	V_{CEO}		–100	V
Emitter to base voltage	V_{EBO}		–7.0	V
Collector current (DC)	$I_{C(DC)}$		–10	A
Collector current (pulse)	$I_{C(pulse)}$	PW ≤ 300 μs, duty cycle ≤ 2%	–20	A
Base current (DC)	$I_{B(DC)}$		–6.0	A
Total power dissipation	P_T	Ta = 25°C	1.8	W
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}		–55 to +150	°C

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Printed in Japan

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

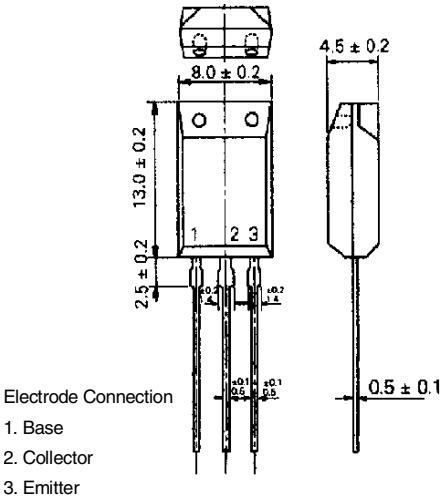
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Collector cutoff current	I_{CBO}	V_{CB} = –100 V, I_E = 0			–10	μA
Collector cutoff current	I_{CER}	V_{CE} = –100 V, R_{EB} = 50 Ω Ta = 125°C			–1.0	mA
Collector cutoff current	I_{CEX1}	V_{CE} = –100 V, $V_{BE(off)}$ = 1.5 V			–10	μA
Collector cutoff current	I_{CEX2}	V_{CE} = –100 V, $V_{BE(off)}$ = 1.5 V Ta = 125°C			–1.0	mA
Emitter cutoff current	I_{EBO}	V_{EB} = –5.0 V, I_C = 0			–10	μA
DC current gain	h_{FE1}*	V_{CE} = –2.0 V, I_C = –0.5 A	100			–
DC current gain	h_{FE2}*	V_{CE} = –2.0 V, I_C = –2.0 A	100		400	–
DC current gain	h_{FE3}*	V_{CE} = –2.0 V, I_C = –6.0 A	60			–
Collector saturation voltage	$V_{CE(sat)1}$*	I_C = –6.0 A, I_B = –0.3 A			–0.3	V
Collector saturation voltage	$V_{CE(sat)2}$*	I_C = –8.0 A, I_B = –0.4 A			–0.5	V
Base saturation voltage	$V_{BE(sat)1}$*	I_C = –6.0 A, I_B = –0.3 A			–1.2	V
Base saturation voltage	$V_{BE(sat)2}$*	I_C = –8.0 A, I_B = –0.4 A			–1.5	V
Gain bandwidth product	f_T	V_{CE} = –10 V, I_C = –0.5 A		150		MHz
Collector capacitance	C_{ob}	V_{CB} = –10 V, I_E = 0, f = 1 MHz		250		pF
Turn-on time	t_{on}	I_C = –6.0 A I_{B1} = –I_{B2} = –0.3 A R_L = 8.3 Ω, V_{CC} = –50 V			0.3	μs
Storage time	t_{stg}				1.5	μs
Fall time	t_f				0.4	μs

* Pulse test PW ≤ 350 μs, duty cycle ≤ 2%

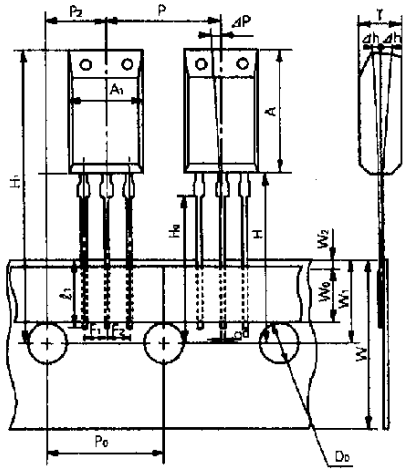
h_{FE} CLASSIFICATION

Marking	M	L	K
h_{FE}	100 to 200	150 to 300	200 to 400

PACKAGE DRAWING (UNIT: mm)



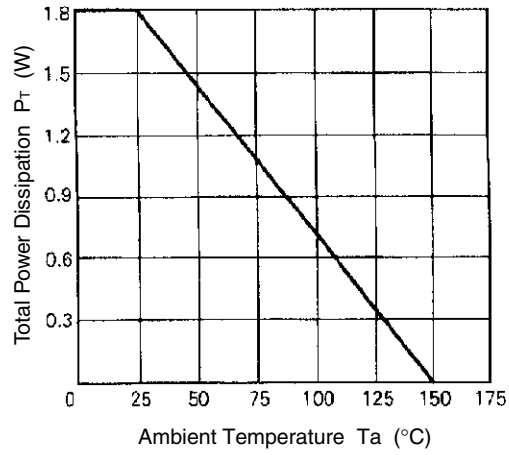
TAPING SPECIFICATION



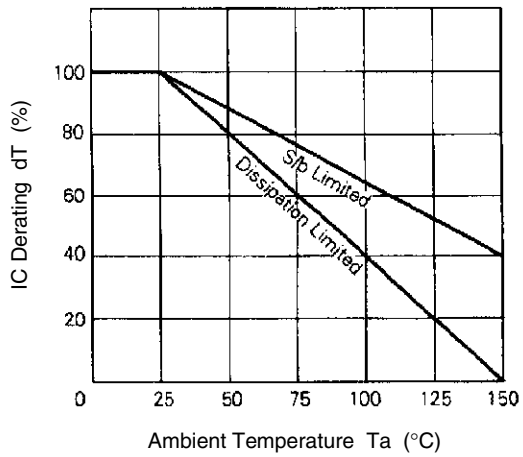
A_1	8.0 ± 0.2
A	13.0 ± 0.2
D_0	φ4.0 ± 0.2
d	0.5 ± 0.1
F_1	$2.5^{+0.4}_{-0.1}$
F_2	$2.5^{+0.4}_{-0.1}$
H	20.0 MAX.
H_0	16.0 ± 0.5
H_1	32.2 MAX.
Δh	0 ± 1.0
ℓ_1	2.5 MIN.
P	12.7 ± 1.0
P_0	12.7 ± 0.3
P_2	6.35 ± 0.5
ΔP	0 ± 1.3
T	4.5 ± 0.2
W	$18.0^{+1.0}_{-0.5}$
W_0	5.0 MIN.
W_1	9.0 ± 0.5
W_2	0.7 MIN.

TYPICAL CHARACTERISTICS (Ta = 25°C)

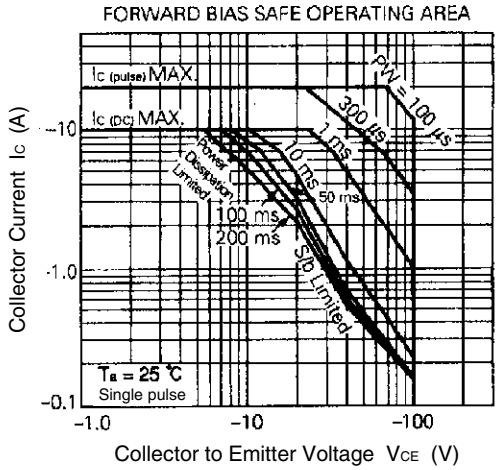
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



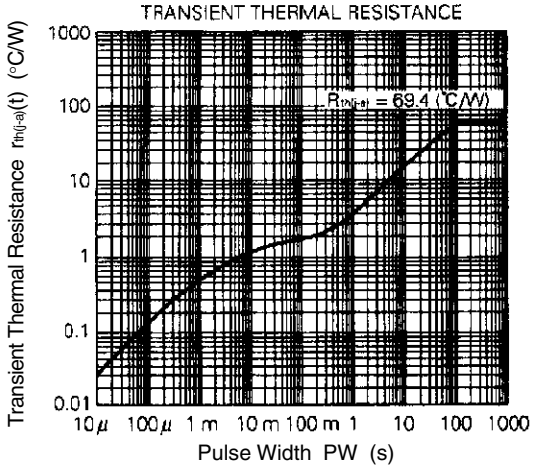
DERATING CURVE OF SAFE OPERATING AREA



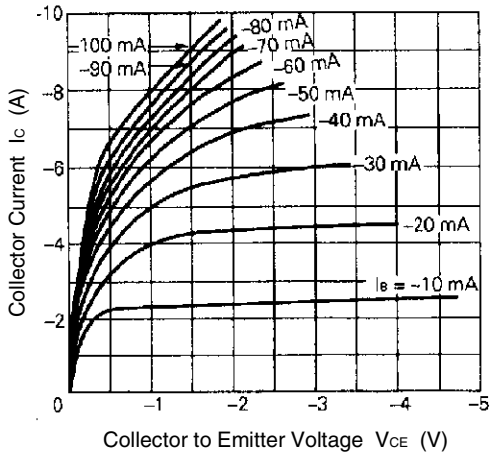
FORWARD BIAS SAFE OPERATING AREA



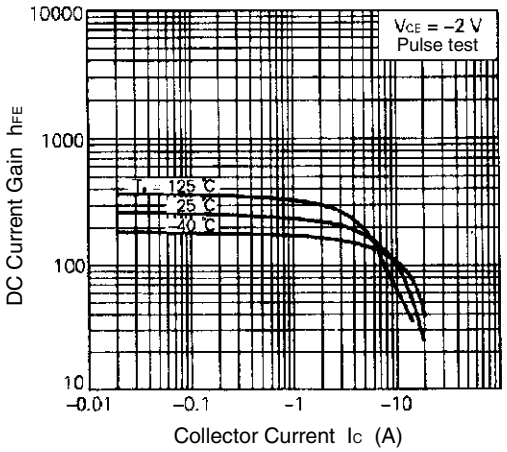
TRANSIENT THERMAL RESISTANCE



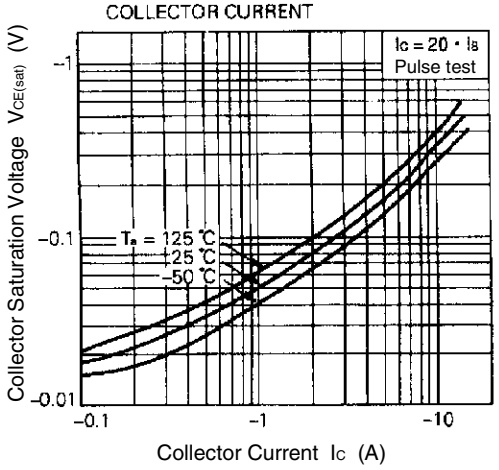
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



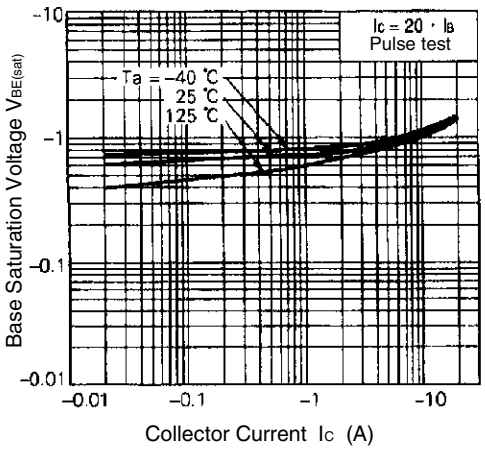
DC CURRENT GAIN vs. COLLECTOR CURRENT



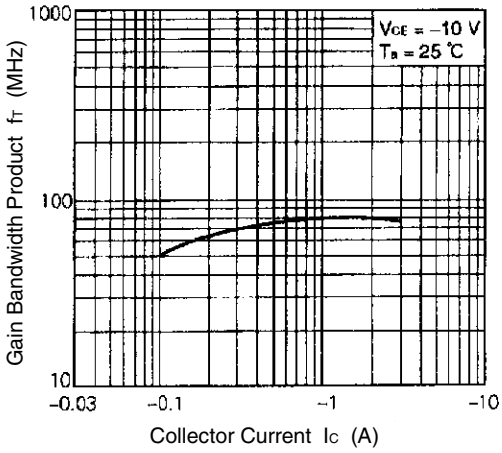
COLLECTOR SATURATION VOLTAGE vs.
COLLECTOR CURRENT



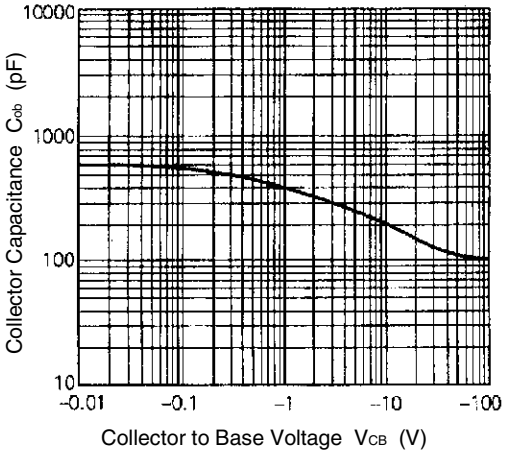
BASE SATURATON VOLTAGE vs.
COLLECTOR CURRENT



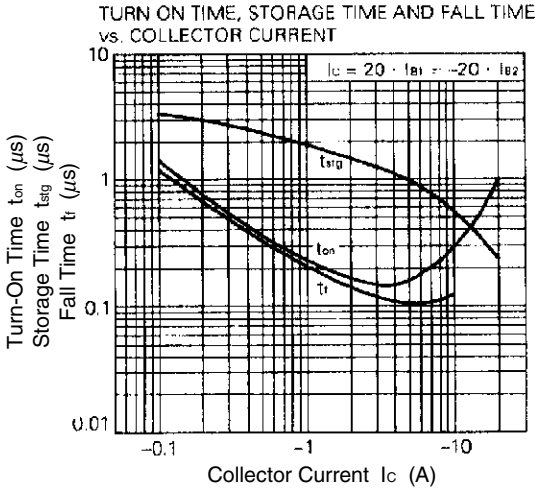
GAIN BANDWIDTH PRODUCT vs.
COLLECTOR CURRENT



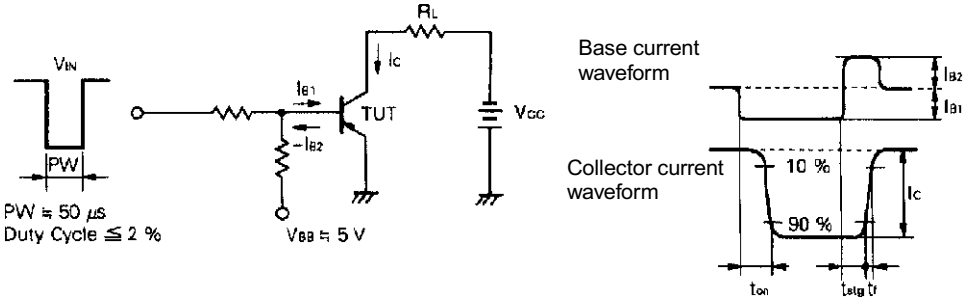
OUTPUT CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



TURN ON TIME, STORAGE TIME AND FALL TIME
vs. COLLECTOR CURRENT



SWITCHING TIME (t_{on}, t_{stg}, t_f) TEST CIRCUIT



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