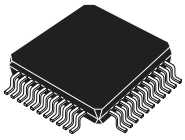
STLC3055N

WLL and ISDN-TA subscriber line interface circuit

Features

- Monochip subscriber line interface circuit (SLIC) optimised for WLL and VoIP applications
- Implement all key features of the BORSHT function
- Single supply (5.5 V to 12 V)
- Built in DC/DC converter controller
- Soft battery reversal with programmable transition time.
- On-hook transmission.
- Programmable off-hook detector threshold
- Metering pulse generation and filter
- Integrated ringing
- Integrated ring trip
- Parallel control interface (3.3 V logic level)
- Programmable constant current feed
- Surface mount package
- Integrated thermal protection
- Dual gain value option
- BCD III S, 90 V technology
- -40 to +85 °C operating range



LQFP44

Description

The STLC3055N is a SLIC device specifically designed for wireless local loop (WLL) and ISDN-terminal adaptors (ISDN-TA) and VoIP applications. One of the distinctive characteristic of this device is the ability to operate with a single supply voltage (from 5.5 V to 12 V) and self generate the negative battery by means of an on chip DC/DC converter controller that drives an external MOS switch.

The battery level is properly adjusted depending on the operating mode. A useful characteristic for these applications is the integrated ringing generator.

The control interface is a parallel type with open drain output and 3.3 V logic levels.

The metering pulses are generated on chip starting from two logic signals (0 and 3.3 V) one define the metering pulse frequency and the other the metering pulse duration. An on chip circuit then provides the proper shaping and filtering. Metering pulse amplitude and shaping (rising and decay time) can be programmed by external components. A dedicated cancellation circuit avoid possible codec input saturation due to metering pulse echo.

Constant current feed can be set from 20 mA to 40 mA. Off-hook detection threshold is programmable from 5 mA to 9 mA.

The device, developed in BCD III S technology (90 V process), operates in the extended temperature range and integrates a thermal protection that sets the device in power down when T_j exceeds 140 °C.

Table 1. Device summary

Order code	Package	Packing
E-STLC3055N (1)	LQFP44	Tray

1. ECOPACK® (see *Section 10*)

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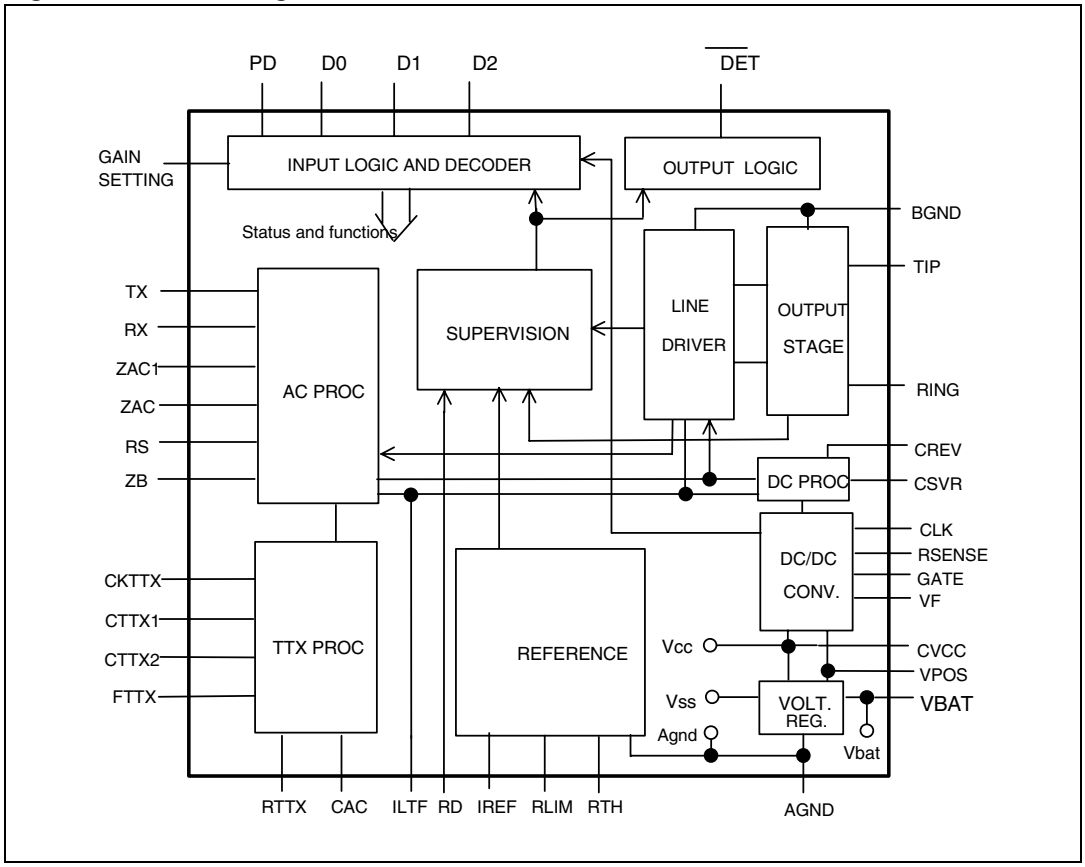
1 Block diagram

Figure 1. Block diagram



2 Pin description

Figure 2. Pin connection (top view)

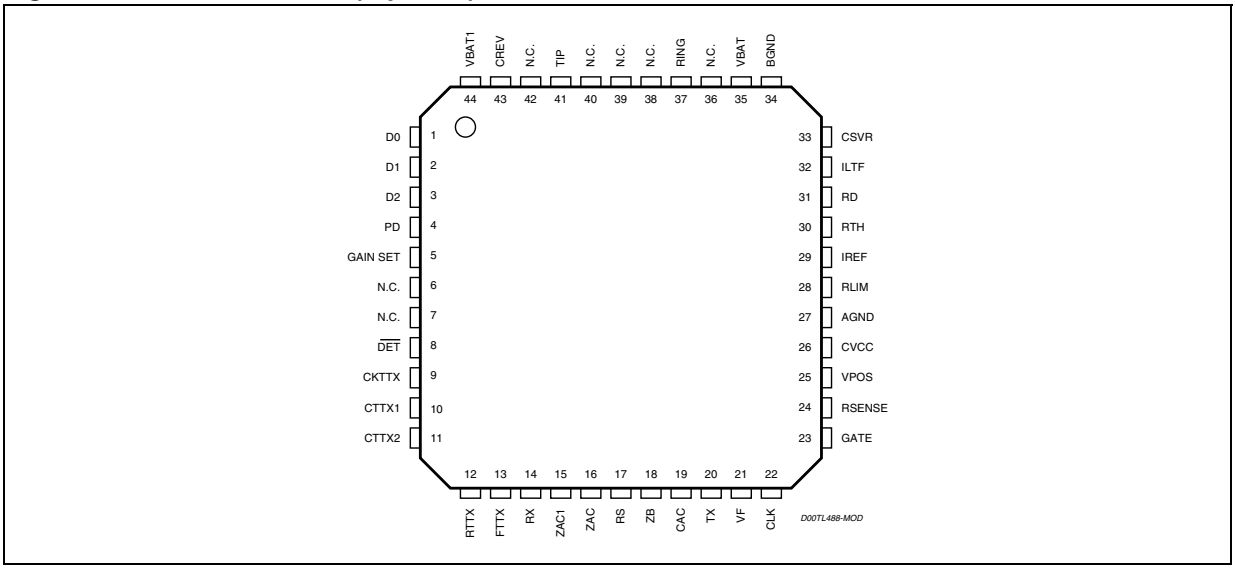


Table 2. Pin description

N°	Pin	Function
1	D0	Control Interface: input bit 0.
2	D1	Control Interface: input bit 1.
3	D2	Control interface: input bit 2.
4	PD	Power down input. Normally connected to CVCC (or to logic level high).
5	Gain SET	Control gain interface: 0 Level R_{xgain} = 0dB T_{xgain} = -6dB 1 Level R_{xgain} = +6dB T_{xgain} = -12dB
6,7,36, 38,39,40,42	NC	Not connected.
8	DET	Logic interface output of the supervision detector (active low).
9	CKTTX	Metering pulse clock input (12 KHz or 16KHz square wave).
10	CTTX1	Metering burst shaping external capacitor.
11	CTTX2	Metering burst shaping external capacitor.
12	RTTX	Metering pulse cancellation buffer output. TTX filter network should be connected to this point. If not used should be left open.
13	FTTX	Metering pulse buffer input this signal is sent to the line and used to perform TTX filtering.
14	RX	4 wire input port (RX input). A 100 kΩ external resistor must be connected to AGND to bias the input stage. This signal is referred to AGND. If connected to single supply CODEC output it must be DC decoupled with proper capacitor.
15	ZAC1	RX buffer output, (the AC impedance is connected from this node to ZAC).
16	ZAC	AC impedance synthesis.

Table 2. Pin description (continued)

N°	Pin	Function
17	RS	Protection resistors image (the image resistor is connected from this node to ZAC).
18	ZB	Balance network for 2 to 4 wire conversion (the balance impedance ZB is connected from this node to AGND. ZA impedance is connected from this node to ZAC1).
19	CAC	AC feedback input, AC/DC split capacitor (CAC).
20	TX	4 wire output port (TX output). The signal is referred to AGND. If connected to single supply CODEC input it must be DC decoupled with proper capacitor.
21	VF	Feedback input for DC/DC converter controller.
22	CLK	Power switch controller clock (typ. 125 kHz). This pin can also be connected to CVCC or AGND. When the CLK pin is connected to CVCC an auto-oscillation is internally generated and it is used instead of the external clock. When the CLK pin is connected to AGND, the GATE output is disabled.
23	GATE	Driver for external Power MOS transistor (P-channel).
24	RSENSE	Voltage input for current sensing. RSENSE should be connected close to this pin and VPOS pin. The PCB layout should minimize the extra resistance introduced by the copper tracks.
25	VPOS	Positive supply
26	CVCC	Internal positive voltage supply filter.
27	AGND	Analog ground, must be shorted with BGND.
28	RLIM	Constant current feed programming pin (via RLIM). RLIM should be connected close to this pin and AGND pin to avoid noise injection.
29	IREF	Internal bias current setting pin. RREF should be connected close to this pin and AGND pin to avoid noise injection.
30	RTH	Off-hook threshold programming pin (via RTH). RTH should be connected close to this pin and AGND pin to avoid noise injection.
31	RD	DC feedback and ring trip input. RD should be connected close to this pin and AGND pin to avoid noise injection.
32	ILTF	Transversal line current image output.
33	CSVR	Battery supply filter capacitor.
34	BGND	Battery ground, must be shorted with AGND.
35	VBAT	Regulated battery voltage self generated by the device via DC/DC converter. Must be shorted to VBAT1.
37	RING	2 wire port; RING wire (Ib is the current sunk into this pin).
41	TIP	2 wire port; TIP wire (Ia is the current sourced from this pin).
43	CREV	Reverse polarity transition time control. One proper capacitor connected between this pin and AGND is setting the reverse polarity transition time. This is the same transition time used to shape the "trapezoidal ringing" during ringing injection.
44	VBAT1	Frame connection. Must be shorted to VBAT.

3 Electrical specification

3.1 Absolute maximum rating

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{pos}	Positive supply voltage	-0.4 to +13	V
A/BGND	AGND to BGND	-1 to +1	V
V_{dig}	Pin D0, D1, D2, $\overline{DET}$, CKTTX	-0.4 to 5.5	V
T_j	Max. junction temperature	150	°C
V_{btot} (1)	Vbtot=|Vpos|+|Vbatl. (Total voltage applied to the device supply pins).	90	V
ESD RATING	Human body model	±1750	V
	Charged device model	±500	V

1. Vbat is self generated by the on chip DC/DC converter and can be programmed via RF1 and RF2. RF1 and RF2 shall be selected in order to fulfil the a.m limits (see *Table 10: External components on page 17*).

3.2 Operating range

Table 4. Operating range

Symbol	Parameter	Value	Unit
V_{pos}	Positive supply voltage	5.5 to +12	V
A/BGND	AGND to BGND	-100 to +100	mV
V_{dig}	Pin D0, D1, D2, $\overline{DET}$, CKTTX, PD	-0.25 to 5.25	V
T_{op}	Ambient operating temperature range	-40 to +85	°C
V_{bat} (1)	Self generated battery voltage	-74 max.	V

1. Vbat is self generated by the on chip DC/DC converter and can be programmed via RF1 and RF2. RF1 and RF2 shall be selected in order to fulfill the a.m limits (see *Table 10: External components on page 17*).

3.3 Thermal data

Table 5. Thermal data

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction to ambient	Typ.	60	°C/W

4 Functional description

The STLC3055N is a device specifically developed for WLL VoIP and ISDN-TA applications.

It is based on a SLIC core, on purpose optimised for these applications, with the addition of a DC/DC converter controller to fulfil the WLL and ISDN-TA design requirements.

The SLIC performs the standard feeding, signalling and transmission functions.

It can be set in four different operating modes via the D0, D1, D2 pins of the control logic interface (0 to 3.3 V logic levels). The loop status is carried out on the $\overline{DET}$ pin (active low).

The $\overline{DET}$ pin is an open drain output to allow easy interfacing with both 3.3 V and 5 V logic levels.

The four possible SLIC's operating modes are:

- Power down
- High impedance feeding (HI-Z)
- Active
- Ringing

Table 6 shows how to set the different SLIC operating modes.

Table 6. SLIC operating modes.

PD	D0	D1	D2	Operating mode
0	0	0	X	Power down
1	0	0	X	H.I. feeding (HI-Z)
1	0	1	0	Active normal polarity
1	0	1	1	Active reverse polarity
1	1	1	0	Active TTX injection (N.P.)
1	1	1	1	Active TTX injection (R.P.)
1	1	0	0/1	Ring (D2 bit toggles @ fring)

4.1 DC/DC converter

The DC/DC converter controller is driving an external power MOS transistor (P-channel) in order to generate the negative battery voltage needed for device operation.

The DC/DC converter controller is synchronised with an external CLK (125 kHz typ.) or with an internal clock generated when the pin CLK is connected to CVCC. One sensing resistor in series to Vpos supply allows to fix the maximum allowed input peak current. This feature is implemented in order to avoid overload on Vpos supply in case of line transient (ex. ring trip detection).

The typical value is obtained for a sensing resistor equal to 110 mΩ that will guarantee an average current consumption from Vpos < 700 mA. When in on-hook the self generated battery voltage is set to a predefined value.

This value can be adjusted via one external resistor (RF1) and it is typical -50 V. When RING mode is selected this value is increased to -70 V typ.

Once the line goes in off-hook condition, the DC/DC converter automatically adjust the generated battery voltage in order to feed the line with a fixed DC current (programmable via RLIM) optimising in this way the power dissipation.

4.2 Operating modes

4.2.1 Power down

When this mode is selected the SLIC is switched off and the TIP and RING pins are in high impedance. Also the line detectors are disabled therefore the off-hook condition cannot be detected.

This mode can be selected in emergency condition when it is necessary to cut any current delivered to the line.

This mode is also forced by STLC3055N in case of thermal overload (T_j > 140 °C).

In this case the device goes back to the previous status as soon as the junction temperature decrease under the hysteresis threshold.

No AC transmission is possible in this mode.

4.2.2 High impedance feeding (HI-Z)

This operating mode is normally selected when the telephone is in on-hook in order to monitor the line status keeping the power consumption at the minimum.

The output voltage in on-hook condition is equal to the self generated battery voltage (-50 V typ).

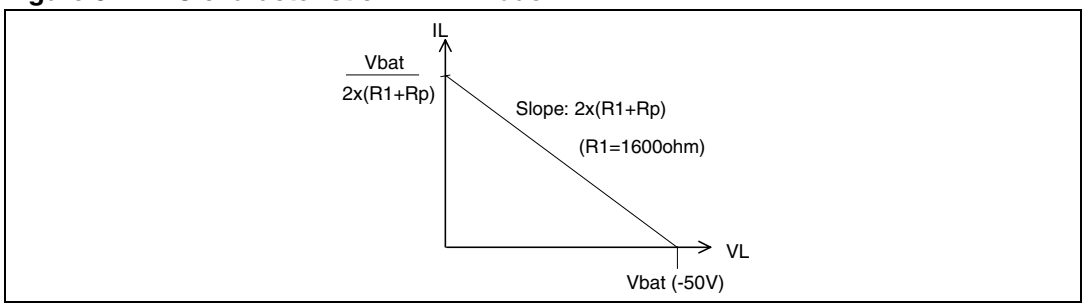
When off-hook occurs the $\overline{DET}$ becomes active (low logic level).

The off-hook threshold in HI-Z mode is the same value as programmed in ACTIVE mode.

The DC characteristic in HI-Z mode is just equal to the self generated battery with 2x(1600 Ω+Rp) in series (see *Figure 3*), where Rp is the external protection resistance.

No AC transmission is possible in this mode.

Figure 3. DC characteristic in HI-Z mode.



4.2.3 Active

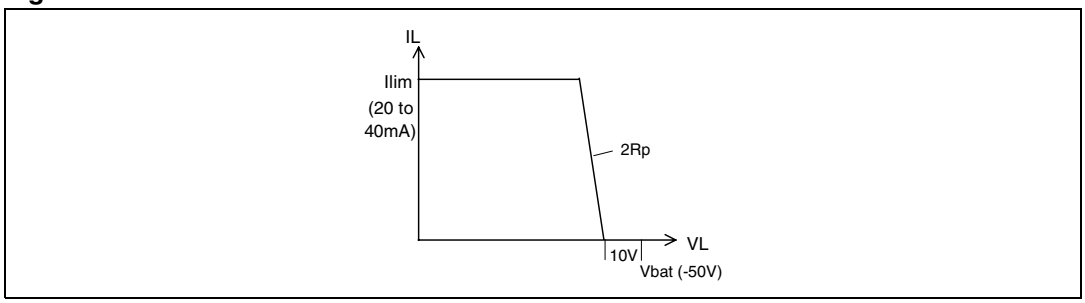
DC characteristics and supervision

When this mode is selected the STLC3055N provides both DC feeding and AC transmission.

The STLC3055N feeds the line with a constant current fixed by RLIM (20 mA to 40 mA range). The on-hook voltage is typically 40 V allowing on-hook transmission; the self generated Vbat is -50 V typ.

If the loop resistance is very high and the line current cannot reach the programmed constant current feed value, the STLC3055N behaves like a 40 V voltage source with a series impedance equal to the protection resistors 2xRp (typ. 2 x 50 Ω). *Figure 4* shows the typical DC characteristic in Active mode.

Figure 4. DC characteristic in active mode



The line status (on/off-hook) is monitored by the SLIC's supervision circuit. The off-hook threshold can be programmed via the external resistor RTH in the range from 5 mA to 9 mA.

Independently on the programmed constant current value, the TIP and RING buffers have a current source capability limited to 80 mA typ. Moreover the power available at Vbat is controlled by the DC/DC converter that limits the peak current drawn from the Vpos supply. The maximum allowed current peak is set by R_{SENSE} resistor.

AC characteristics

The SLIC provides the standard SLIC transmission functions:

Once in active mode the SLIC can operate with two different Tx, Rx Gain. Setting properly by the gain set control bit (see *Table 7*).

Table 7. Gain set in active mode

Gain set	4 to 2 wire gain	2 to 4 wire gain	Impedance synthesis scale factor
0	0 dB	-6 dB	x 50
1	+6 dB	-12 dB	x 25

- **Input impedance synthesis:** can be real or complex and is set by a scaled (x 50 or x 25) external ZAC impedance.
- **Transmit and receive:** The AC signal present on the 2W port (TIP and RING pins) is transferred to the TX output with a -6 dB or -12 dB gain and from the RX input to the 2W port with a 0 dB or +6 dB gain.
- **2 to 4 wire conversion:** The balance impedance can be real or complex, the proper cancellation is obtained by means of two external impedance ZA and ZB

Once in Active mode (D1=1) the SLIC can operate in different states setting properly D0 and D2 control bits (see also *Table 8*).

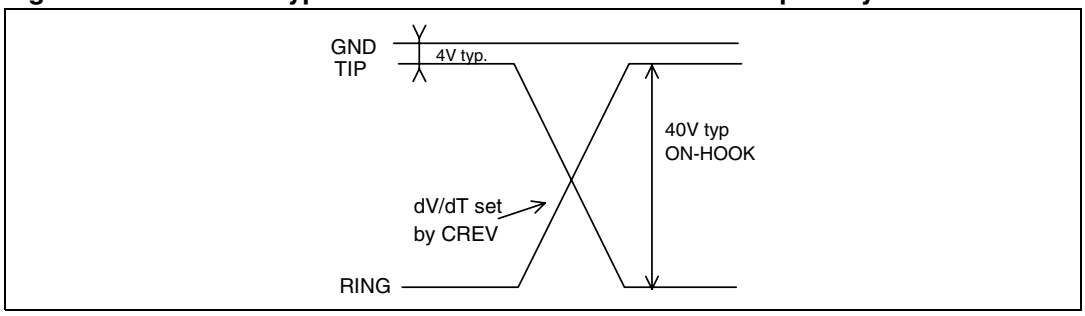
Table 8. SLIC states in active mode

D0	D1	D2	Operating Mode
0	1	0	Active normal polarity
0	1	1	Active reverse polarity
1	1	0	Active TTX injection (normal polarity)
1	1	1	Active TTX injection (reverse polarity)

Polarity reversal

The D2 bit controls the line polarity, the transition between the two polarities is performed in a "soft" way. This means that the TIP and RING wire exchange their polarities following a ramp transition (see *Figure 5*). The transition time is controlled by an external capacitor CREV. This capacitor is also setting the shape of the ringing trapezoidal waveform. When the control pins set battery reversal the line polarity is reversed with a proper transition time set via an external capacitor (CREV).

Figure 5. TIP/RING typical transition from direct to reverse polarity



Metering pulse injection (Ttx)

The metering pulses circuit consists of a burst shaping generator that gives a square wave shaped and a low pass filter to reduce the harmonic distortion of the output signal.

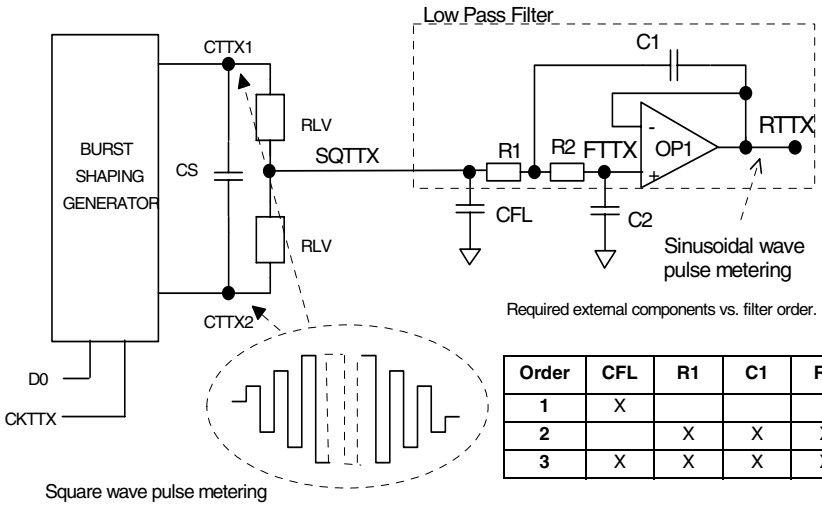
The metering pulse is obtained starting from two logic signals:

- CKTTX: is a square wave at the TTX frequency (12 or 16 kHz) and should be permanently applied to the CKTTX pin or at least for all the duration of the TTX pulse (including rising and decay phases).
- D0: enable the TTX generation circuit and define the TTX pulse duration.

These two signals are processed by a dedicated circuitry integrated on chip that generate the metering pulse as an amplitude modulated shaped squarewave (SQTTX) (see *Figure 6*).

Both the amplitude and the envelope of the squarewave (SQTTX) can be programmed by means of external components. In particular the amplitude is set by the two resistors RLV and the shaping by the capacitor CS.

Figure 6. Metering pulse generation circuit.



Required external components vs. filter order.

Order	CFL	R1	C1	R2	C2	THD
1	X					13%
2		X	X	X	X	6%
3	X	X	X	X	X	3%

The waveform so generated is then filtered and injected on the line.

The low pass filter can be obtained using the integrated buffer OP1 connected between pin FTTX (OP1 non inverting input) and RTTX (OP1 output) (see *Figure 6*) and implementing a "Sallen and Key" configuration. Depending on the external components count it is possible to build an optimised application depending on the distortion level required. In particular harmonic distortion levels equal to 13 %, 6 % and 3 % can be obtained respectively with first, second and third order filters (see *Figure 6*).

The circuit showed in *Figure 8: Application diagram with metering pulse generation. on page 20* is related to the simple first order filter.

Once the shaped and filtered signal is obtained at RTTX buffer output it is injected on the TIP/RING pins with a +6 dB gain or +12 dB gain.

It should be noted that this is the nominal condition obtained in presence of ideal TTX echo cancellation (obtained via proper setting of RTTX and CTTX).

In addition, the effective level obtained on the line will depend on the line impedance and the protection resistors value. In the typical application (TTX line impedance =200 Ω, RP = 50 Ω, and ideal TTX echo cancellation) the metering pulse level on the line will be 1.33 or 2.66 times the level applied to the RTTX pin.

As already mentioned the metering pulse echo cancellation is obtained by means of two external components (RTTX and CTTX) that should match the line impedance at the TTX frequency. This simple network has a double effect:

- Synthesize a low output impedance at the TIP/RING pins at the TTX frequency.
- Cut the eventual TTX echo that will be transferred from the line to the TX output.

4.2.4 Ringing

When this mode is selected STLC3055N self generate an higher negative battery (-70 V typ.) in order to allow a balanced ringing signal of typically 65 Vpeak.

In this condition both the DC and AC feedback are disabled and the SLIC line drivers operate as voltage buffers. The ring waveform is obtained toggling the D2 control bit at the

desired ring frequency. This bit in fact controls the line polarity (0=direct; 1=reverse). As in the Active mode the line voltage transition is performed with a ramp transition, obtaining in this way a trapezoidal balanced ring waveform (see *Figure 7*). The shaping is defined by the CREV external capacitor.

Selecting the proper capacitor value it is possible to get different CREST factor values.

The following table shows the CREST factor values obtained with a 20 Hz and 25 Hz ring frequency and with 1REN. These value are valid either with European or USA specification.

Figure 7. TIP/RING typical ringing waveform

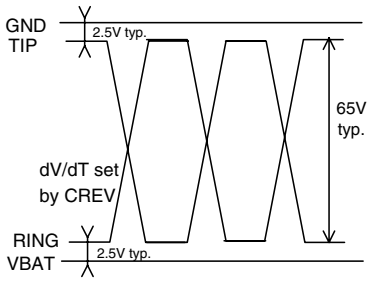


Table 9. CREST factor

CREV	CREST factor @20 Hz	CREST factor @25 Hz
22nF	1.2	1.26
27nF	1.25	1.32
33nF	1.33	Not significant (1)

1. Distortion already less than 10%.

The ring trip detection is performed sensing the variation of the AC line impedance from on-hook (relatively high) to off-hook (low). This particular ring trip method allows to operate without DC offset superimposed on the ring signal and therefore obtaining the maximum possible ring level on the load starting from a given negative battery. It should be noted that such a method is optimised for operation on short loop applications and may not operate properly in presence of long loop applications (> 500 Ω). Once ring trip is detected, the $\overline{DET}$ output is activated (logic level low), at this point the card controller or a simple logic circuit should stop the D2 toggling in order to effectively disconnect the ring signal and then set the STLC3055N in the proper operating mode (normally Active).

Ring level in presence of more telephone in parallel

As already mentioned above the maximum current that can be drawn from the Vpos supply is controlled and limited via the external R_{SENSE}. This will limit also the power available at the self generated negative battery.

If for any reason the ringer load will be too low the self generated battery will drop in order to keep the power consumption to the fixed limit and therefore also the ring voltage level will be reduced.

In the typical application with R_{SENSE} = 110 mΩ the peak current from Vpos is limited to about 900 mA, which correspond to an average current of 700 mA max. In this condition the STLC3055N can drive up to 3REN with a ring frequency fr=25 Hz (1REN = 1800 Ω + 1.0 µF, European standard).

In order to drive up to 5REN (1REN= 6930 Ω + 8 µF, US standard) it is necessary to modify the external components as follows:

CREV = 15 nF

RD = 2.2 kΩ

Rsense = 100 mΩ .

5 Application information

5.1 Layout recommendation

A properly designed PCB layout is a basic issue to guarantee a correct behavior and good noise performances. Noise sources can be identified in not enough good grounds, not enough low impedance supplies and parasitic coupling between PCB tracks and high impedance pins of the device.

Particular care must be taken on the ground connection and in this case the star configuration allows surely to avoid possible problems (see *Figure 8 on page 20* and *Figure 9 on page 21*).

The ground of the power supply (VPOS) has to be connected to the center of the star, let's call this point Supply GND. This point should show a resistance as low as possible, that means it should be a ground plane.

In particular to avoid noise problems the layout should prevent any coupling between the DC/DC converter components that are referred to PGND (CVPOS, CD, L) and analog pins that are referred to AGND (ex: RD, IREF, RTH, RLIM, VF). AGND and BGND must be shorter together. The GND connection of protection components have to be connected to the Supply GDND.

As a first recommendation the components CV, L, D1, CVPOS, RSENSE should be kept as close as possible to each other and isolated from the other components.

Additional improvements can be obtained:

- decoupling the center of the star from the analog ground of STLC3055N using small chokes.
- adding a capacitor in the range of 100 nF between VPOS and AGND in order to filter the switch frequency on VPOS.

5.2 External components list

In order to properly define the external components value the following system parameters have to be defined:

- The AC input impedance shown by the SLIC at the line terminals "Zs" to which the return loss measurement is referred. It can be real (typ. 600 Ω) or complex.
- The AC balance impedance, it is the equivalent impedance of the line "Zl" used for evaluation of the trans-hybrid loss performances (2/4 wire conversion). It is usually a complex impedance.
- The value of the two protection resistors Rp in series with the line termination. The line impedance at the TTX frequency "Zlttx".
- The metering pulse level amplitude measured at line termination "VLOTTX". In case of low order filtering, VLOTTX represents the amplitude (Vrms) of the fundamental frequency component. (typ 12 or 16 kHz).
- Pulse metering envelope rise and decay time constant "τ".
- The slope of the ringing waveform "$\Delta V_{TR}/\Delta T$ ".
- The value of the constant current limit current "Ilim".
- The value of the off-hook current threshold "I_{TH}".
- The value of the ring trip rectified average threshold current "I_{RTH}".
- The value of the required self generated negative battery "V_{BATR}" in ring mode (max value is 70 V). This value can be obtained from the desired ring peak level +5 V.
- The value of the maximum current peak sunk from Vpos "IPK".

Table 10. External components

Name	Function	Formula	Typ. value
RRX	Rx input bias resistor		100 kΩ 5%
RREF	Bias setting current	RREF = 1.3/Ibias Ibias = 50 µA	26 kΩ 1%
CSVR	Negative battery filter	CSVR = 1/(2π · fp · 1.8 MΩ) fp = 50 Hz	1.5 nF 10% 100 V
RD	Ring Trip threshold setting resistor	RD = 100/I_{RTH} 2 kΩ < RD < 5 kΩ	4.12 kΩ 1% @ IRTH = 24 mA
CAC	AC/DC split capacitance		22 µF 20% 15 V @ RD = 4.12 kΩ
RP	Line protection resistor	Rp > 30 Ω	50 Ω 1%
RLIM	Current limiting programming	RLIM = 1300/Ilim 32.5kΩ < RLIM < 65kΩ	52.3 kΩ 1% @ Ilim = 25 mA
RTH	Off-hook threshold programming (ACTIVE mode)	RTH = 290/I_{TH} 27 kΩ < RTH < 52 kΩ	32.4 kΩ 1% @I_{TH} = 9 mA
CREV	Reverse polarity transition time programming	CREV = ((1/3750) · $\Delta T/\Delta V_{TR}$)	22 nF 10% 10 V @ 12 V/ms
RDD	Pull up resistors		100 kΩ
CVCC	Internally supply filter capacitor		100 nF 20% 10 V

Table 10. External components (continued)

Name	Function	Formula	Typ. value
CVpos	Positive supply filter capacitor with low impedance for switch mode power supply		100 µF(1)
CV	Battery supply filter capacitor with low impedance for switch mode power supply		100 µF 20% 100 V (2)
CVB	High frequency noise filter		470 nF 20% 100 V
CRD (3)	High frequency noise filter		100 nF 10% 15 V
Q1	DC/DC converter switch P-channel MOS transistor	RDS(ON) ≤ 1.2 Ω,VDS = -100 V Total gate charge = 20 nC max. with VGS = 4.5 V and VDS = 1 V ID > 500 mA	Possible choiches: IRF9510 or IRF9520 or IRF9120 or equivalent
D1	DC/DC converter series diode	V_r > 100 V, t_{RR} ≤ 50 ns	SMBYW01-200 or equivalent
RSENSE	DC/DC converter peak current limiting	R_{SENSE} = 100 mV/I_{PK}	110 mΩ @I_{PK} = 900 mA
RF1	Negative battery programming level	250 kΩ < RF1 < 300 kΩ (4)	300 kΩ 1% @ V_{BATR} = -70 V
RF2	Negative battery programming level		9.1 kΩ 1 %
L	DC/DC converter inductor	DC resistance ≤ 0.1 Ω (5)	L=100 µH SUMIDA CDRH125 or equivalent

1. CVpos should be defined depending on the power supply current capability and maximum allowable ripple.
2. For low ripple application use 2 x 47 µF in parallel.
3. Can be saved if proper PCB layout avoid noise coupling on RD pin (high impedance input).

4 RF1 sets the self generated battery voltage in Ring and Active (II=0) mode as follows:

	267 kΩ	**280 kΩ**	**294 kΩ**	**300 kΩ**
$V_{BAT(ACTIVE)}$	-46 V	-48 V	-49 V	-50 V
$V_{BATR(RING)}$	-62 V	-65 V	-68 V	-70 V

V_{BATR} should be defined considering the ring peak level required (Vringpeak=V_{BATR}-6 V typ.). The above relation is valid provided that the Vpos power supply current capability and the RSENSE programming allow to source all the current requested by the particular ringer load configuration.

5 For high efficiency in HI-Z mode coil resistance @125 kHz must be < 3 Ω

Table 11. External components @gain set = 0

Name	Function	Formula	Typ. value
RS	Protection resistance image	RS = 50 · (2Rp)	5 kΩ @ Rp = 50 Ω
ZAC	Two wire AC impedance	ZAC = 50 · (Zs - 2Rp)	25 kΩ 1% @ Zs = 600 Ω
ZA(1)	SLIC impedance balancing network	ZA = 50 · Zs	30 kΩ 1% @ Zs = 600 Ω

Table 11. External components @gain set = 0 (continued)

Name	Function	Formula	Typ. value
ZB(1)	Line impedance balancing network	ZB = 50 · Zl	30 kΩ 1% @ Zl = 600 Ω
CCOMP	AC feedback loop compensation	fo = 250 kHz CCOMP = 1/(2π·fo·100·(RP))	120 pF 10% 10 V @ Rp = 50 Ω
CH	Trans-Hybrid Loss frequency compensation	CH = CCOMP	120 pF 10% 10 V
RTTX(2)	Pulse metering cancellation resistor	RTTX = 50Re (Zlttx+2Rp)	15 kΩ @Zlttx = 200 Ω real
CTTX(2)	Pulse metering cancellation capacitor	CTTX = 1/{50·2π·fttx[-Im(Zlttx)]}	100nF 10% 10V(3) @ Zlttx = 200Ω real
RLV	Pulse metering level resistor	RLV = $63.3 \cdot 10^{3} \cdot \alpha \cdot V_{LOTTX}$ α = (|Zlttx + 2Rp|/|Zlttx|)	16.2 kΩ @ V_{LOTTX} = 170mVrms
CS	Pulse metering shaping capacitor	CS = τ/(2·RLV)	100 nF 10% 10V @ τ = 3.2 ms, RLV = 16.2 kΩ
CFL	Pulse metering filter capacitor	CFL = 2/(2π·fttx·RLV)	1.5 nF 10% 10 V @fttx = 12 kHz RLV = 16.2 kΩ

1. In case Zs=Zl, ZA and ZB can be replaced by two resistors of same value: RA=RB=|Zs|.
2. Defining ZTTX as the impedance of RTTX in series with CTTX, RTTX and CTTX can also be calculated from the following formula:
ZTTX=50*(Zlttx+2Rp).
3. In this case CTTX is just operating as a DC decoupling capacitor (fp=100 Hz).

Table 12. External components @gain set = 1

Name	Function	Formula	Typ. value
RS	Protection resistance image	RS = 25 · (2Rp)	2.55 kΩ @ Rp = 50 Ω
ZAC	Two wire AC impedance	ZAC = 25 · (Zs - 2Rp)	12.5 kΩ 1% @ Zs = 600 Ω
ZA(1)	SLIC impedance balancing network	ZA = 25 · Zs	15 kΩ 1% @ Zs = 600 Ω
ZB(1)	Line impedance balancing network	ZB = 25 · Zl	15 kΩ 1% @ Zl = 600 Ω
CCOMP	AC feedback loop compensation	fo = 250kHz CCOMP = 2/(2π·fo·100·(RP))	220 pF 10% 10VL @ Rp = 50 Ω
CH	Trans-Hybrid Loss frequency compensation	CH = CCOMP	220 pF 10% 10 V
RTTX(2)	Pulse metering cancellation resistor	RTTX = 25Re (Zlttx+2Rp)	7.5 kΩ @Zlttx = 200 Ω real
CTTX(2)	Pulse metering cancellation capacitor	CTTX = 1/25·2π·fttx·[-Im(Zlttx)]	100 nF 10% 10 V(3) @ Zlttx = 200 Ω real
RLV	Pulse metering level resistor	RLV = $31.7 \cdot 10^{3} \cdot \alpha \cdot V_{LOTTX}$ α = (|Zlttx + 2Rp|/|Zlttx|)	16.2 kΩ @ V_{LOTTX} = 340 mVrms

Table 12. External components @gain set = 1 (continued)

Name	Function	Formula	Typ. value
CS	Pulse metering shaping capacitor	CS = τ/(2·RLV)	100 nF 10% 10V @ τ = 3.2 ms, RLV = 16.2 kΩ
CFL	Pulse metering filter capacitor	CFL = 2/(2π·fttx·RLV)	1.5nF 10% 10 V @fttx = 12 kHz RLV = 16.2 kΩ

1. In case Zs=Zl, ZA and ZB can be replaced by two resistors of same value: RA=RB=|Zs|.
2. Defining ZTTX as the impedance of RTTX in series with CTTX, RTTX and CTTX can also be calculated from the following formula:
ZTTX=50*(Zlttx+2Rp).
3. In this case CTTX is just operating as a DC decoupling capacitor (fp=100 Hz).

5.3 Application diagram

Figure 8. Application diagram with metering pulse generation.

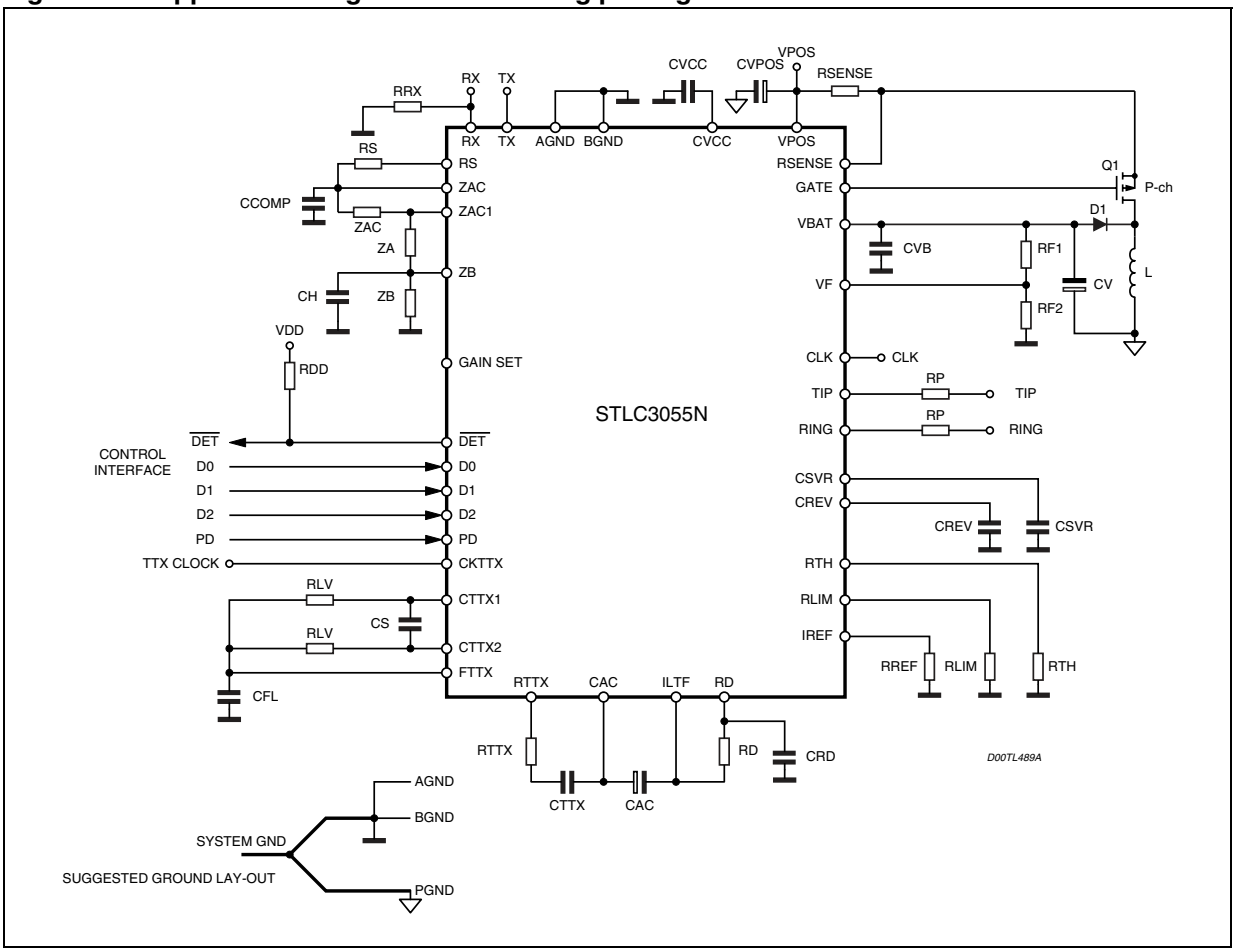
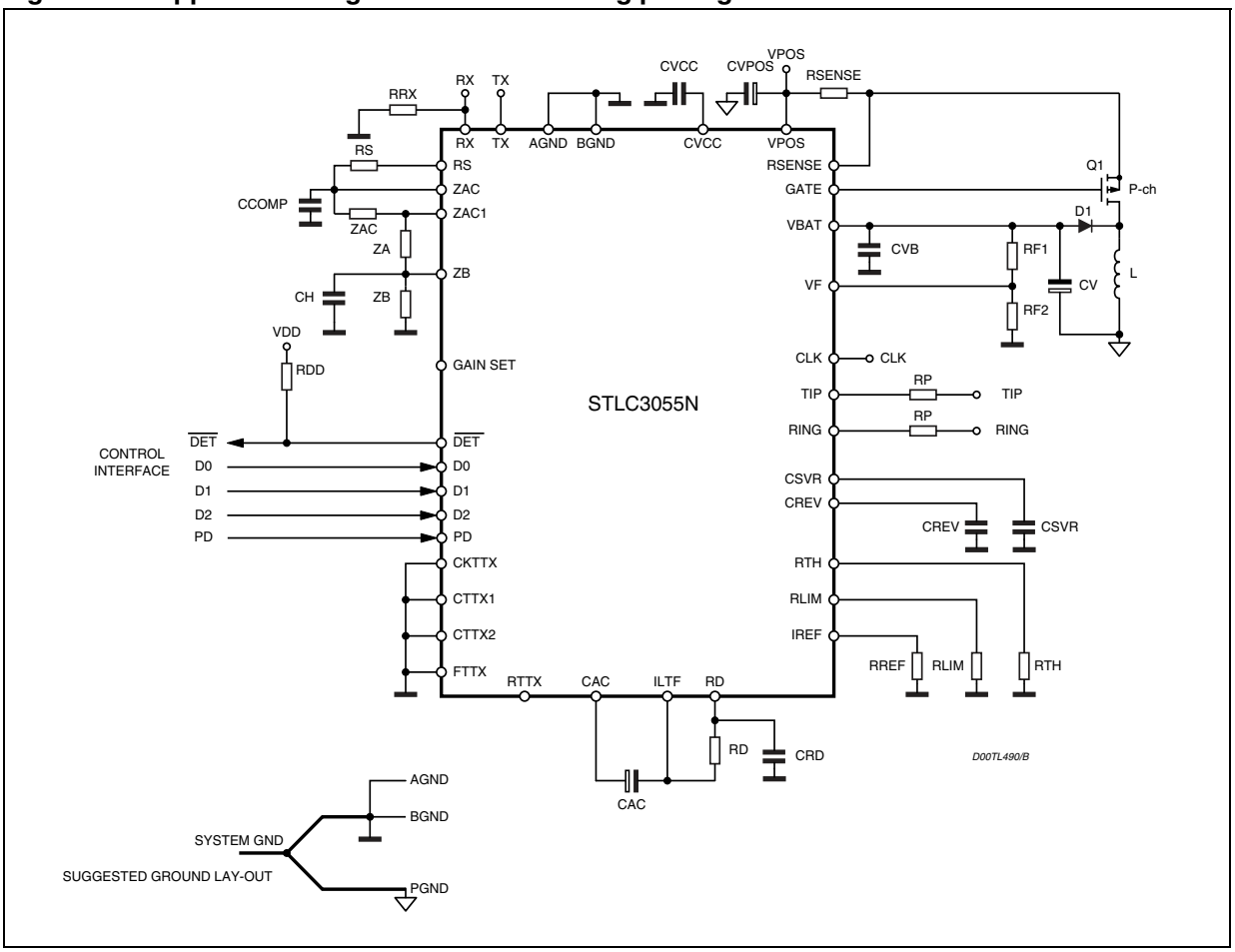


Figure 9. Application diagram without metering pulse generation



6 Electrical characteristics

Table 13. Electrical characteristics

Test conditions: V_{pos} = 6.0V, AGND = BGND, normal polarity, T_{amb} = 25 °C.
External components as listed in the "typical values" column of external components table.
Note: Testing of all parameter is performed at 25 °C. Characterisation as well as design rules used allow correlation of tested performances at other temperatures. All parameters listed here are met in the operating range: -40 to +85 °C.

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
DC characteristics						
V_{lohi}	Line voltage	Il = 0, HI-Z (High impedance feeding) T_{amb} = 0 to 85 °C	44	50		V
V_{lohi}	Line voltage	Il = 0, HI-Z (High impedance feeding) T_{amb} = -40 to 85 °C	42	48		V
V_{loa}	Line voltage	Il = 0, ACTIVE T_{amb} = 0 to 85 °C	33	40		V
V_{loa}	Line voltage	Il = 0, ACTIVE T_{amb} = -40 to 85 °C	31	37		V
Ilim	Lim. current programming range	ACTIVE mode	20		40	mA
Ilima	Lim. current accuracy	ACTIVE mode. Rel. to programmed value 20 mA to 40 mA	-10		10	%
Rfeed HI	Feeding resistance	HI-Z (High Impedance feeding)	2.4		3.6	kΩ
AC characteristics						
L/T	Long. to transv. (see *Section 6.1: Test circuits.*)	Rp = 50 Ω, 1% tol., ACTIVE N. P., R_L = 600 Ω (1) f = 300 to 3400 Hz	50	58		dB
T/L	Transv. to long. (see *Section 6.1: Test circuits.*)	Rp = 50 Ω, 1% tol., ACTIVE N. P., R_L = 600 Ω (1) f = 300 to 3400 Hz	40	45		dB
T/L	Transv. to long. (see *Section 6.1: Test circuits.*)	Rp = 50 Ω, 1% tol., ACTIVE N. P., R_L = 600 Ω (1) f = 1 kHz	48	53		dB
2WRL	2W return loss	300 to 3400 Hz, ACTIVE N. P., R_L = 600 Ω (1)	22	26		dB
THL	Trans-hybrid loss	300 to 3400 Hz, 20Log|VRX/VTX|, ACTIVE N. P., R_L = 600 Ω (1)	30			dB

Table 13. Electrical characteristics (continued)

Test conditions: V_{pos} = 6.0V, AGND = BGND, normal polarity, T_{amb} = 25 °C.
External components as listed in the "typical values" column of external components table.
Note: Testing of all parameter is performed at 25 °C. Characterisation as well as design rules used allow correlation of tested performances at other temperatures. All parameters listed here are met in the operating range: -40 to +85 °C.

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Ovl	2W overload level	at line terminals on ref. imped. ACTIVE N. P., R_L = 600 Ω (1)	3.2			dBm
TXoff	TX output offset	ACTIVE N. P., R_L = 600 Ω (1)	-250		250	mV
G24	Transmit gain abs.	0 dBm @ 1020 Hz, ACTIVE N. P., R_L = 600 Ω (1)	-6.4		-5.6	dB
G42	Receive gain abs.	0 dBm @ 1020 Hz, ACTIVE N. P., R_L = 600 Ω (1)	-0.4		0.4	dB
G24f	TX gain variation vs. freq.	rel. 1020Hz; 0 dBm, 300 to 3400 Hz, ACTIVE N. P., R_L = 600 Ω (1)	-0.12		0.12	dB
G24f	RX gain variation vs. freq.	rel. 1020 Hz; 0 dBm, 300 to 3400 Hz, ACTIVE N. P., R_L = 600 Ω (1)	-0.12		0.12	dB
V2Wp	Idle channel noise at line 0dB gainset	psophometric filtered ACTIVE N. P., R_L = 600 Ω (1) T_{amb} = 0 to +85 °C		-73	-68	dBmp
V2Wp	Idle channel noise at line 0dB gainset	psophometric filtered ACTIVE N. P., R_L = 600 Ω (1) T_{amb} = -40 to +85 °C		-68		dBmp
V4Wp	Idle channel noise at line 0dB gainset	psophometric filtered ACTIVE N. P., R_L = 600 Ω (1) T_{amb} = 0 to +85 °C		-75	-70	dBmp
V4Wp	Idle channel noise at line 0dB gainset	psophometric filtered ACTIVE N. P., R_L = 600 Ω (1) T_{amb} = -40 to +85 °C		-75		dBmp
Thd	Total Harmonic Distortion	ACTIVE N. P., R_L = 600 Ω (1)			-44	dB
VTTX	Metering pulse level on line	ACTIVE - TTX; Gain Set = 1 Zl = 200 Ω fttx = 12 kHz;	260	340		mVrms
CLKfreq	CLK operating range		-10%	125	10%	kHz
Ring						
Vring	Line voltage	RING D2 toggling @ fr = 25 Hz Load = 3REN; Crest Factor = 1.25 1REN = 1800 Ω + 1.0 µF T_{amb} = 0 to +85°C	45	49		Vrms

Table 13. Electrical characteristics (continued)

Test conditions: V_{pos} = 6.0V, AGND = BGND, normal polarity, T_{amb} = 25 °C.
External components as listed in the "typical values" column of external components table.
Note: Testing of all parameter is performed at 25 °C. Characterisation as well as design rules used allow correlation of tested performances at other temperatures. All parameters listed here are met in the operating range: -40 to +85 °C.

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Vring	Line voltage	RING D2 toggling @ fr = 25Hz Load = 3REN; Crest Factor = 1.25 1REN = 1800Ω + 1.0µF T_{amb} = -40 to +85°C	44	48		Vrms
Detectors						
IOFFTHA	Off/hook current threshold	ACT. mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)	10.5			mA
ROFTHA	Off/hook loop resistance threshold	ACT. mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)			3.4	kΩ
IONTHA	On/hook current threshold	ACT. mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)			6	mA
RONTHA	On/hook loop resistance threshold	ACT. mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)	8			kΩ
IOFFTHI	Off/hook current threshold	Hi Z mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)	10.5			mA
ROFFTHI	Off/hook loop resistance threshold	Hi Z mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)			800	Ω
IONTHI	On/hook current threshold	Hi Z mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)			6	mA
RONTHI	On/hook loop resistance threshold	Hi Z mode, RTH = 32.4kΩ 1% (Prog. ITH = 9mA)	8			kΩ
Irt	Ring Trip detector threshold range	Ring mode	20		50	mA
Irta	Ring Trip detector threshold accuracy	Ring mode	-15		15	%
Trtd	Ring trip detection time	Ring mode		60		ms
Td	Dialling distortion	Active mode	-1		1	ms
Rlrt (2)	Loop resistance				500	Ω
ThAl	Tj for th. alarm activation			160		°C

Table 13. Electrical characteristics (continued)

Test conditions: V_{pos} = 6.0V, AGND = BGND, normal polarity, T_{amb} = 25 °C.
External components as listed in the "typical values" column of external components table.
Note: Testing of all parameter is performed at 25 °C. Characterisation as well as design rules used allow correlation of tested performances at other temperatures. All parameters listed here are met in the operating range: -40 to +85 °C.

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Digital interface INPUTS: D0, D1, D2, PD, CLK OUTPUTS: $\overline{DET}$						
Vih	In put high voltage		2			V
Vil	Input low voltage				0.8	V
Iih	Input high current		-10		10	µA
Iil	Input low current		-10		10	µA
Vol	Output low voltage	Iol = 1mA			0.45	V
PSRR and power consumption						
PSERRC	Power supply rejection Vpos to 2W port	Vripple = 100mVrms 50 to 4000Hz	26	36		dB
Ivpos	Vpos supply current @ ii = 0	HI-Z On-Hook ACTIVE On-Hook, RING (line open)		13 50 55	25 80 90	mA mA mA
Ipk	Peak current limiting accuracy	RING Off-Hook RSENSE = 110mΩ	-20%	950	+20%	mApk

1. R_L: Line Resistance
2. Rlrt = Maximum loop resistance (incl. telephone) for correct ring trip detection.

6.1 Test circuits

Referring to the application diagram shown in *Figure 8 on page 20* and using as external components the typical values specified in the *Table 10 on page 17* and *Table 11 on page 18*, find below the proper configuration for each measurement.

All measurements requiring DC current termination should be performed using "Wandel & Goltermann DC Loop Holding Circuit GH-1" or equivalent.

Figure 10. 2W return loss *2WRL = 20Log(|Zref + Zs|/|Zref-Zs|) = 20Log(E/2Vs)*

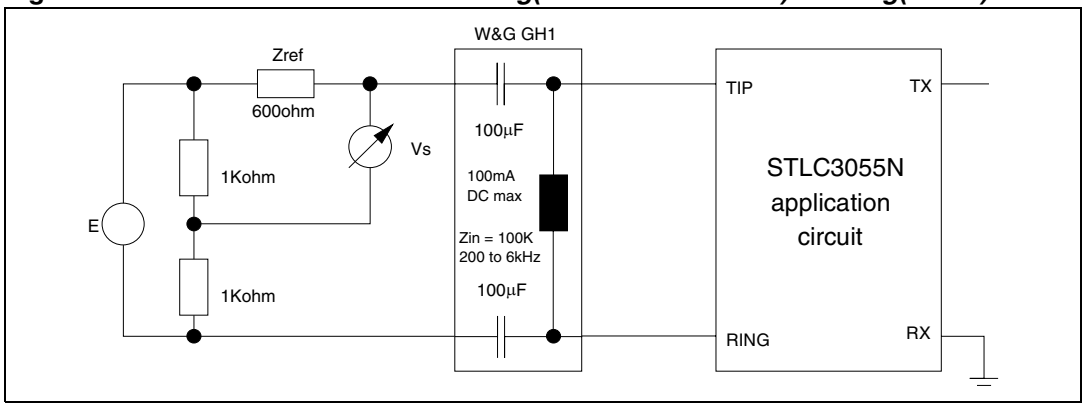


Figure 11. THL trans hybrid loss *THL = 20Log|Vrx/Vtx|*

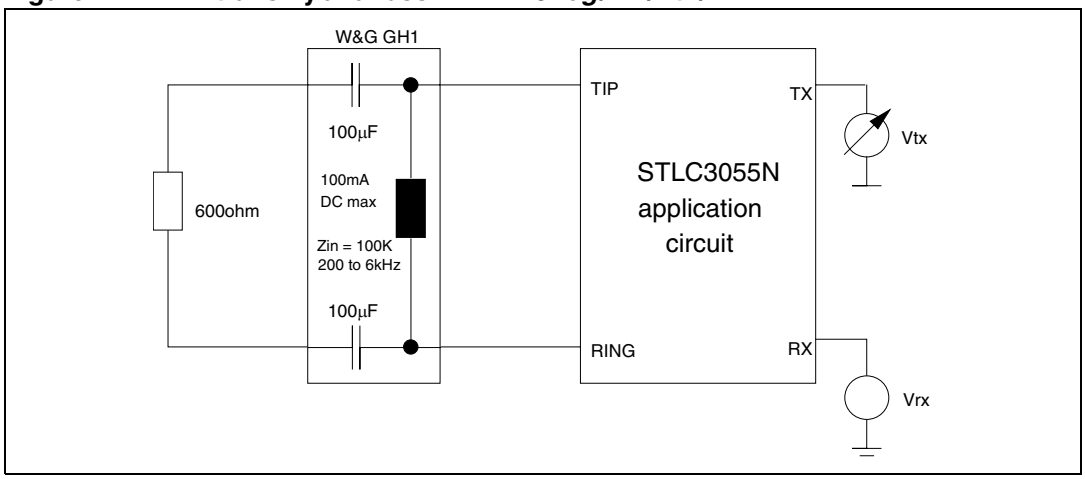


Figure 12. G24 transmit gain *G24 = 20Log|2Vtx/E|*

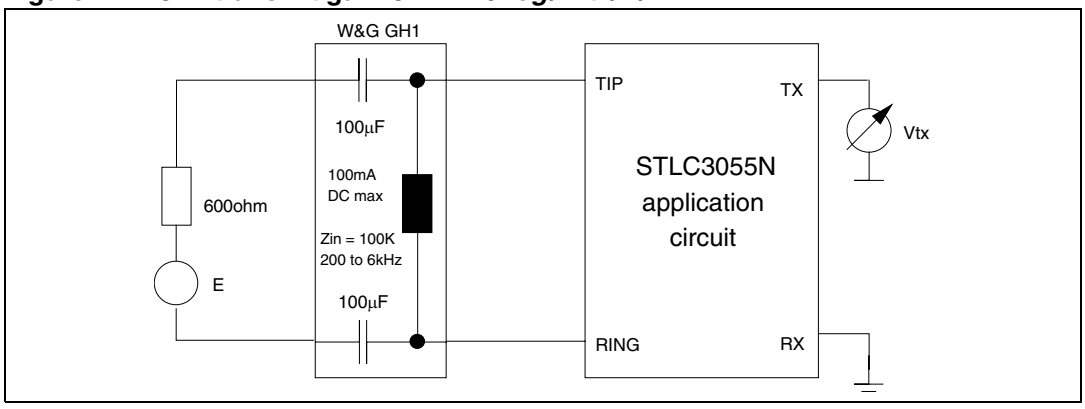


Figure 13. G42 receive gain *G42 = 20Log|VI/Vrx|*

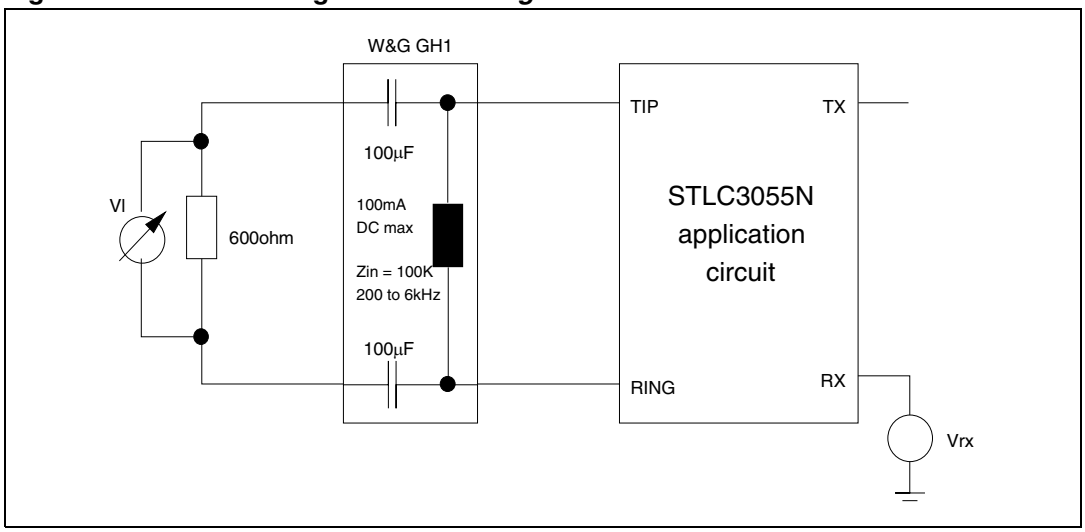


Figure 14. PSRRC power supply rejection Vpos to 2W port *PSSRC = 20Log|Vn/VI|*

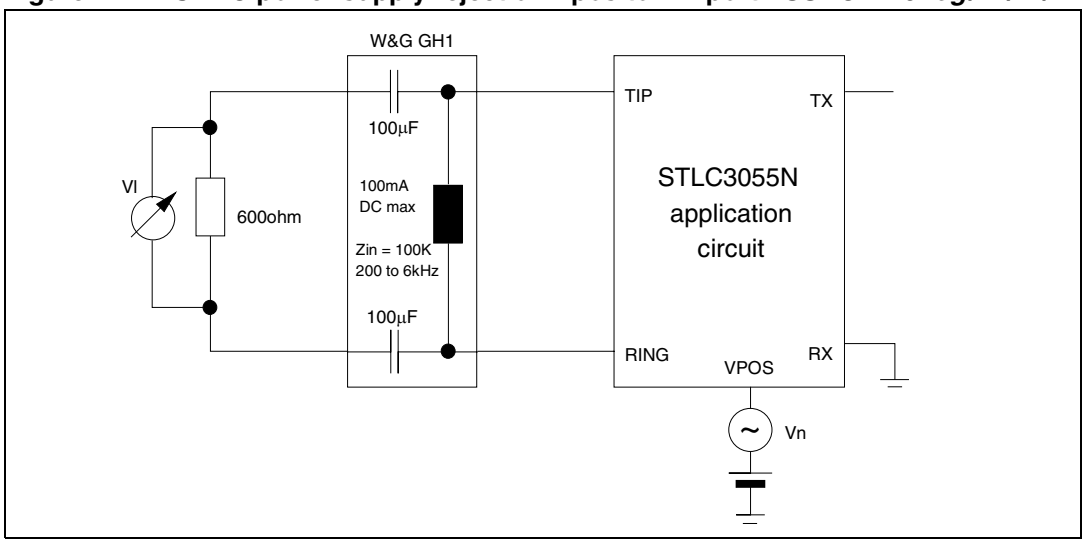


Figure 15. L/T longitudinal to transversal conversion *L/T = 20Log|Vcm/VI|*

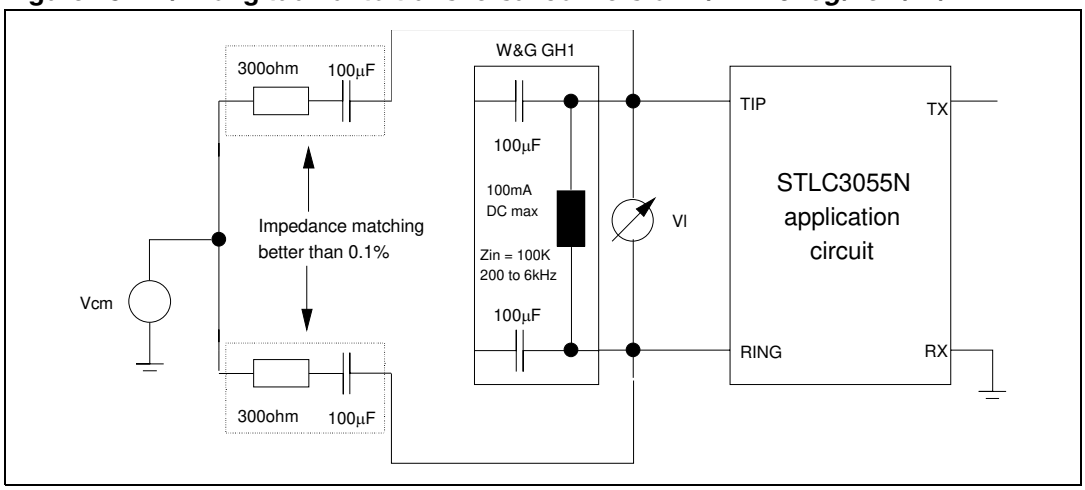


Figure 16. T/L transversal to longitudinal conversion *T/L = 20Log|Vrx/Vcm|*

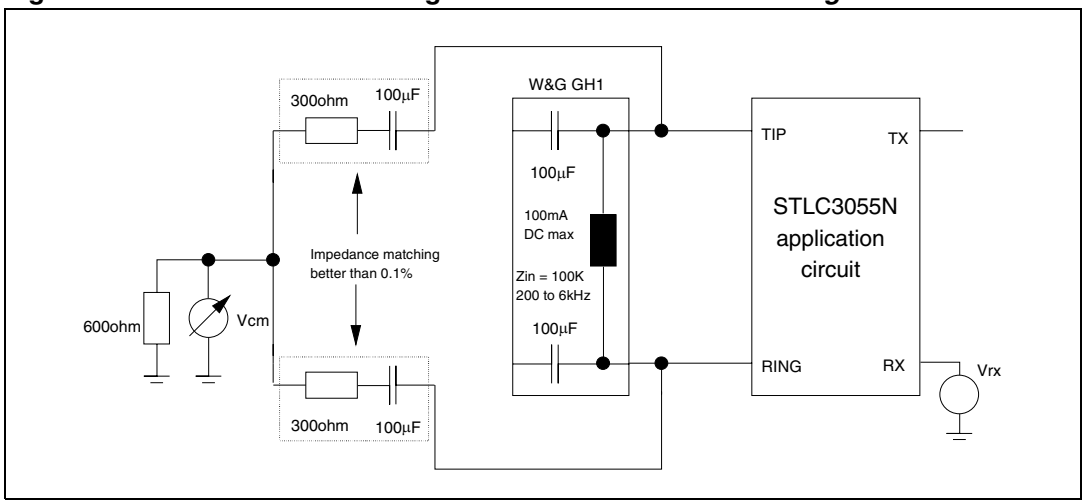


Figure 17. VTTX metering pulse level on line

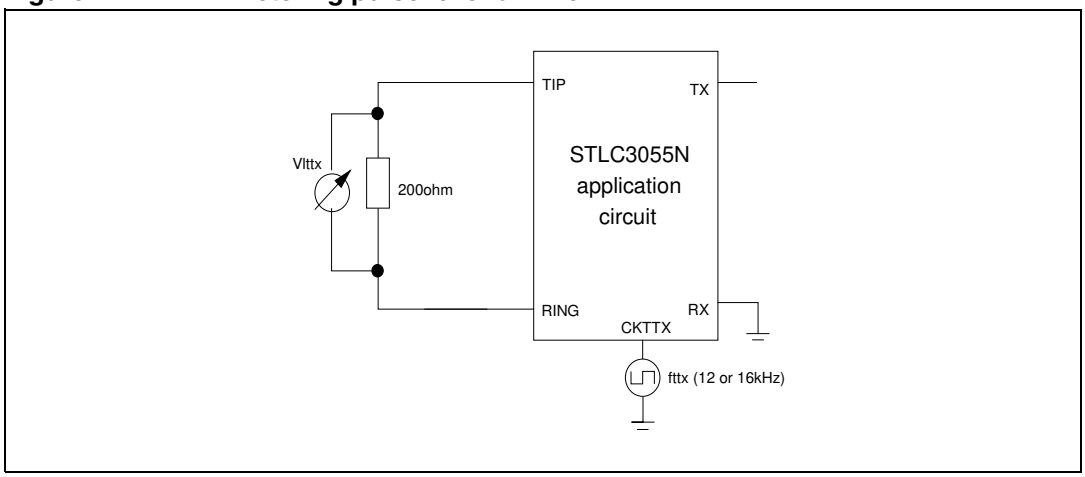
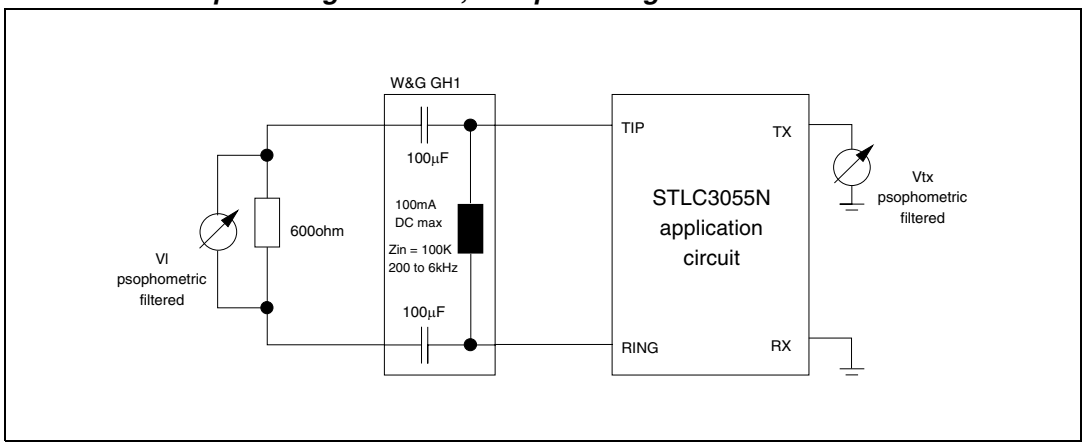


Figure 18. V2Wp and W4Wp: idle channel psophometric noise at line and TX. *V2Wp = 20Log|Vl/0.774l|; V4Wp = 20Log|Vtx/0.774l|*



7 Overvoltage protection

Figure 19. Simplified configuration for indoor overvoltage protection

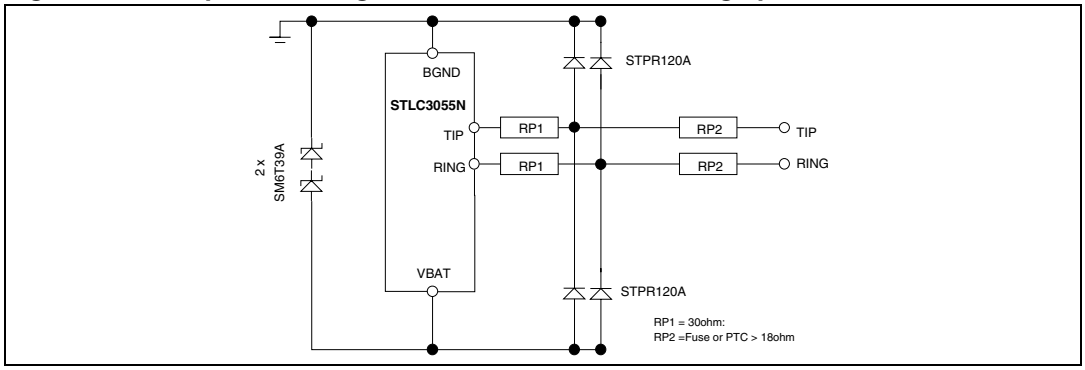
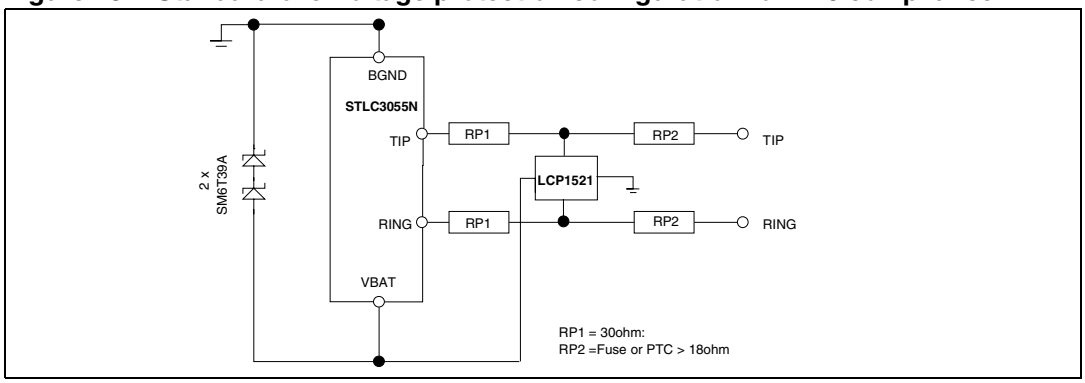
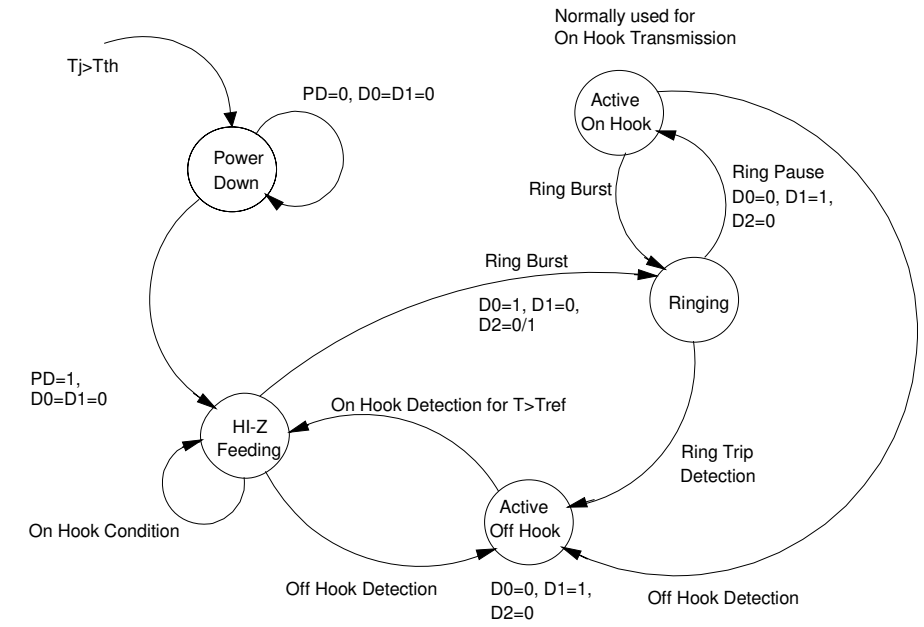


Figure 20. Standard overvoltage protection configuration for K20 compliance



8 Typical state diagram for STLC3055N operation

Figure 21. State diagram



Note: all state transitions are under the microprocessor control.

9 STLC3055Q vs STLC3055N compatibility.

STLC3055N is pin to pin compatible with the old STLC3055Q but offer a better performance in term of power consumption and can be set in a new gain configuration in order to be compatible with the 3.3 V codec.

9.1 Typical power consumption comparison

Table 14. Power consumption differences

Operative mode	STLC3055Q	STLC3055N
HI-Z	52 - 60 mA	13 - 25 mA
Active on hook	93 - 115 mA	50 - 80 mA
Ring (no REN)	120 - 140 mA	55 - 90 mA

To meet this result some differences, with a minimum impact on the application, has been introduced in STLC3055N.

9.2 Hardware differences

- **RX input.** In STLC3055N it is necessary a 100 kΩ external resistor between RX input and AGND to bias the input stage.
- **Rp.** The STLC3055N required a Rp value of 50 Ω instead of 41 Ω.
- **TTX filter.** To optimize the ttx signal dynamic, the values of RLV and CFL have been changed;

Table 15. Hardware differences

Component	STLC3055Q	STLC3055N
RRX		100 kΩ
Rp	41 Ω	50 Ω
RLV	27 kΩ	16.2 kΩ
CFL	1 nF	1.5 nF

9.3 Parameter differences

Table 16. Parameter differences

Parameter	STLC3055Q	STLC3055N
Absolute max. rating	17 V	13 V
Operating range	15.8 V	12 V
Typ. metering pulse level (Gs 1)		340 mVrms
Typ. metering pulse level (Gs 0)	200 mV_{rms}	170 mV_{rms}

10 Package information

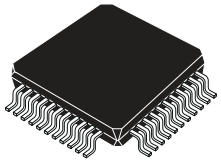
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK® is an ST trademark.

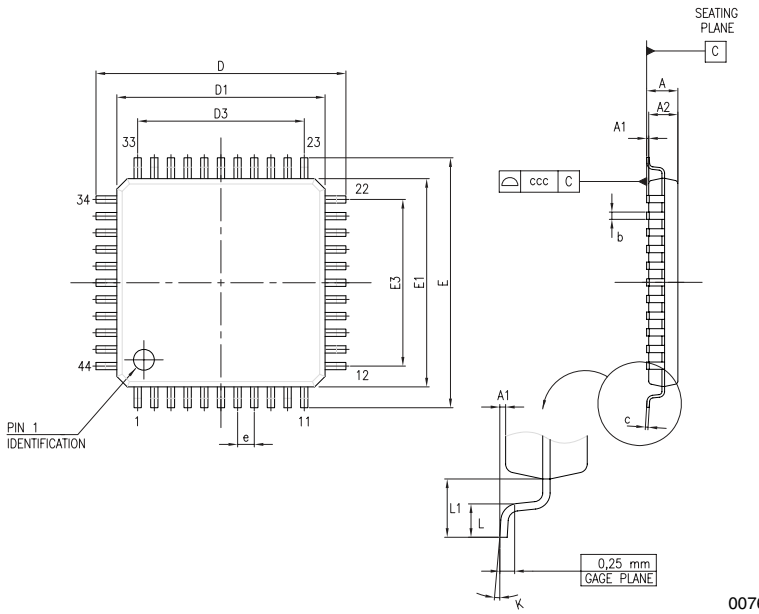
Figure 22. LQFP44 (10 x 10 x 1.4 mm) mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		8.00			0.315	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		8.00			0.315	
e		0.80			0.031	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°(min.), 3.5°(typ.), 7°(max.)					
ccc			0.10			0.0039

OUTLINE AND MECHANICAL DATA



LQFP44 (10 x 10 x 1.4mm)



11 Revision history

Table 17. Document revision history

Date	Revision	Changes
11-Sep-2003	4	First Issue
01-Oct-2004	5	Update Functional Description and Electrical Characteristics. Aligned the graphic style to be compliant with the new “Corporate Technical Publications Design Guide”
15-Oct-2004	6	Modified the application diagrams and some typo errors.
05-Nov-2004	7	Removed all max. values of the ‘Line Voltage’ parameter on the page 14/24. Changed the unit from mA to % of the ‘Ilima’ parameter on the page 14/24.
15-Jan-2005	8	Add pin 4 PD in Applications and Block Diagram Add in Table 2 ‘ESD Rating’
01-Jul-2005	9	Changed VTTX value
21-Feb-2006	10	Added part number “E-STLC3055N” (ECOPACK). Added RRX resistance in the figures 9 and 10. Added Appendix D.
12-Feb-2009	11	Document reformatted. Updated *Section 10: Package information on page 32*.

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