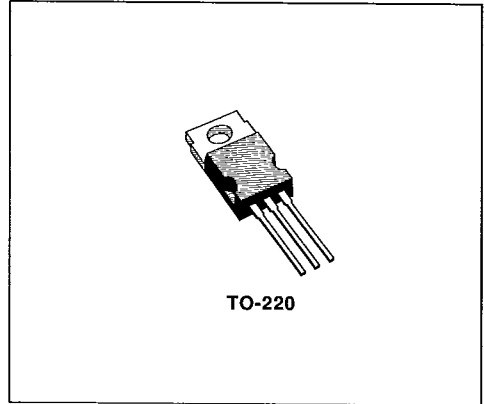
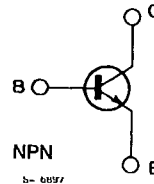


DESCRIPTION

The MJE13004/13005 are silicon multiepitaxial mesa NPN transistors in Jedec TO-220 plastic package particularly intended for switch-mode applications.



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		MJE13004	MJE13005	
V_{CEV}	Collector-emitter Voltage	600	700	V
V_{CEO}	Collector-emitter Voltage ($I_B = 0$)	300	400	V
V_{EBO}	Emitter-base ($I_C = 0$)	9		V
I_C	Collector Current	4		A
I_{CM}	Collector Peak Current	8		A
I_B	Base Current	2		A
I_{BM}	Base Peak Current	4		A
P_{tot}	Total Power Dissipation at $T_{case} \leq 25^\circ C$	75		W
T_{stg}	Storage Temperature	- 65 to 150		$^\circ C$
T_j	Junction Temperature	150		$^\circ C$

THERMAL DATA

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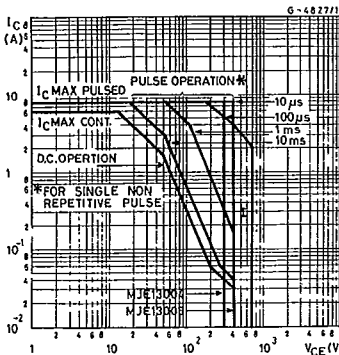
$R_{th\ j-case}$	Thermal Resistance Junction-case	max	1.67	$^{\circ}C/W$
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ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{cEV}	Collector Cutoff Current ($V_{BE} = -1.5V$)	for MJE13004 $V_{CE} = 600V$ $V_{CE} = 600V$ $T_{case} = 100^{\circ}C$ for MJE13005 $V_{CE} = 700V$ $V_{CE} = 700V$ $T_{case} = 100^{\circ}C$			1 5	mA mA
I_{EBO}	Emitter Cutoff Current ($I_C = 0$)	$V_{EB} = 9V$			1	mA
$V_{CE0(sus)}^*$	Collector-emitter Sustaining Voltage ($I_B = 0$)	$I_C = 10mA$ for MJE13004 for MJE13005	300 400			V V
$V_{CE(sat)}^*$	Collector-emitter Saturation Voltage	$I_C = 1A$ $I_B = 0.2A$ $I_C = 2A$ $I_B = 0.5A$ $I_C = 4A$ $I_B = 1A$			0.5 0.6 1	V V V
$V_{BE(sat)}^*$	Base-emitter Saturation Voltage	$I_C = 1A$ $I_B = 0.2A$ $I_C = 2A$ $I_B = 0.5A$			1.2 1.6	V V
h_{FE}	DC Current Gain	$I_C = 1A$ $V_{CE} = 5V$ $I_C = 2A$ $V_{CE} = 5V$	10 8	30	60 40	
t_{on} t_s t_f	Turn-on Time Storage Time Fall Time	$I_C = 2A$ $I_{B1} = -I_{B2} = 0.4A$ $V_{CC} = 250V$			0.8 4 0.9	μs μs μs

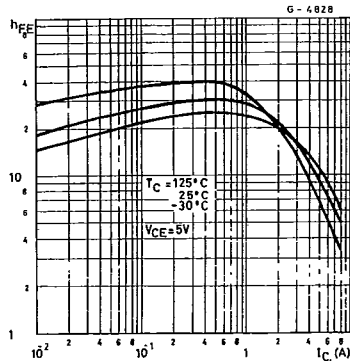
* Pulsed : pulse duration = 300 μs , duty cycle = 1.5%.

Safe Operating Areas.

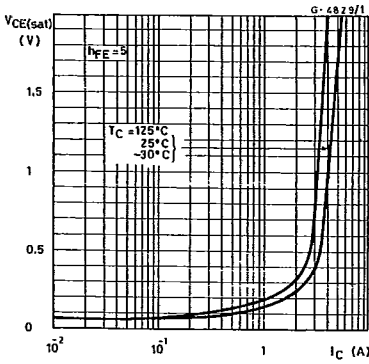


1 - Area of permissible operation during turn-on provided $R_{BE} \leq 100\Omega$ and $t_p \leq 0.25\mu s$.

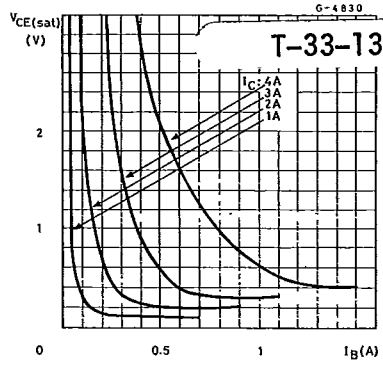
DC Current Gain.



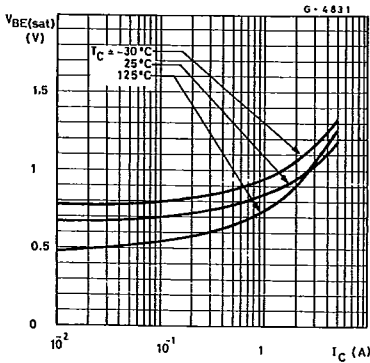
Collector-emitter Saturation Voltage.



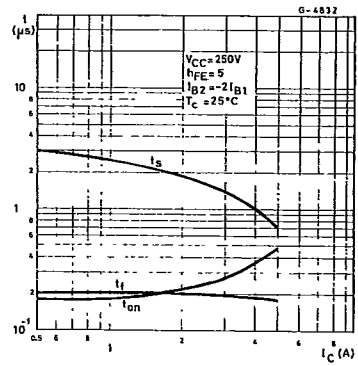
Collector-emitter Saturation Voltage.



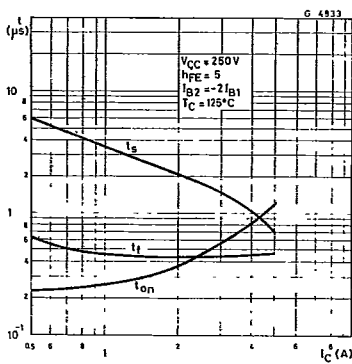
Base-emitter Saturation Voltage.



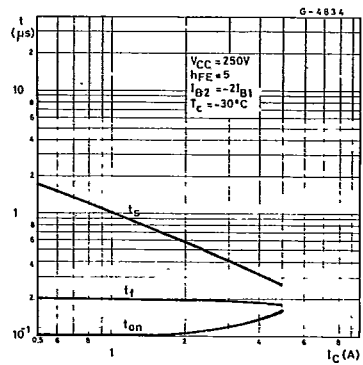
Saturated Switching Characteristics.



Saturated Switching Characteristics.



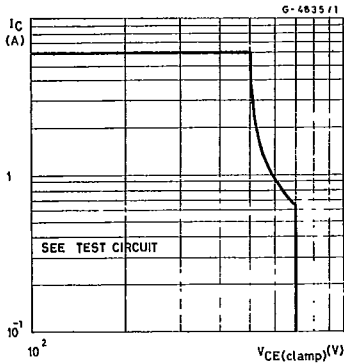
Saturated Switching Characteristics.



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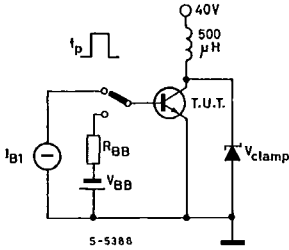
Clamped Reverse bias Safe Operating Areas.



Clamped $E_{s/b}$ Test Circuit.

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TEST CONDITIONS :

- $5V \geq |-V_{BB}| \geq 2V$
- $I_C / I_B \geq 4$
- $2I_{B1} \geq |-I_{B2}| \geq I_{B1}$
- $t_p =$ adjusted for normal I_C
- $R_{BB} =$ adjusted for I_{B2}