FDMS86581

MOSFET, N-Channel, POWERTRENCH®, 60 V, 30 A, 15 mΩ

ON Semiconductor®

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Features

- Typical $R_{DS(on)}$ = 12.5 mΩ at V_{GS} = 10 V, I_D = 30 A
- Typical $Q_{G(tot)}$ = 13 nC at V_{GS} = 10 V, I_D = 25 A
- UIS Capability
- RoHS Compliant

Applications

- DC–DC Power Supplies
- AC–DC Power Supplies
- Motor Control
- Load Switching

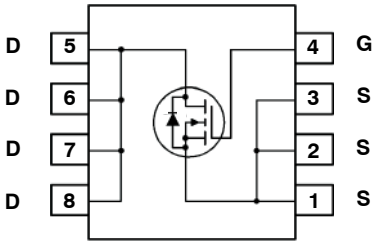
MOSFET MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain–to–Source Voltage	60	V
V_{GS}	Gate–to–Source Voltage	±20	V
I_D	Drain Current – Continuous (VGS = 10) T_C = 25°C (Note 1)	30	A
	Pulsed Drain Current, T_C = 25°C	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	13.5	mJ
P_D	Power Dissipation	50	W
	Derate Above 25°C	0.33	W/°C
T_J, T_{STG}	Operating and Storage Temperature	–55 to +175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	50	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by bondwire configuration.
2. Starting T_J = 25°C, L = 40 μH, I_{AS} = 26 A, V_{DD} = 60 V during inductor charging and V_{DD} = 0 V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2 oz copper.

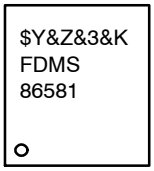
ELECTRICAL CONNECTION



N-Channel MOSFET

Power 56
(PQFN8 5x6)
CASE 483AE

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDMS86581	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Shipping†
FDMS86581	FDMS86581	Power 56	3000 Units/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions		Min	Typ.	Max.	Units
OFF CHARACTERISTICS							
B_{VDSS}	Drain−to−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V		60	–	–	V
I_{DSS}	Drain−to−Source Leakage Current	V_{DS} = 60 V, V_{GS} = 0 V	T_J = 25°C	–	–	1	A
			T_J = 175°C (Note 4)	–	–	1	mA
I_{GSS}	Gate−to−Source Leakage Current	V_{GS} = ± 20 V		–	–	±100	nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		2.0	2.7	4.0	V
$R_{DS(on)}$	Drain to Source On Resistance	I_D = 30 A, V_{GS} = 10 V	T_J = 25°C	–	12.5	15.0	mΩ
			T_J = 175°C (Note 4)	–	25.1	30.1	mΩ
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 30 V, V_{GS} = 0 V, f = 1 MHz		–	881	–	pF
C_{oss}	Output Capacitance			–	281	–	pF
C_{rss}	Reverse Transfer Capacitance			–	15	–	pF
R_G	Gate Resistance	f = 1 MHz		–	3.1	–	Ω
$Q_{g(ToT)}$	Total Gate Charge	V_{GS} = 0 to 10 V, V_{DD} = 30 V, I_D = 25 A		–	13	19	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 2 V, V_{DD} = 30 V, I_D = 25 A		–	2	–	nC
Q_{gs}	Gate−to−Source Gate Charge	V_{DD} = 30 V, I_D = 25 A		–	4	–	nC
Q_{gd}	Gate−to−Drain “Miller” Charge			–	3	–	nC
SWITCHING CHARACTERISTICS							
t_{on}	Turn−On Time	V_{DD} = 30 V, I_D = 30 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		–	–	20	ns
$t_{d(on)}$	Turn−On Delay			–	9	–	ns
t_r	Rise Time			–	5	–	ns
$t_{d(off)}$	Turn−Off Delay			–	15	–	ns
t_f	Fall Time			–	4	–	ns
t_{off}	Turn−Off Time			–	–	28	ns
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source−to−Drain Diode Voltage	I_{SD} = 30 A, V_{GS} = 0 V		–	–	1.25	V
		I_{SD} = 15 A, V_{GS} = 0 V		–	–	1.2	V
t_{rr}	Reverse−Recovery Time	I_F = 30 A, dI_{SD}/dt = 100 A/μs, V_{DD} = 48 V		–	37	55	ns
Q_{rr}	Reverse Recovery Charge			–	22	33	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

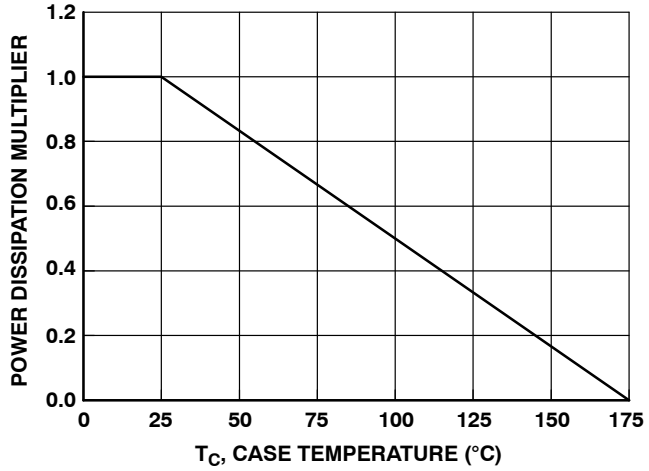


Figure 1. Normalized Power Dissipation vs. Case Temperature

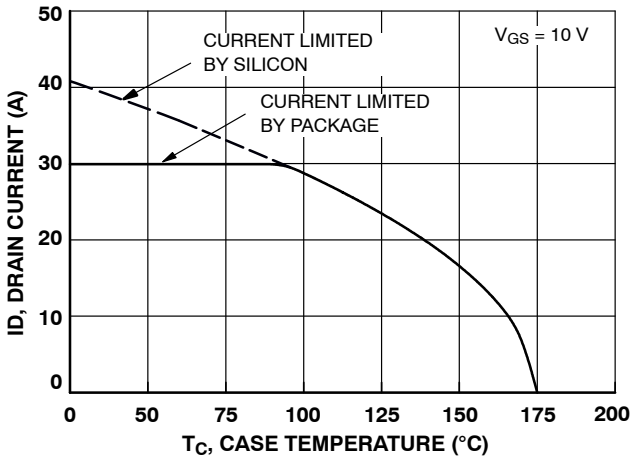


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

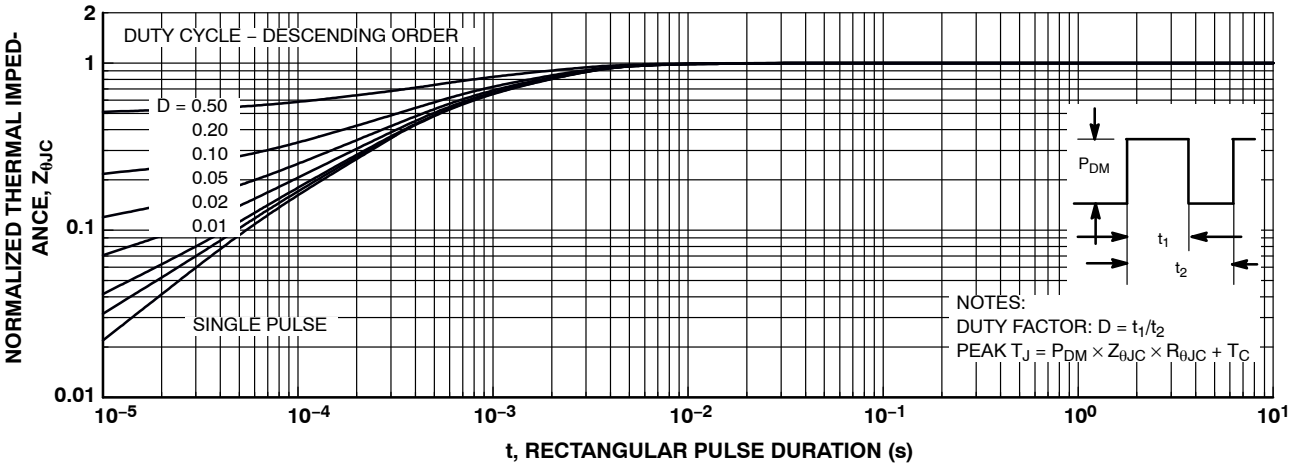


Figure 3. Normalized Maximum Transient Thermal Impedance

TYPICAL CHARACTERISTICS (continued)

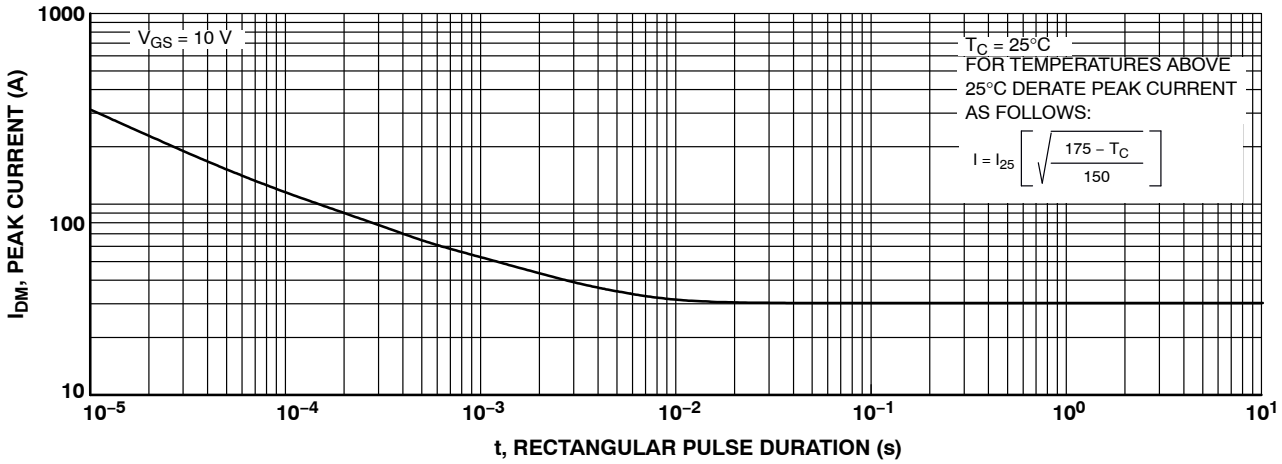


Figure 4. Peak Current Capability

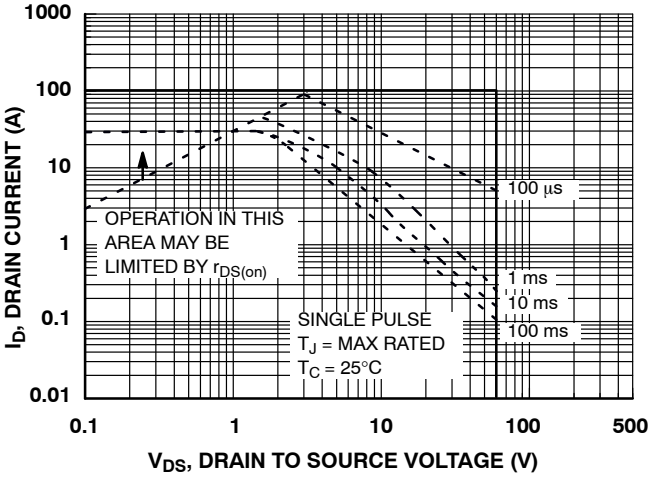
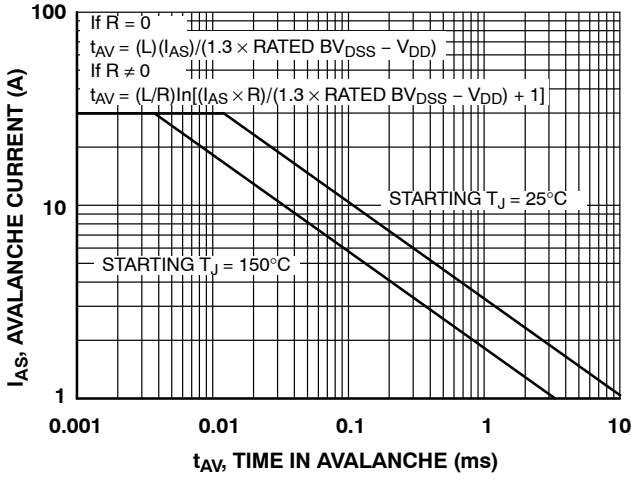


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515.

Figure 6. Unclamped Inductive Switching Capability

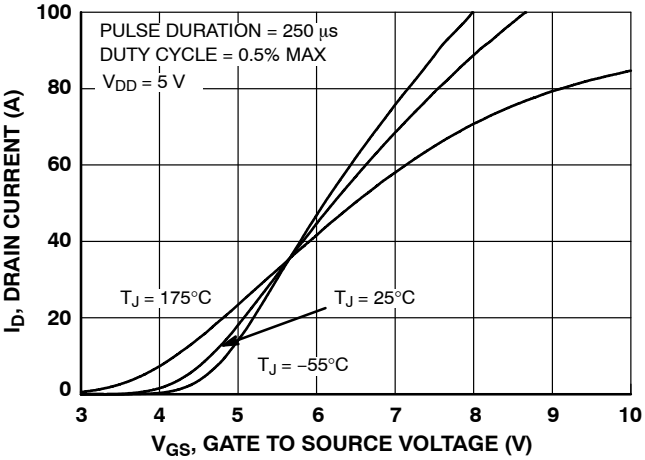


Figure 7. Transfer Characteristics

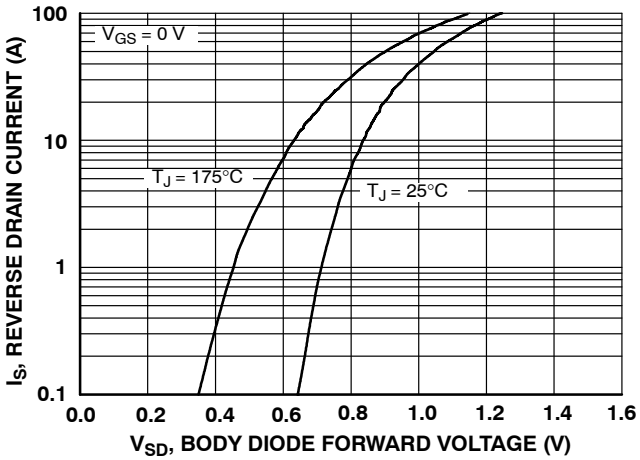


Figure 8. Forward Diode Characteristics

TYPICAL CHARACTERISTICS (continued)

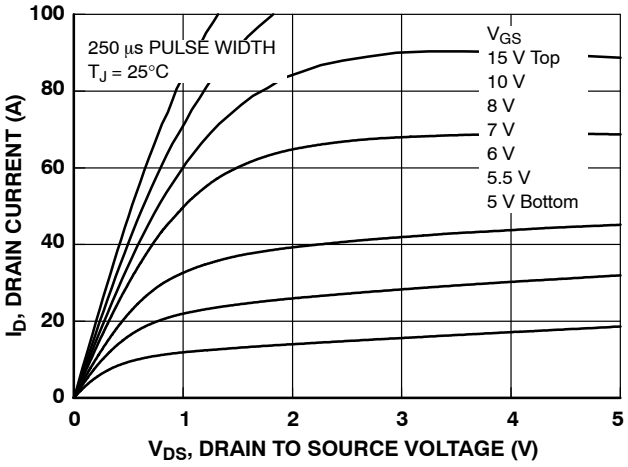


Figure 9. Saturation Characteristics

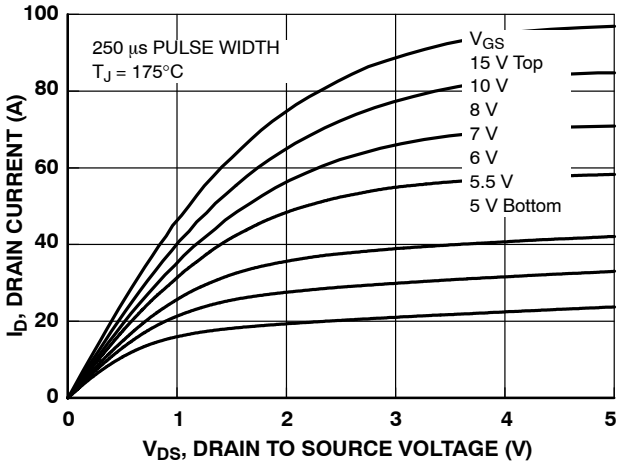


Figure 10. Saturation Characteristics

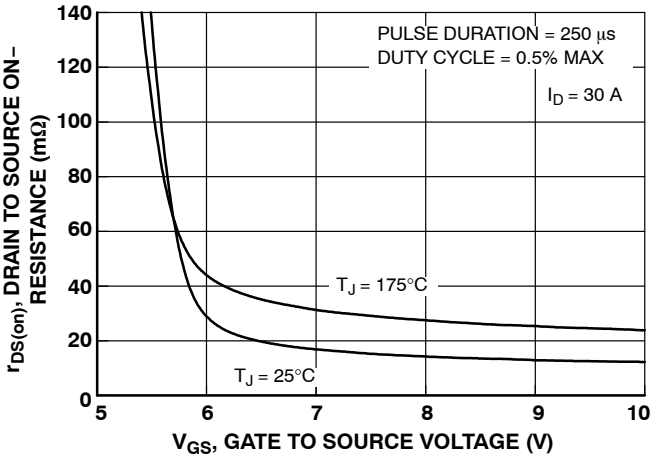


Figure 11. R_{DSON} vs. Gate Voltage

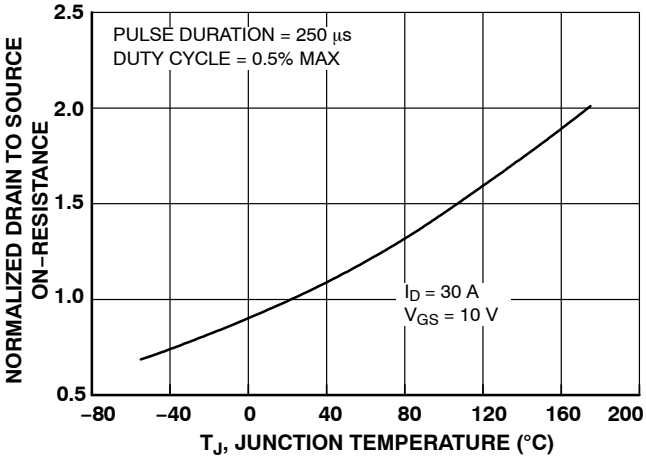


Figure 12. Normalized R_{DSON} vs. Junction Temperature

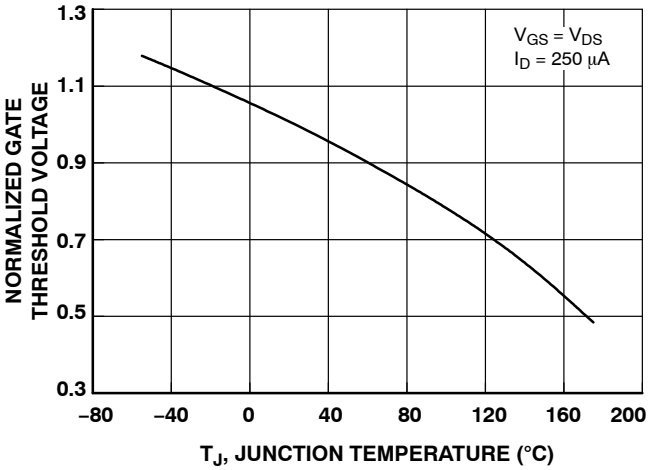


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

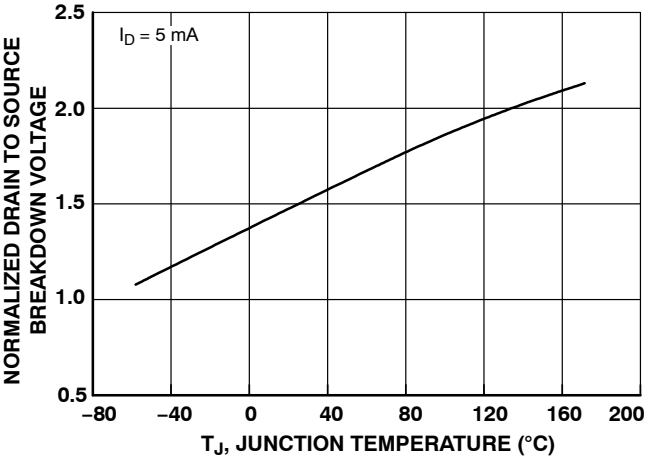


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

TYPICAL CHARACTERISTICS (continued)

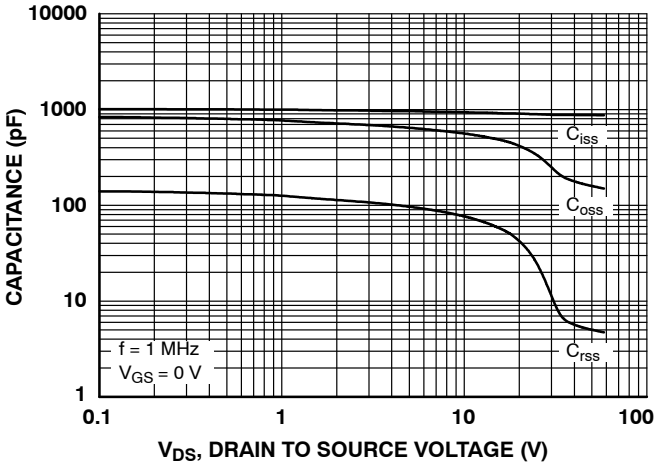


Figure 15. Capacitance vs. Drain to Source Voltage

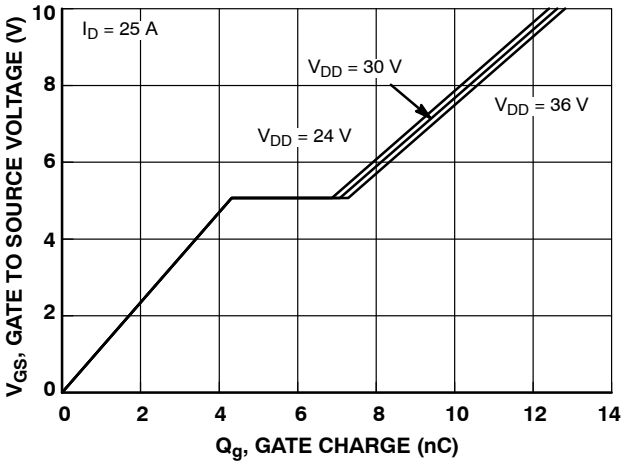
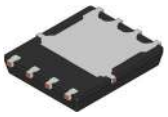


Figure 16. Gate Charge vs. Gate to Source Voltage

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



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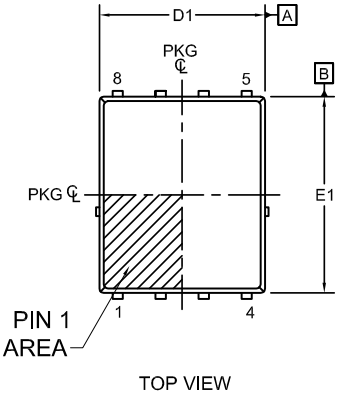
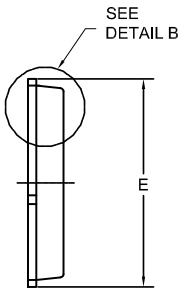
ISSUE C

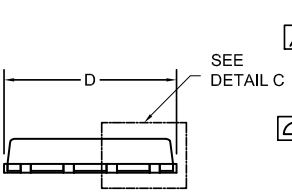
DATE 21 JAN 2022



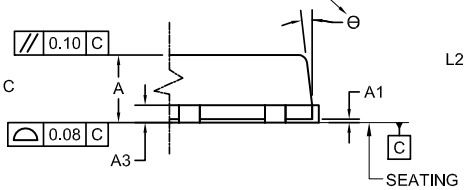
TOP VIEW



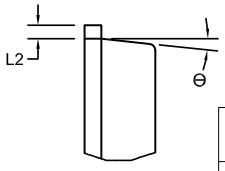
OPTIONAL DRAFT
ANGLE MAY APPEAR
ON FOUR SIDES
OF THE PACKAGE



SIDE VIEW



DETAIL C
SCALE: 2:1

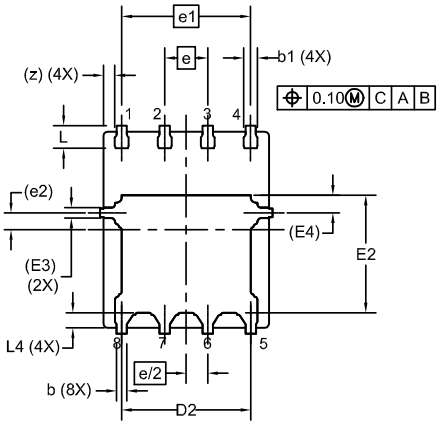


DETAIL B
SCALE: 2:1

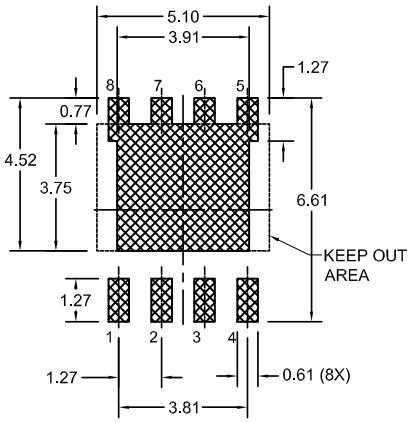
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
Θ	0°	-	12°



BOTTOM VIEW



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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