# 18-BIT, 1-MSPS, PSEUDO-BIPOLAR, FULLY DIFFERENTIAL INPUT, MICROPOWER SAMPLING ANALOG-TO-DIGITAL CONVERTER WITH PARALLEL INTERFACE, REFERENCE

## FEATURES

- **0 to 1-MHz Sample Rate**
- **±1.2 LSB Typ, ±2.5 LSB Max INL**
- **+0.75/-0.6 LSB Typ, +1.5/-1 LSB Max DNL**
- **18-Bit NMC Ensured Over Temperature**
- **±0.05-mV Offset Error**
- **±0.05-PPM/°C Offset Error Drift**
- **±0.035 %FSR Gain Error**
- **±0.5-PPM/°C Gain Error Drift**
- **99dB SNR, -121dB THD, 123dB SFDR**
- **Zero Latency**
- **Low Power: 225 mW at 1 MSPS**
- **Unipolar Differential Input Range: $V_{ref}$ to –Vref**
- **Onboard Reference with 6 PPM/°C Drift**
- **Onboard Reference Buffer**
- **High-Speed Parallel Interface**
- **Wide Digital Supply 2.7 V to 5.25 V**
- **8-/16-/18-Bit Bus Transfer**
- **48-Pin 7x7 QFN Package**

## APPLICATIONS

- **Medical Instruments**
- **Optical Networking**
- **Transducer Interface**
- **High Accuracy Data Acquisition Systems**
- **Magnetometers**

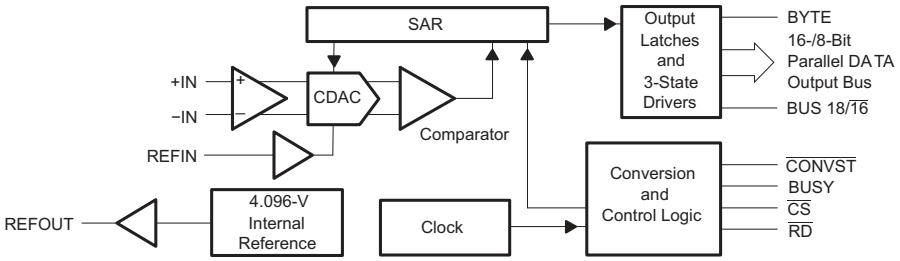
## DESCRIPTION

The ADS8482 is an 18-bit, 1-MSPS A/C converter with an internal 4.096-V reference and a pseudo-bipolar, fully differential input. The device includes a 18-bit capacitor-based SAR A/D converter with inherent sample and hold. The ADS8482 offers a full 18-bit interface, a 16-bit option where data is read using two read cycles, or an 8-bit bus option using three read cycles.

The ADS8482 is available in a 48-lead 7x7 QFN package and is characterized over the industrial –40°C to 85°C temperature range.

### HIGH SPEED SAR CONVERTER FAMILY

| TYPE/SPEED | 500 kHz | ~600 kHz | 750 kHz | 1 MHz | 1.25 MHz | 2 MHz | 3 MHz | 4MHz |
|---|---|---|---|---|---|---|---|---|
| 18-Bit Pseudo-Diff | ADS8383 | ADS8381 | | ADS8481 | | | | |
| | | ADS8380 (s) | | | | | | |
| 18-Bit Pseudo-Bipolar, Fully Diff | | ADS8382 (s) | | ADS8482 | | | | |
| 16-Bit Pseudo-Diff | ADS8327 | ADS8370 (s) | ADS8371 | ADS8471 | ADS8401 | ADS8411 | | |
| | ADS8328 | ADS8372 (s) | | | ADS8405 | ADS8410 (s) | | |
| 16-Bit Pseudo-Bipolar, Fully Diff | | | | ADS8472 | ADS8402 | ADS8412 | | ADS8422 |
| | | | | | ADS8406 | ADS8413 (s) | | |
| 14-Bit Pseudo-Diff | | | | | ADS7890 (s) | | ADS7891 | |
| 12-Bit Pseudo-Diff | | | | ADS7886 | | ADS7883 | | ADS7881 |




Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION(1)

| MODEL | MAXIMUM INTEGRAL LINEARITY (LSB) | MAXIMUM DIFFERENTIAL LINEARITY (LSB) | NO MISSING CODES RESOLUTION (BIT) | PACKAGE TYPE | PACKAGE DESIGNATOR | TEMPER-ATURE RANGE | ORDERING INFORMATION | TRANS-PORT MEDIA QTY. |
|---|---|---|---|---|---|---|---|---|
| ADS8482I | ±4 | –1 to +1.5 | 18 | 7x7 48 Pin QFN | RGZ | –40°C to 85°C | ADS8482IRGZT | Tape and reel 250 |
| | | | | | | | ADS8482IRGZR | Tape and reel 1000 |
| ADS8482IB | ±2.5 | –1 to +1.5 | 18 | 7x7 48 Pin QFN | RGZ | –40°C to 85°C | ADS8482IBRGZT | Tape and reel 250 |
| | | | | | | | ADS8482IBRGZR | Tape and reel 1000 |

(1) For the most current specifications and package information, refer to our website at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | | VALUE | UNIT |
|---|---|---|---|---|
| | Voltage | +IN to AGND | –0.4 to +VA + 0.1 | V |
| | | –IN to AGND | –0.4 to +VA + 0.1 | V |
| | | +VA to AGND | –0.3 to 7 | V |
| | | +VBD to BDGND | –0.3 to 7 | V |
| | | +VA to +VBD | –0.3 to 2.55 | V |
| | Digital input voltage to BDGND | | –0.3 to +VBD + 0.3 | V |
| | Digital output voltage to BDGND | | –0.3 to +VBD + 0.3 | V |
| $T_A$ | Operating free-air temperature range | | –40 to 85 | °C |
| $T_{stg}$ | Storage temperature range | | –65 to 150 | °C |
| | Junction temperature ($T_J$ max) | | 150 | °C |
| | QFN package | Power dissipation | $(T_J Max – T_A)/\theta_{JA}$ | |
| | | $\theta_{JA}$ thermal impedance | 22 | °C/W |
| | Lead temperature, soldering | Vapor phase (60 sec) | 215 | °C |
| | | Infrared (15 sec) | 220 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## SPECIFICATIONS

$T_A$ = –40°C to 85°C, +VA = 5 V, +VBD = 3 V or 5 V, $V_{ref}$ = 4.096 V, $f_{SAMPLE}$ = 1 MSPS (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ANALOG INPUT** | | | | | | |
| Full-scale input voltage(1) | | +IN – (–IN) | $–V_{ref}$ | | $V_{ref}$ | V |
| Absolute input voltage | | +IN | –0.2 | | $V_{ref}$ + 0.2 | V |
| | | –IN | –0.2 | | $V_{ref}$ + 0.2 | |
| Common-mode input range | | | $(V_{ref})/2$ – 0.2 | $(V_{ref})/2$ | $(V_{ref})/2$ + 0.2 | V |
| Input capacitance | | | | 65 | | pF |
| Input leakage current | | | | 1 | | nA |
| **SYSTEM PERFORMANCE** | | | | | | |
| Resolution | | | | 18 | | Bits |
| No missing codes | ADS8482I | | 18 | | | Bits |
| | ADS8482IB | | 18 | | | |
| Integral linearity (2) | ADS8482I | | –4 | ±1.2 | 4 | LSB (18 bit)(3) |
| | ADS8482IB | | –2.5 | ±1.2 | 2.5 | |
| Differential linearity | ADS8482I | | –1 | –0.6/0.75 | 1.5 | LSB (18 bit) |
| | ADS8482IB | | –1 | –0.6/0.75 | 1.5 | |
| Offset error(4) | ADS8482I | | –0.5 | ±0.05 | 0.5 | mV |
| | ADS8482IB | | –0.5 | ±0.05 | 0.5 | |
| Offset error temperature drift | ADS8482I | | | ±0.05 | | ppm/°C |
| | ADS8482IB | | | ±0.05 | | |
| Gain error(4)(5) | ADS8482I | $V_{ref}$ = 4.096 V | –0.1 | ±0.035 | 0.1 | %FS |
| | ADS8482IB | $V_{ref}$ = 4.096 V | –0.1 | ±0.035 | 0.1 | %FS |
| Gain error temperature drift | ADS8482I | | | ±0.5 | | ppm/°C |
| | ADS8482IB | | | ±0.5 | | |
| Common-mode rejection ratio | | At dc (±0.2 V around $V_{ref}$/2) | | 60 | | dB |
| | | +IN – (–IN) = 1 Vpp at 1 MHz | | 55 | | |
| Noise | | | | 25 | | µV RMS |
| Power supply rejection ratio | | At 1FFFFh output code | | 60 | | dB |
| **SAMPLING DYNAMICS** | | | | | | |
| Conversion time | | | | 625 | 650 | ns |
| Acquisition time | | | 320 | 350 | | ns |
| Throughput rate | | | | | 1 | MHz |
| Aperture delay | | | | 4 | | ns |
| Aperture jitter | | | | 5 | | ps |
| Step response | | | | 150 | | ns |
| Over voltage recovery | | | | 150 | | ns |

(1) Ideal input span, does not include gain or offset error.
(2) This is endpoint INL, not best fit.
(3) LSB means least significant bit
(4) Measured relative to an ideal full-scale input [+IN – (–IN)] of 8.192 V
(5) This specification does not include the internal reference voltage error and drift.

## SPECIFICATIONS (Continued)

$T_A$ = –40°C to 85°C, +VA = 5 V, +VBD = 3 V or 5 V, $V_{ref}$ = 4.096 V, $f_{SAMPLE}$ = 1 MSPS (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Total harmonic distortion (THD)(1) | ADS8482I | $V_{IN}$ = 8 $V_{pp}$ at 2 kHz | | –120 | | dB |
| | ADS8482IB | | | –121 | | |
| | ADS8482I | $V_{IN}$ = 8 $V_{pp}$ at 20 kHz | | –105 | | |
| | ADS8482IB | | | –110 | | |
| | ADS8482I | $V_{IN}$ = 8 $V_{pp}$ at 100 kHz | | –100 | | |
| | ADS8482IB | | | –103 | | |
| Signal to noise ratio (SNR)(1) | ADS8482I | $V_{IN}$ = 8 $V_{pp}$ at 2 kHz | 96 | 98.6 | | dB |
| | ADS8482IB | | 97.5 | 99 | | |
| | ADS8482I | $V_{IN}$ = 8 $V_{pp}$ at 20 kHz | | 98 | | |
| | ADS8482IB | | | 98.5 | | |
| | ADS8482I | $V_{IN}$ = 8 $V_{pp}$ at 100 kHz | | 95 | | |
| | ADS8482IB | | | 97 | | |
| Signal to noise + distortion (SINAD)(1) | ADS8482I | $V_{IN}$ = 8 $V_{pp}$ at 2 kHz | 96 | 98.5 | | dB |
| | ADS8482IB | | 97.5 | 99 | | |
| | ADS8482I | $V_{IN}$ = 8 $V_{pp}$ at 20 kHz | | 97 | | |
| | ADS8482IB | | | 98 | | |
| | ADS8482I | $V_{IN}$ = 8 $V_{pp}$ at 100 kHz | | 93 | | |
| | ADS8482IB | | | 95 | | |
| Spurious free dynamic range (SFDR)(1) | ADS8482I | $V_{IN}$ = 8 $V_{pp}$ at 2 kHz | | 120 | | dB |
| | ADS8482IB | | | 123 | | |
| | ADS8482I | $V_{IN}$ = 8 $V_{pp}$ at 20 kHz | | 107 | | |
| | ADS8482IB | | | 113 | | |
| | ADS8482I | $V_{IN}$ = 8 $V_{pp}$ at 100 kHz | | 102 | | |
| | ADS8482IB | | | 105 | | |
| –3dB Small signal bandwidth | | | | 15 | | MHz |

(1) Calculated on the first nine harmonics of the input frequency.

## SPECIFICATIONS (Continued)

$T_A$ = –40°C to 85°C, +VA = 5 V, +VBD = 3 V or 5 V, $V_{ref}$ = 4.096 V, $f_{SAMPLE}$ = 1 MSPS (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **VOLTAGE REFERENCE INPUT** | | | | | | |
| Reference voltage at REFIN, $V_{ref}$ | | | 3.0 | 4.096 | +VA – 0.8 | V |
| Reference resistance(1) | | | | 500 | | kΩ |
| Reference current drain | | $f_s$ = 1 MHz | | | 1 | mA |
| **INTERNAL REFERENCE OUTPUT** | | | | | | |
| Internal reference start-up time | | From 95% (+VA), with 1-µF storage capacitor | | | 120 | ms |
| Reference voltage range, $V_{ref}$ | | $I_O$ = 0 | 4.081 | 4.096 | 4.111 | V |
| Source current | | Static load | | | 10 | µA |
| Line regulation | | +VA = 4.75 V ~ 5.25 V | | 60 | | µV |
| Drift | | $I_O$ = 0 | | ±6 | | PPM/°C |
| **DIGITAL INPUT/OUTPUT** | | | | | | |
| Logic family –CMOS | | | | | | |
| Logic level | $V_{IH}$ | $I_{IH}$ = 5 µA | +VBD – 1 | | +VBD + 0.3 | V |
| | $V_{IL}$ | $I_{IL}$ = 5 µA | –0.3 | | 0.8 | |
| | $V_{OH}$ | $I_{OH}$ = 2 TTL loads | +VBD – 0.6 | | | |
| | $V_{OL}$ | $I_{OL}$ = 2 TTL loads | | | | |
| Data format – Straight Binary | | | | | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | |
| Power supply voltage | +VBD | | 2.7 | 3.3 | 5.25 | V |
| | +VA | | 4.75 | 5 | 5.25 | V |
| Supply current(2) | | $f_s$ = 1 MHz | | 45 | 50 | mA |
| Power dissipation(2) | | $f_s$ = 1 MHz | | 225 | 250 | mW |
| **TEMPERATURE RANGE** | | | | | | |
| Operating free-air | | | –40 | | 85 | °C |

(1) Can vary ±20%
(2) This includes only +VA current. +VBD current is typical 1 mA with 5 pF load capacitance on all output pins.

## TIMING CHARACTERISTICS

All specifications typical at –40°C to 85°C, +VA =+VBD = 5 V (1)(2)(3)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{(CONV)}$ | Conversion time | | | 650 | ns |
| $t_{(ACQ)}$ | Acquisition time | 320 | | | ns |
| $t_{(HOLD)}$ | Sample capacitor hold time | | | 25 | ns |
| $t_{pd1}$ | $\overline{CONVST}$ low to BUSY high | | | 40 | ns |
| $t_{pd2}$ | Propagation delay time, end of conversion to BUSY low | | | 15 | ns |
| $t_{pd3}$ | Propagation delay time, start of convert state to rising edge of BUSY | | | 15 | ns |
| $t_{w1}$ | Pulse duration, $\overline{CONVST}$ low | 40 | | | ns |
| $t_{su1}$ | Setup time, $\overline{CS}$ low to $\overline{CONVST}$ low | 20 | | | ns |
| $t_{w2}$ | Pulse duration, $\overline{CONVST}$ high | 20 | | | ns |
| | $\overline{CONVST}$ falling edge jitter | | | 10 | ps |
| $t_{w3}$ | Pulse duration, BUSY signal low | $t_{(ACQ)}$min | | | ns |
| $t_{w4}$ | Pulse duration, BUSY signal high | | | 650 | ns |
| $t_{h1}$ | Hold time, first data bus transition ($\overline{RD}$ low, or $\overline{CS}$ low for read cycle, or BYTE or BUS18/$\overline{16}$ input changes) after $\overline{CONVST}$ low | 40 | | | ns |
| $t_{d1}$ | Delay time, $\overline{CS}$ low to $\overline{RD}$ low | 0 | | | ns |
| $t_{su2}$ | Setup time, $\overline{RD}$ high to $\overline{CS}$ high | 0 | | | ns |
| $t_{w5}$ | Pulse duration, $\overline{RD}$ low | 50 | | | ns |
| $t_{en}$ | Enable time, $\overline{RD}$ low (or $\overline{CS}$ low for read cycle) to data valid | | | 20 | ns |
| $t_{d2}$ | Delay time, data hold from $\overline{RD}$ high | 5 | | | ns |
| $t_{d3}$ | Delay time, BUS18/$\overline{16}$ or BYTE rising edge or falling edge to data valid | 10 | | 20 | ns |
| $t_{w6}$ | Pulse duration, $\overline{RD}$ high | 20 | | | ns |
| $t_{w7}$ | Pulse duration, $\overline{CS}$ high | 20 | | | ns |
| $t_{h2}$ | Hold time, last $\overline{RD}$ (or $\overline{CS}$ for read cycle ) rising edge to $\overline{CONVST}$ falling edge | 50 | | | ns |
| $t_{pd4}$ | Propagation delay time, BUSY falling edge to next $\overline{RD}$ (or $\overline{CS}$ for read cycle) falling edge | 0 | | | ns |
| $t_{d4}$ | Delay time, BYTE edge to BUS18/$\overline{16}$ edge skew | 0 | | | ns |
| $t_{su3}$ | Setup time, BYTE or BUS18/$\overline{16}$ transition to $\overline{RD}$ falling edge | 10 | | | ns |
| $t_{h3}$ | Hold time, BYTE or BUS18/$\overline{16}$ transition to $\overline{RD}$ falling edge | 10 | | | ns |
| $t_{dis}$ | Disable time, $\overline{RD}$ high ($\overline{CS}$ high for read cycle) to 3-stated data bus | | | 20 | ns |
| $t_{d5}$ | Delay time, BUSY low to MSB data valid delay | | | 0 | ns |
| $t_{d6}$ | Delay time, $\overline{CS}$ rising edge to BUSY falling edge | 50 | | | ns |
| $t_{d7}$ | Delay time, BUSY falling edge to $\overline{CS}$ rising edge | 50 | | | ns |
| $t_{su5}$ | BYTE transition setup time, from BYTE transition to next BYTE transition, or BUS18/$\overline{16}$ transition setup time, from BUS18/$\overline{16}$ to next BUS18/$\overline{16}$. | 50 | | | ns |
| $t_{su(ABORT)}$ | Setup time from the falling edge of $\overline{CONVST}$ (used to start the valid conversion) to the next falling edge of $\overline{CONVST}$ (when CS = 0 and $\overline{CONVST}$ are used to abort) or to the next falling edge of $\overline{CS}$ (when $\overline{CS}$ is used to abort). | 60 | | 550 | ns |

(1) All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +VBD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See timing diagrams.
(3) All timing are measured with 20 pF equivalent loads on all data bits and BUSY pins.

## TIMING CHARACTERISTICS

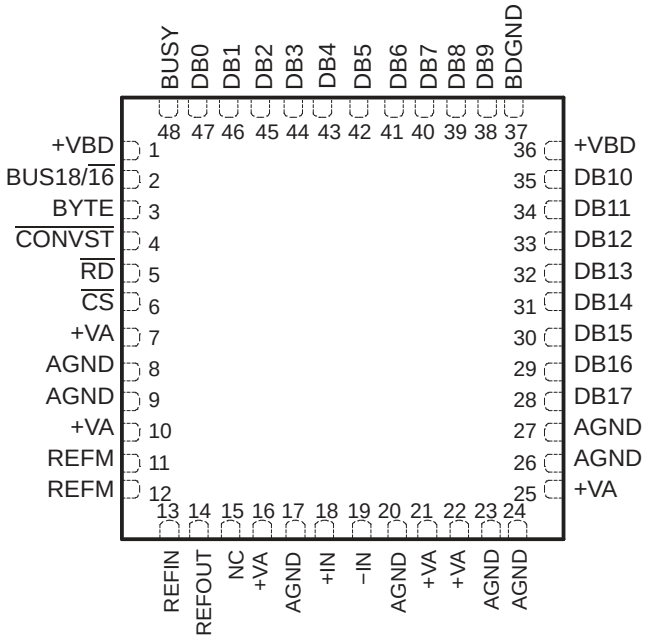
All specifications typical at –40°C to 85°C, +VA = 5 V +VBD = 3 V (1)(2)(3)

| | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{(CONV)}$ | Conversion time | | | 650 | ns |
| $t_{(ACQ)}$ | Acquisition time | 310 | | | ns |
| $t_{(HOLD)}$ | Sample capacitor hold time | | | 25 | ns |
| $t_{pd1}$ | $\overline{CONVST}$ low to BUSY high | | | 40 | ns |
| $t_{pd2}$ | Propagation delay time, end of conversion to BUSY low | | | 25 | ns |
| $t_{pd3}$ | Propagation delay time, start of convert state to rising edge of BUSY | | | 25 | ns |
| $t_{w1}$ | Pulse duration, $\overline{CONVST}$ low | 40 | | | ns |
| $t_{su1}$ | Setup time, $\overline{CS}$ low to $\overline{CONVST}$ low | 20 | | | ns |
| $t_{w2}$ | Pulse duration, CONVST high | 20 | | | ns |
| | $\overline{CONVST}$ falling edge jitter | | | 10 | ps |
| $t_{w3}$ | Pulse duration, BUSY signal low | $t_{(ACQ)}$min | | | ns |
| $t_{w4}$ | Pulse duration, BUSY signal high | | | 650 | ns |
| $t_{h1}$ | Hold time, first data bus transition ($\overline{RD}$ low, or $\overline{CS}$ low for read cycle, or BYTE or BUS18/$\overline{16}$ input changes) after $\overline{CONVST}$ low | 40 | | | ns |
| $t_{d1}$ | Delay time, $\overline{CS}$ low to $\overline{RD}$ low | 0 | | | ns |
| $t_{su2}$ | Setup time, $\overline{RD}$ high to $\overline{CS}$ high | 0 | | | ns |
| $t_{w5}$ | Pulse duration, $\overline{RD}$ low | 50 | | | ns |
| $t_{en}$ | Enable time, $\overline{RD}$ low (or $\overline{CS}$ low for read cycle) to data valid | | | 30 | ns |
| $t_{d2}$ | Delay time, data hold from $\overline{RD}$ high | 5 | | | ns |
| $t_{d3}$ | Delay time, BUS18/$\overline{16}$ or BYTE rising edge or falling edge to data valid | 10 | | 30 | ns |
| $t_{w6}$ | Pulse duration, $\overline{RD}$ high | 20 | | | ns |
| $t_{w7}$ | Pulse duration, $\overline{CS}$ high | 20 | | | ns |
| $t_{h2}$ | Hold time, last $\overline{RD}$ (or $\overline{CS}$ for read cycle ) rising edge to $\overline{CONVST}$ falling edge | 50 | | | ns |
| $t_{pd4}$ | Propagation delay time, BUSY falling edge to next $\overline{RD}$ (or $\overline{CS}$ for read cycle) falling edge | 0 | | | ns |
| $t_{d4}$ | Delay time, BYTE edge to BUS18/$\overline{16}$ edge skew | 0 | | | ns |
| $t_{su3}$ | Setup time, BYTE or BUS18/$\overline{16}$ transition to $\overline{RD}$ falling edge | 10 | | | ns |
| $t_{h3}$ | Hold time, BYTE or BUS18/$\overline{16}$ transition to $\overline{RD}$ falling edge | 10 | | | ns |
| $t_{dis}$ | Disable time, $\overline{RD}$ high ($\overline{CS}$ high for read cycle) to 3-stated data bus | | | 30 | ns |
| $t_{d5}$ | Delay time, BUSY low to MSB data valid delay | | | 0 | ns |
| $t_{d6}$ | Delay time, $\overline{CS}$ rising edge to BUSY falling edge | 50 | | | ns |
| $t_{d7}$ | Delay time, BUSY falling edge to $\overline{CS}$ rising edge | 50 | | | ns |
| $t_{su5}$ | BYTE transition setup time, from BYTE transition to next BYTE transition, or BUS18/$\overline{16}$ transition setup time, from BUS18/$\overline{16}$ to next BUS18/$\overline{16}$. | 50 | | | ns |
| $t_{su(ABORT)}$ | Setup time from the falling edge of $\overline{CONVST}$ (used to start the valid conversion) to the next falling edge of $\overline{CONVST}$ (when CS = 0 and $\overline{CONVST}$ are used to abort) or to the next falling edge of $\overline{CS}$ (when $\overline{CS}$ is used to abort). | 70 | | 550 | ns |

(1) All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +VBD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See timing diagrams.
(3) All timing are measured with 20 pF equivalent loads on all data bits and BUSY pins.

## PIN ASSIGNMENTS

**RGZ PACKAGE**
**(TOP VIEW)**




NC − No internal connection

NOTE: The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

## TERMINAL FUNCTIONS

| NAME | NO | I/O | DESCRIPTION |
|---|---|---|---|
| AGND | 8, 9, 17, 20, 23, 24, 26, 27 | – | Analog ground |
| BDGND | 37 | – | Digital ground for bus interface digital supply |
| BUSY | 48 | O | Status output. High when a conversion is in progress. |
| BUS18/$\overline{16}$ | 2 | I | Bus size select input. Used for selecting 18-bit or 16-bit wide bus transfer.<br>0: Data bits output on the 18-bit data bus pins DB[17:0].<br>1: Last two data bits D[1:0] from 18-bit wide bus output on:<br>a) the low byte pins DB[9:2] if BYTE = 0<br>b) the high byte pins DB[17:10] if BYTE = 1 |
| BYTE | 3 | I | Byte select input. Used for 8-bit bus reading.<br>0: No fold back<br>1: Low byte D[9:2] of the 16 most significant bits is folded back to high byte of the 16 most significant pins DB[17:10]. |
| $\overline{\text{CONVST}}$ | 4 | I | Convert start. The falling edge of this input ends the acquisition period and starts the hold period. |
| $\overline{\text{CS}}$ | 6 | I | Chip select. The falling edge of this input starts the acquisition period. |

| Data Bus | | | 8-BIT BUS | | | 16-BIT BUS | | 18-BIT BUS |
|---|---|---|---|---|---|---|---|---|
| | | | BYTE = 0 | BYTE = 1 | BYTE = 1 | BYTE = 0 | BYTE = 0 | BYTE = 0 |
| | | | BUS18/$\overline{16}$ = 0 | BUS18/$\overline{16}$ = 0 | BUS18/$\overline{16}$ = 1 | BUS18/$\overline{16}$ = 0 | BUS18/$\overline{16}$ = 1 | BUS18/$\overline{16}$ = 0 |
| DB17 | 28 | O | D17 (MSB) | D9 | All ones | D17 (MSB) | All ones | D17 (MSB) |
| DB16 | 29 | O | D16 | D8 | All ones | D16 | All ones | D16 |
| DB15 | 30 | O | D15 | D7 | All ones | D15 | All ones | D15 |
| DB14 | 31 | O | D14 | D6 | All ones | D14 | All ones | D14 |
| DB13 | 32 | O | D13 | D5 | All ones | D13 | All ones | D13 |
| DB12 | 33 | O | D12 | D4 | All ones | D12 | All ones | D12 |
| DB11 | 34 | O | D11 | D3 | D1 | D11 | All ones | D11 |
| DB10 | 35 | O | D10 | D2 | D0 (LSB) | D10 | All ones | D10 |
| DB9 | 38 | O | D9 | All ones | All ones | D9 | All ones | D9 |

## TERMINAL FUNCTIONS (continued)

| NAME | NO | I/O | DESCRIPTION | | | | | |
|---|---|---|---|---|---|---|---|---|
| DB8 | 39 | O | D8 | All ones | All ones | D8 | All ones | D8 |
| DB7 | 40 | O | D7 | All ones | All ones | D7 | All ones | D7 |
| DB6 | 41 | O | D6 | All ones | All ones | D6 | All ones | D6 |
| DB5 | 42 | O | D5 | All ones | All ones | D5 | All ones | D5 |
| DB4 | 43 | O | D4 | All ones | All ones | D4 | All ones | D4 |
| DB3 | 44 | O | D3 | All ones | All ones | D3 | D1 | D3 |
| DB2 | 45 | O | D2 | All ones | All ones | D2 | D0 (LSB) | D2 |
| DB1 | 46 | O | D1 | All ones | All ones | D1 | All ones | D1 |
| DB0 | 47 | O | D0 (LSB) | All ones | All ones | D0 (LSB) | All ones | D0 (LSB) |
| | | | | | | | | |
| –IN | 19 | I | Inverting input channel | | | | | |
| +IN | 18 | I | Noninverting input channel | | | | | |
| NC | 15 | | No connection | | | | | |
| REFIN | 13 | I | Reference input | | | | | |
| REFOUT | 14 | O | Reference output. Add 1-µF capacitor between the REFOUT pin and REFM pin when internal reference is used. | | | | | |
| REFM | 11, 12 | I | Reference ground | | | | | |
| $\overline{RD}$ | 5 | I | Synchronization pulse for the parallel output. When $\overline{CS}$ is low, this serves as output enable and puts the previous conversion results on the bus. | | | | | |
| +VA | 7, 10, 16, 21, 22, 25 | – | Analog power supplies, 5-V DC | | | | | |
| +VBD | 1, 36 | – | Digital power supply for bus | | | | | |

## TYPICAL CHARACTERISTICS

**DC HISTOGRAM**
**(8192 Conversion Outputs)**

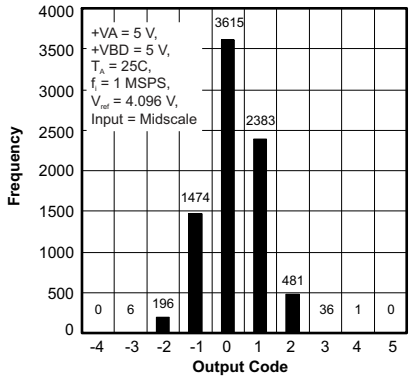



**Figure 1.**

**INTERNAL REFERENCE VOLTAGE**
**vs**
**FREE-AIR TEMPERATURE**

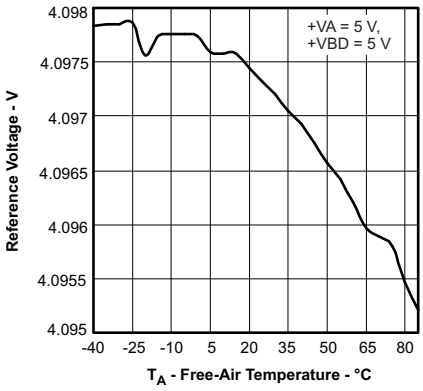



**Figure 2.**

**INTERNAL REFERENCE VOLTAGE**
**vs**
**SUPPLY VOLTAGE**

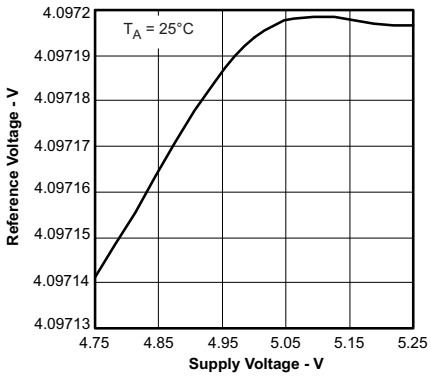



**Figure 3.**

## TYPICAL CHARACTERISTICS (continued)

**SUPPLY CURRENT vs FREE-AIR TEMPERATURE**

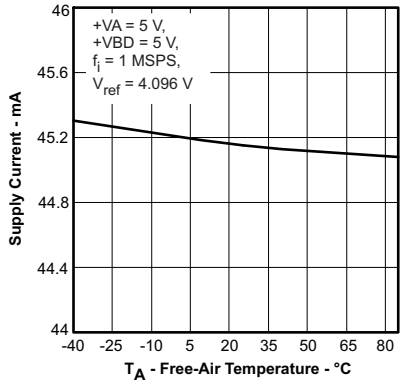



Figure 4.

**SUPPLY CURRENT vs SUPPLY VOLTAGE**

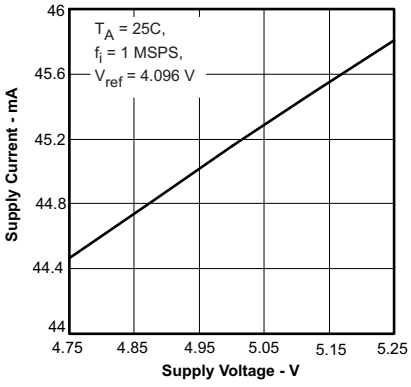



Figure 5.

**SUPPLY CURRENT vs SAMPLE RATE**

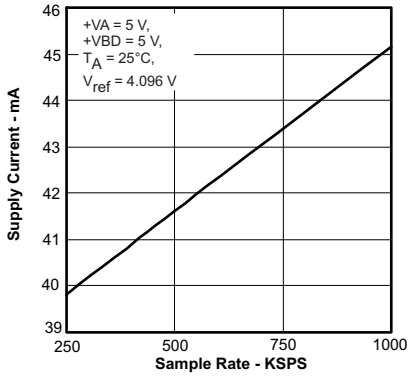



Figure 6.

**DIFFERENTIAL NONLINEARITY vs FREE-AIR TEMPERATURE**

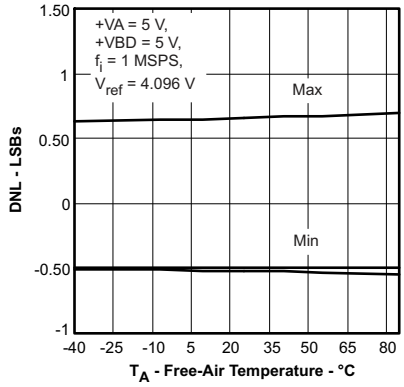



Figure 7.

**INTEGRAL NONLINEARITY vs FREE-AIR TEMPERATURE**

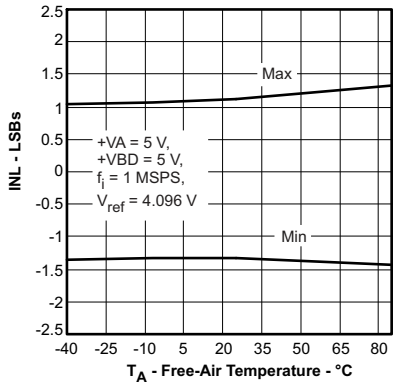



Figure 8.

**DIFFERENTIAL NONLINEARITY vs SUPPLY VOLTAGE**

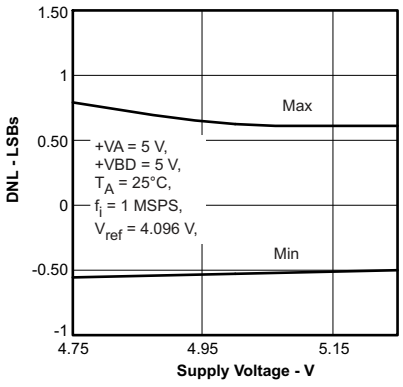



Figure 9.

**INTEGRAL NONLINEARITY vs SUPPLY VOLTAGE**

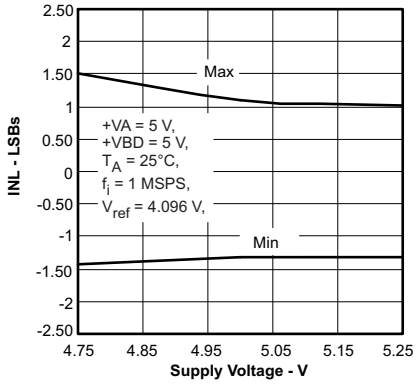



Figure 10.

**DIFFERENTIAL NONLINEARITY vs REFERENCE VOLTAGE**

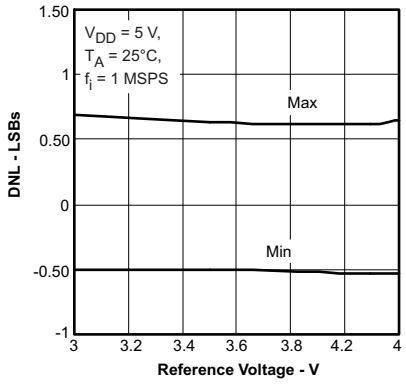



Figure 11.

**INTEGRAL NONLINEARITY vs REFERENCE VOLTAGE**

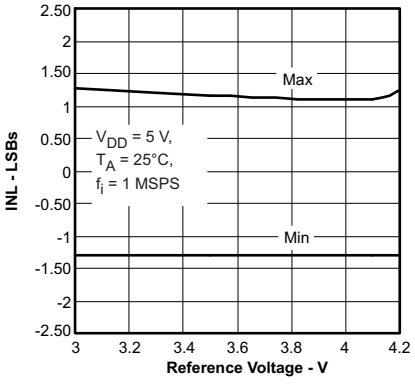



Figure 12.

## TYPICAL CHARACTERISTICS (continued)

**OFFSET ERROR vs FREE-AIR TEMPERATURE**

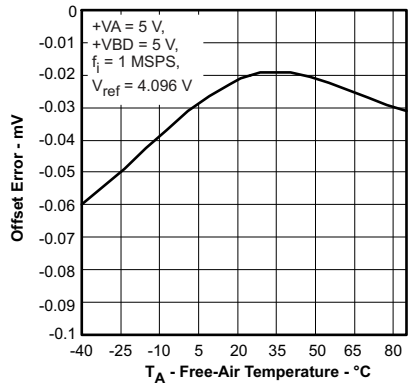



Figure 13.

**OFFSET ERROR vs SUPPLY VOLTAGE**

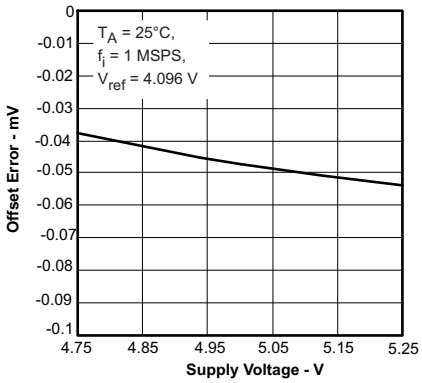



Figure 14.

**OFFSET ERROR vs REFERENCE VOLTAGE**

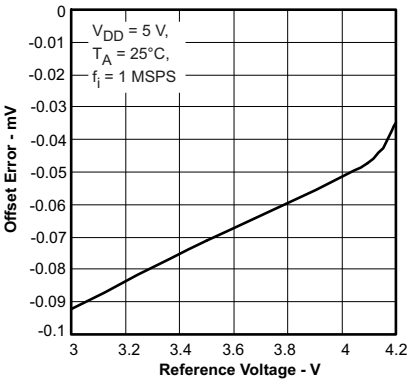



Figure 15.

**GAIN ERROR vs SUPPLY VOLTAGE**

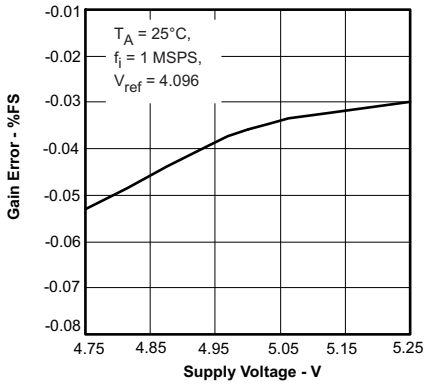



Figure 16.

**GAIN ERROR vs FREE-AIR TEMPERATURE**

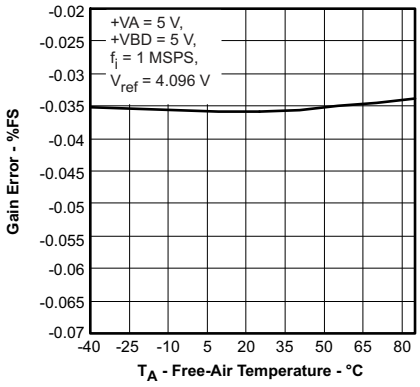



Figure 17.

**GAIN ERROR vs REFERENCE VOLTAGE**

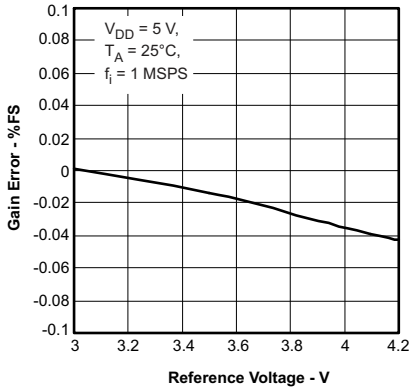



Figure 18.

**OFFSET ERROR TEMPERATURE DRIFT DISTRIBUTION (35 Samples)**

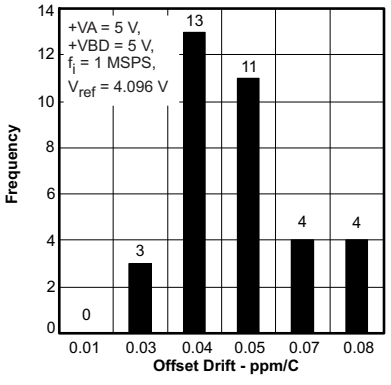



Figure 19.

**GAIN ERROR TEMPERATURE DRIFT DISTRIBUTION (35 Samples)**

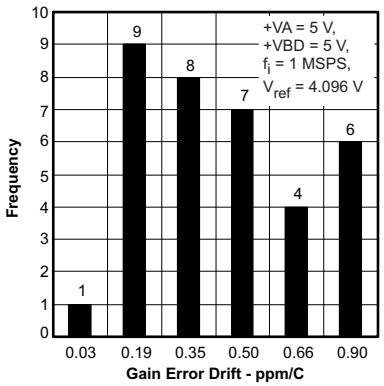



Figure 20.

**TOTAL HARMONIC DISTORTION vs REFERENCE VOLTAGE**

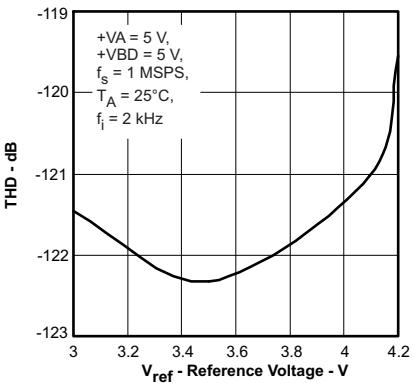



Figure 21.

## TYPICAL CHARACTERISTICS (continued)

**SIGNAL-TO-NOISE RATIO vs REFERENCE VOLTAGE**

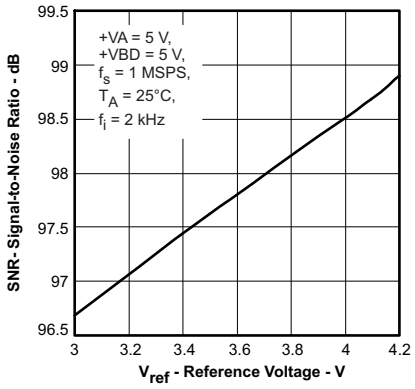



Figure 22.

**SIGNAL-TO-NOISE + DISTORTION vs REFERENCE VOLTAGE**

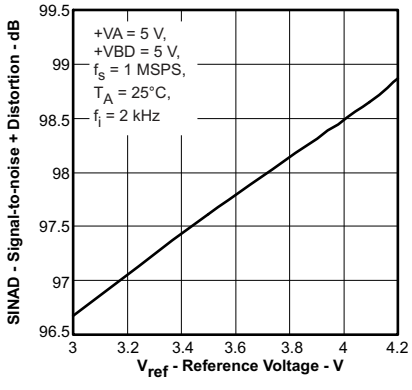



Figure 23.

**TOTAL HARMONIC DISTORTION vs FREE-AIR TEMPERATURE**

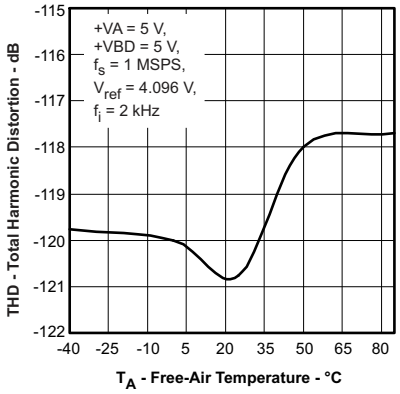



Figure 24.

**SPURIOUS FREE DYNAMIC RANGE vs FREE-AIR TEMPERATURE**

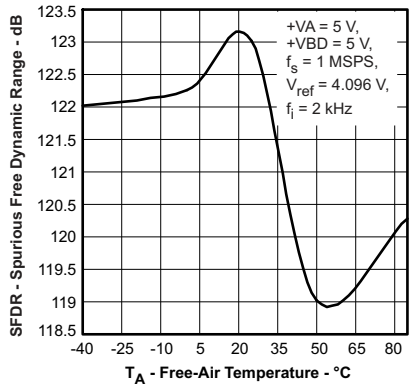



Figure 25.

**SIGNAL-TO-NOISE RATIO vs FREE-AIR TEMPERATURE**

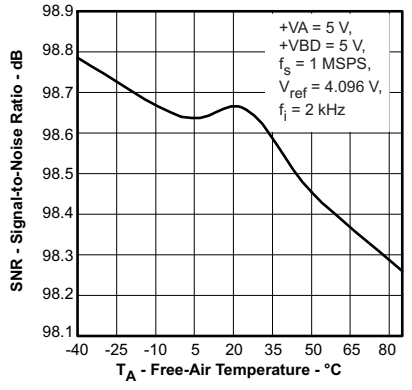



Figure 26.

**SIGNAL-TO-NOISE + DISTORTION vs FREE-AIR TEMPERATURE**

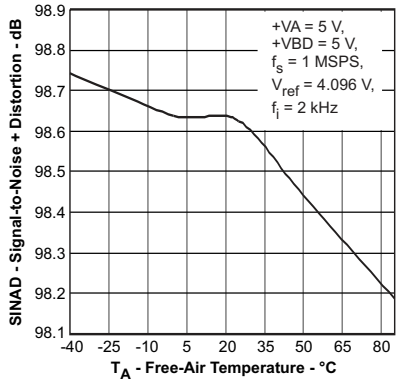



Figure 27.

**DNL**

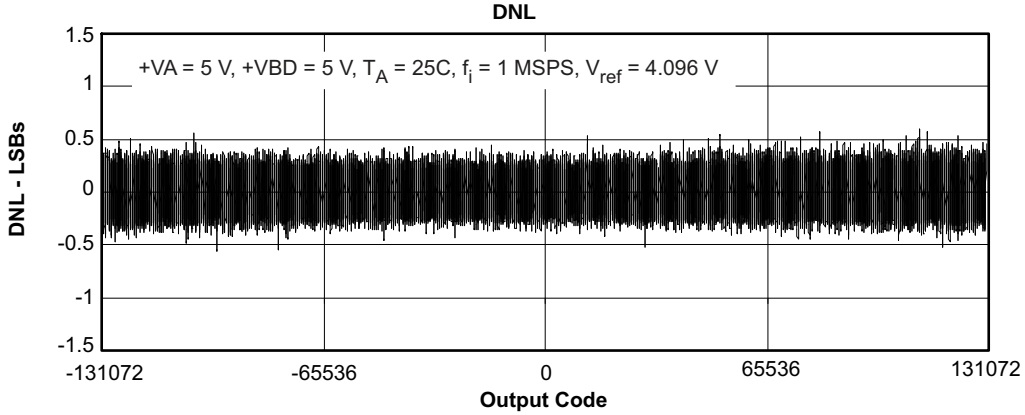



Figure 28.

## TYPICAL CHARACTERISTICS (continued)

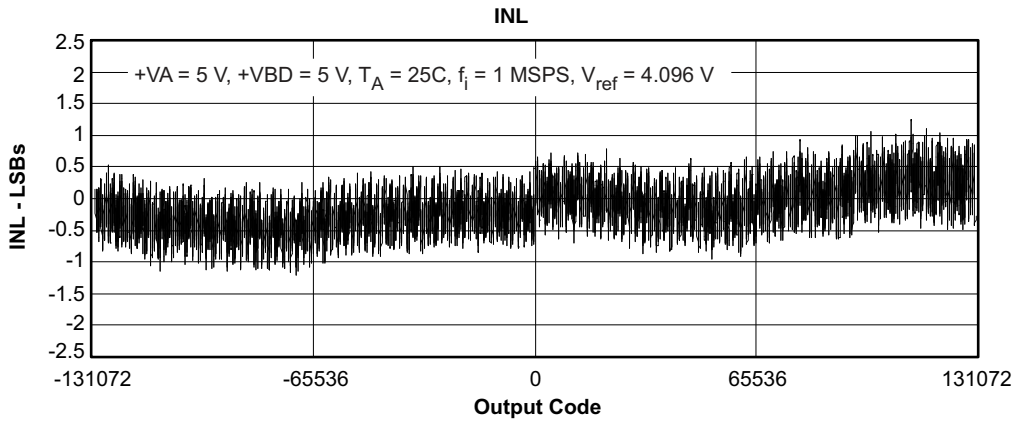
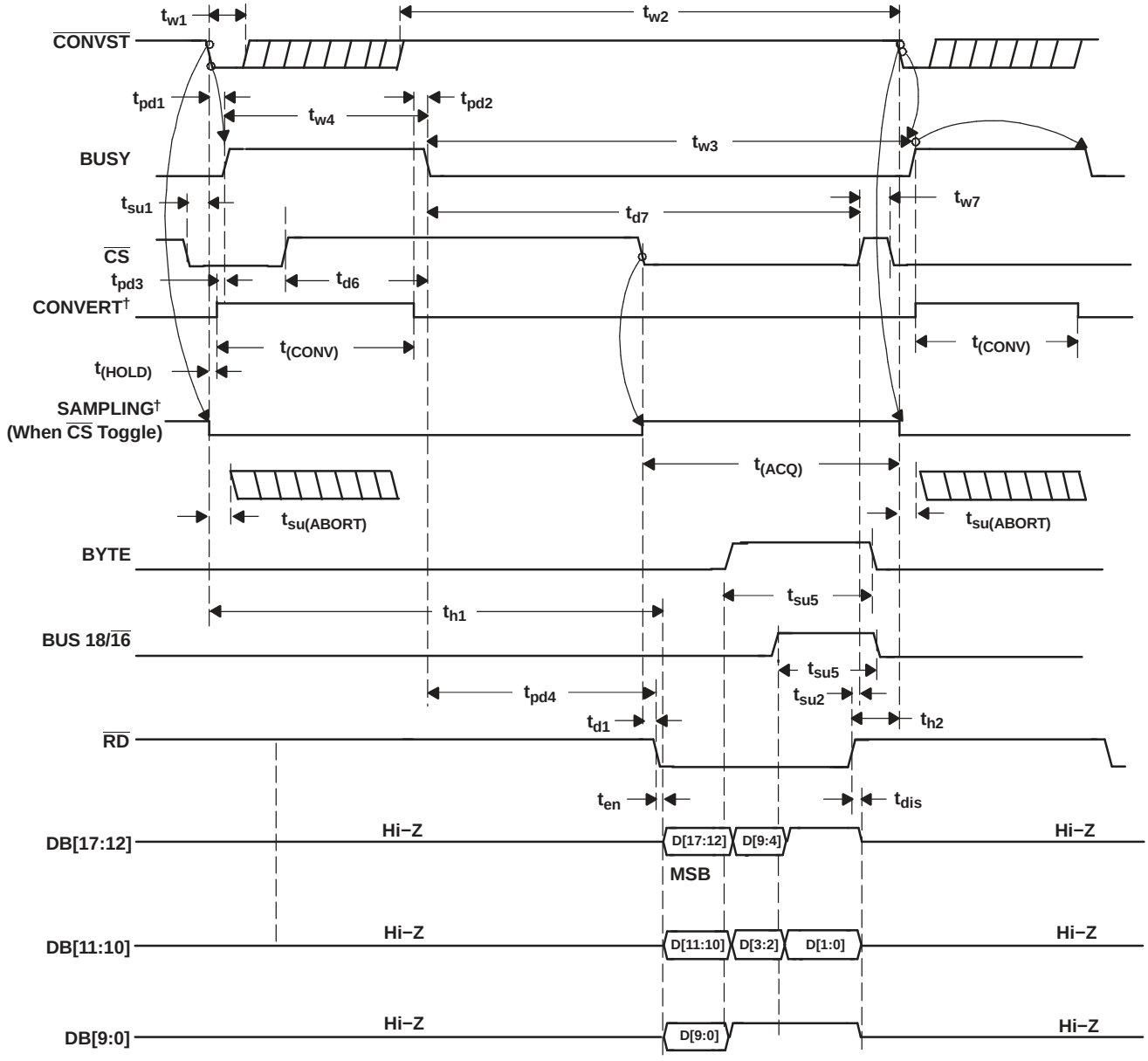


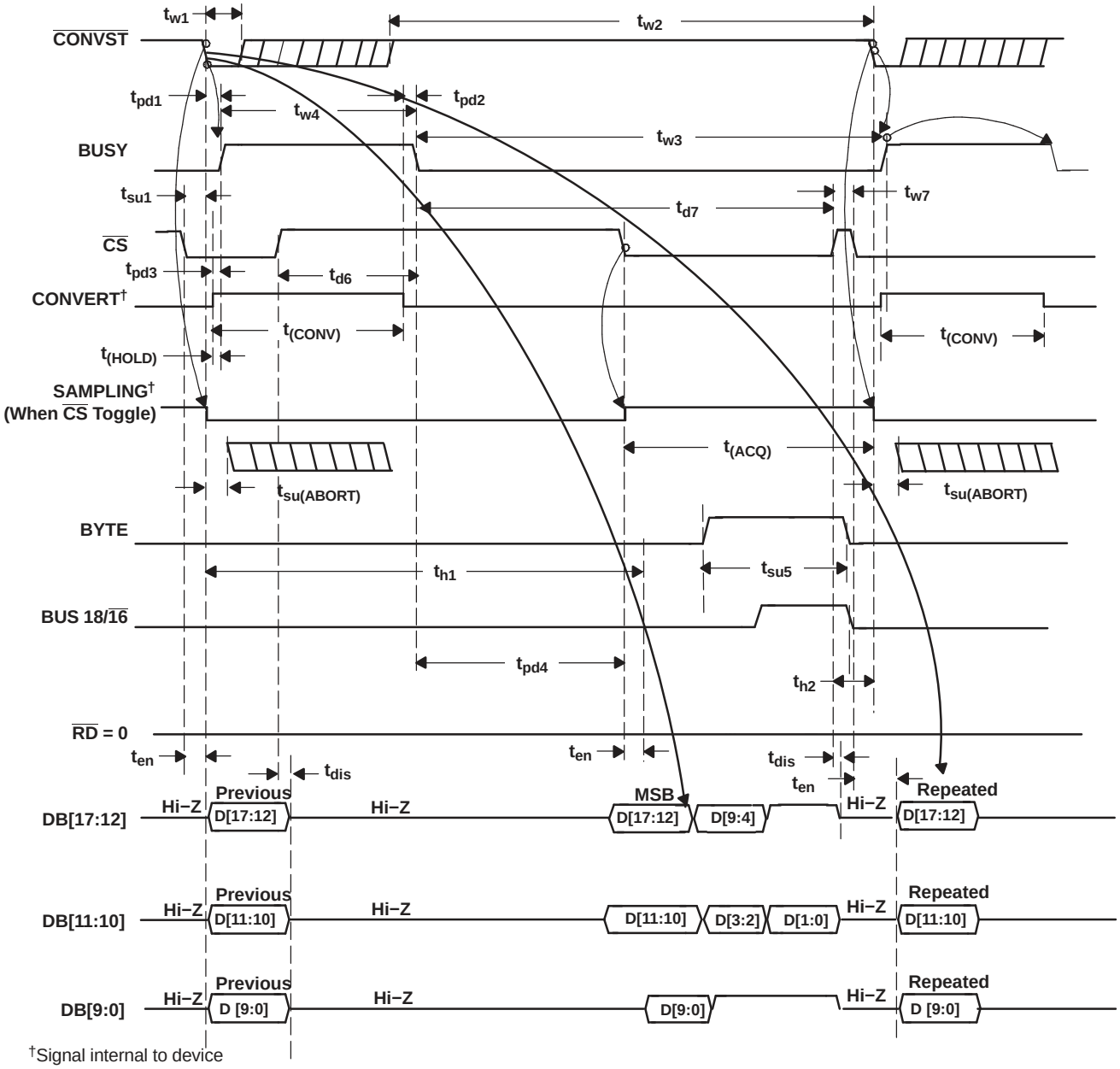

**Figure 29.**

## TIMING DIAGRAMS



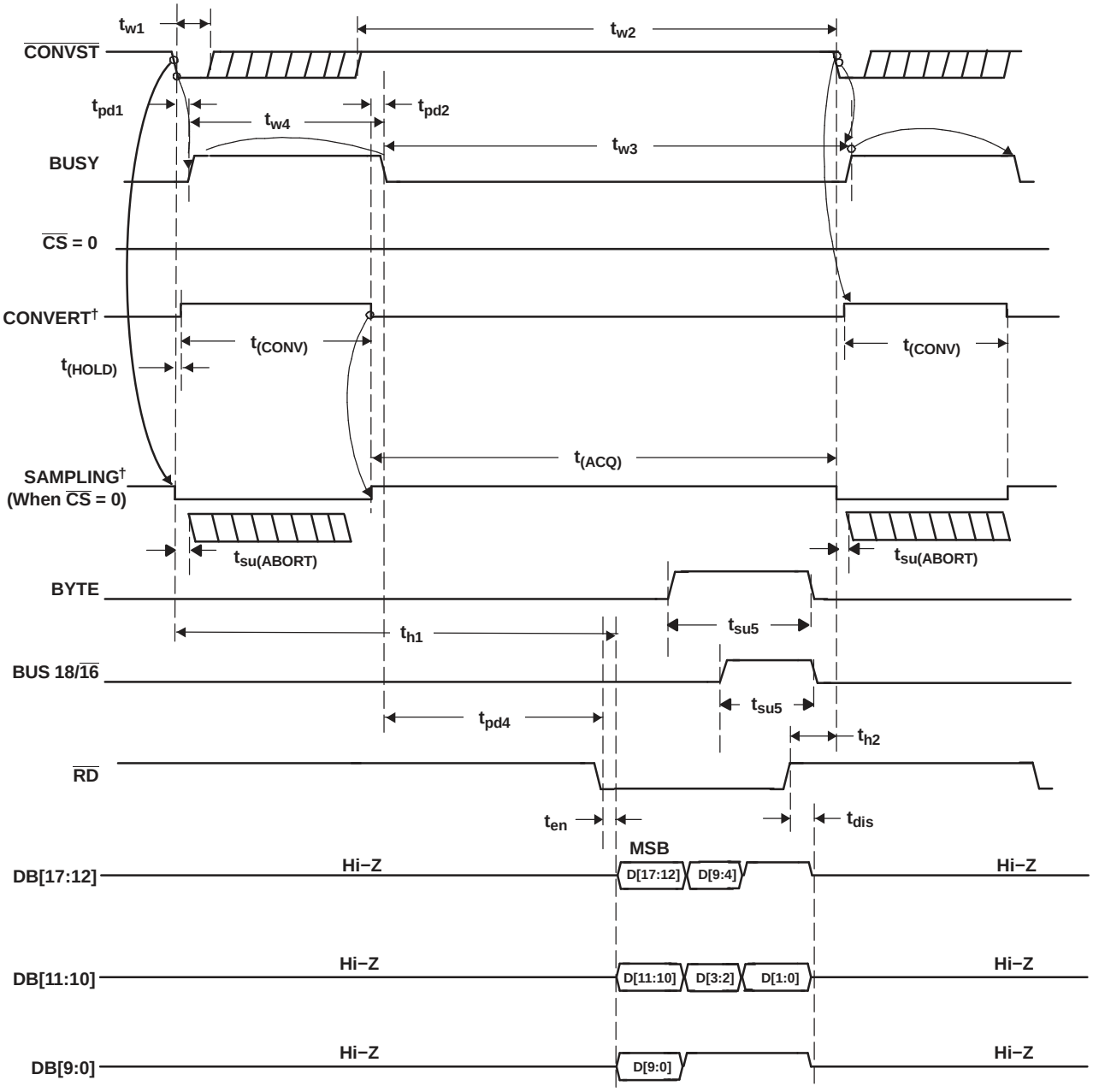

†Signal internal to device

**Figure 30. Timing for Conversion and Acquisition Cycles With $\overline{CS}$ and $\overline{RD}$ Toggling**



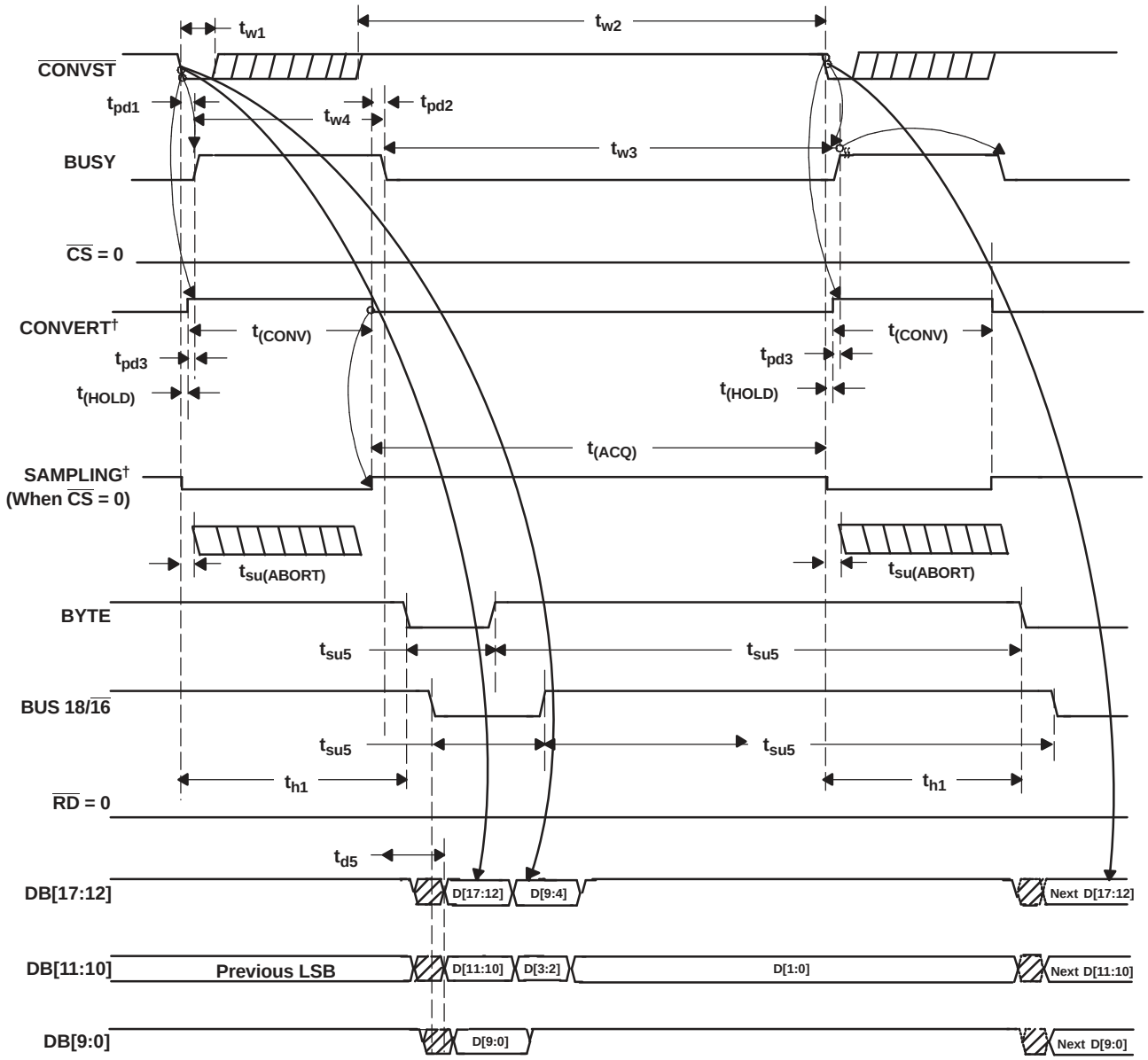

†Signal internal to device

**Figure 31. Timing for Conversion and Acquisition Cycles With $\overline{CS}$ Toggling, $\overline{RD}$ Tied to BDGND**




†Signal internal to device

**Figure 32. Timing for Conversion and Acquisition Cycles With $\overline{CS}$ Tied to BDGND, $\overline{RD}$ Toggling**




†Signal internal to device

**Figure 33. Timing for Conversion and Acquisition Cycles With $\overline{CS}$ and $\overline{RD}$ Tied to BDGND - Auto Read**

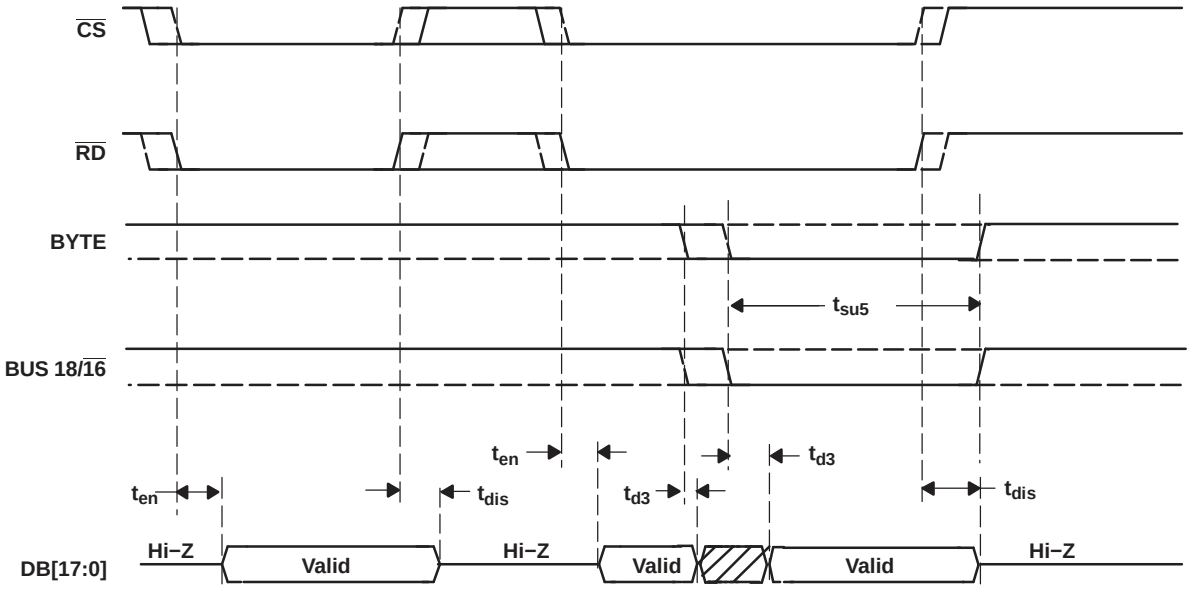



**Figure 34. Detailed Timing for Read Cycles**

# APPLICATION INFORMATION

## MICROCONTROLLER INTERFACING

### ADS8482 to 8-Bit Microcontroller Interface

Figure 35 shows a parallel interface between the ADS8482 and a typical microcontroller using the 8-bit data bus. The BUSY signal is used as a falling-edge interrupt to the microcontroller.

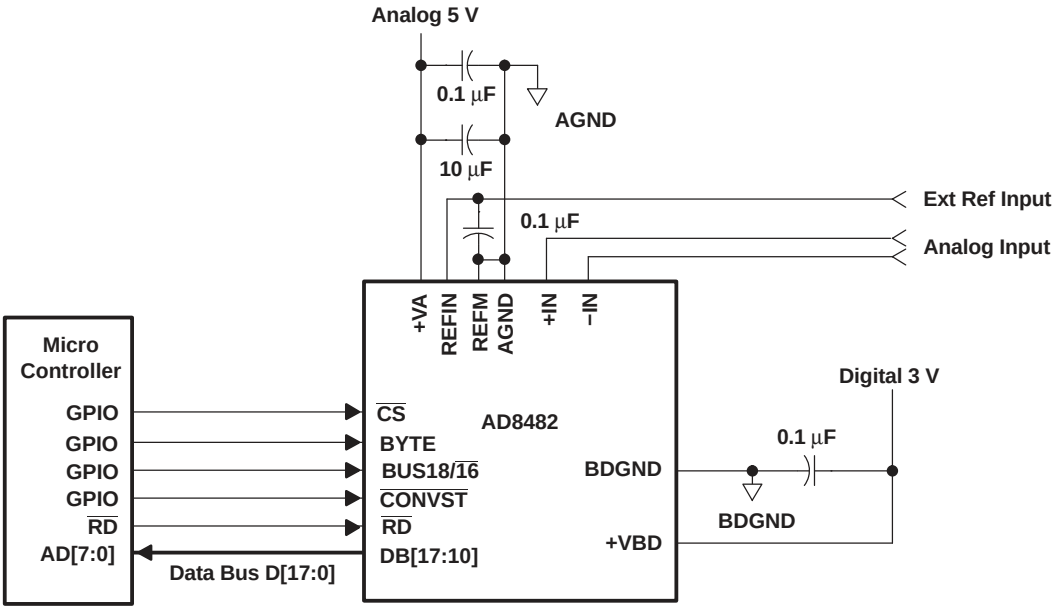



**Figure 35. ADS8482 Application Circuitry**

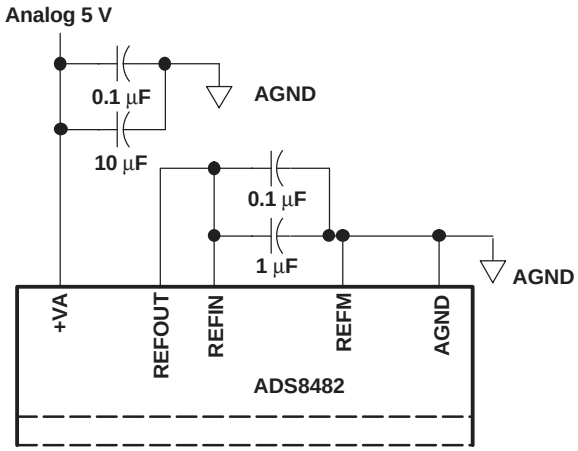



**Figure 36. ADS8482 Using Internal Reference**

## PRINCIPLES OF OPERATION

The ADS8482 is a high-speed successive approximation register (SAR) analog-to-digital converter (ADC). The architecture is based on charge redistribution which inherently includes a sample/hold function. See Figure 35 for the application circuit for the ADS8482.

The conversion clock is generated internally. The conversion time of 650 ns is capable of sustaining a 1 MHz throughput.

The analog input is provided to two input pins: +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

### REFERENCE

The ADS8482 can operate with an external reference with a range from 3.0 V to 4.2 V. The reference voltage on the input pin #13 (REFIN) of the converter is internally buffered. A clean, low noise, well-decoupled reference voltage on this pin is required to ensure good performance of the converter. A low noise band-gap reference like the REF3240 can be used to drive this pin. A 0.1-µF decoupling capacitor is required between REFIN and REFM pins (pin #13 and pin #12) of the converter. This capacitor should be placed as close as possible to the pins of the device. Designers should strive to minimize the routing length of the traces that connect the terminals of the capacitor to the pins of the converter. An RC network can also be used to filter the reference voltage. A 100-Ω series resistor and a 0.1-µF capacitor, which can also serve as the decoupling capacitor can be used to filter the reference voltage.

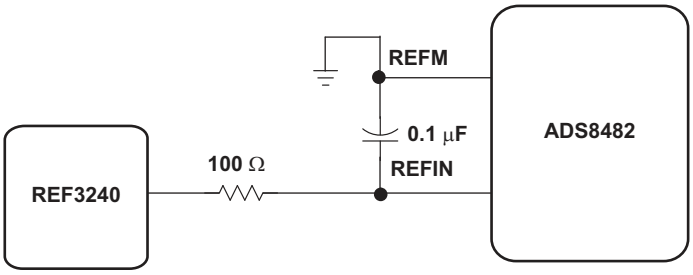



**Figure 37. ADS8482 Using External Reference**

The ADS8482 also has limited low pass filtering capability built into the converter. The equivalent circuitry on the REFIN input ia as shown in Figure 38.

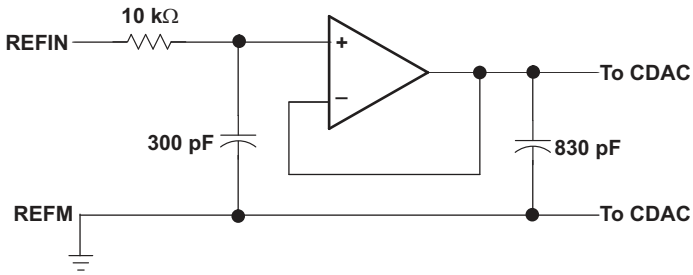



**Figure 38. Simplified Reference Input Circuit**

The REFM input of the ADS8482 should always be shorted to AGND. A 4.096-V internal reference is included. When internal reference is used, pin 14 (REFOUT) is connected to pin 13 (REFIN) with an 0.1-µF decoupling capacitor and 1-µF storage capacitor between pin 14 (REFOUT) and pins 11 and 12 (REFM) (see Figure 36). The internal reference of the converter is double buffered. If an external reference is used, the second buffer provides isolation between the external reference and the CDAC. This buffer is also used to recharge all of the capacitors of the CDAC during conversion. Pin 14 (REFOUT) can be left unconnected (floating) if external reference is used.

## PRINCIPLES OF OPERATION (continued)

### ANALOG INPUT

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs is captured on the internal capacitor array. Both +IN and –IN input has a range of –0.2 V to Vref + 0.2 V. The input span [+IN – (–IN)] is limited to $–V_{ref}$ to $V_{ref}$.

The input current on the analog inputs depends upon a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS8482 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input must be able to charge the input capacitance (65 pF) to an 18-bit settling level within the acquisition time (320 ns) of the device. When the converter goes into the hold mode, the input impedance is greater than 1 GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the +IN and –IN inputs and the span [+IN – (–IN)] must be within the limits specified. Outside of these ranges, the converter's linearity may not meet specifications. To minimize noise, low bandwidth input signals with low-pass filters are used.

Care must be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. If this is not observed, the two inputs could have different setting times. This may result in offset error, gain error, and linearity error which varies with temperature and input voltage.

The analog input to the converter needs to be driven with a low noise, high-speed op-amp like the THS4031. An RC filter is recommended at the input pins to low-pass filter the noise from the source. The input to the converter is a uni-polar input voltage in the range 0 to $V_{ref}$. The THS4031 can be used in the source follower configuration to drive the converter.

## PRINCIPLES OF OPERATION (continued)

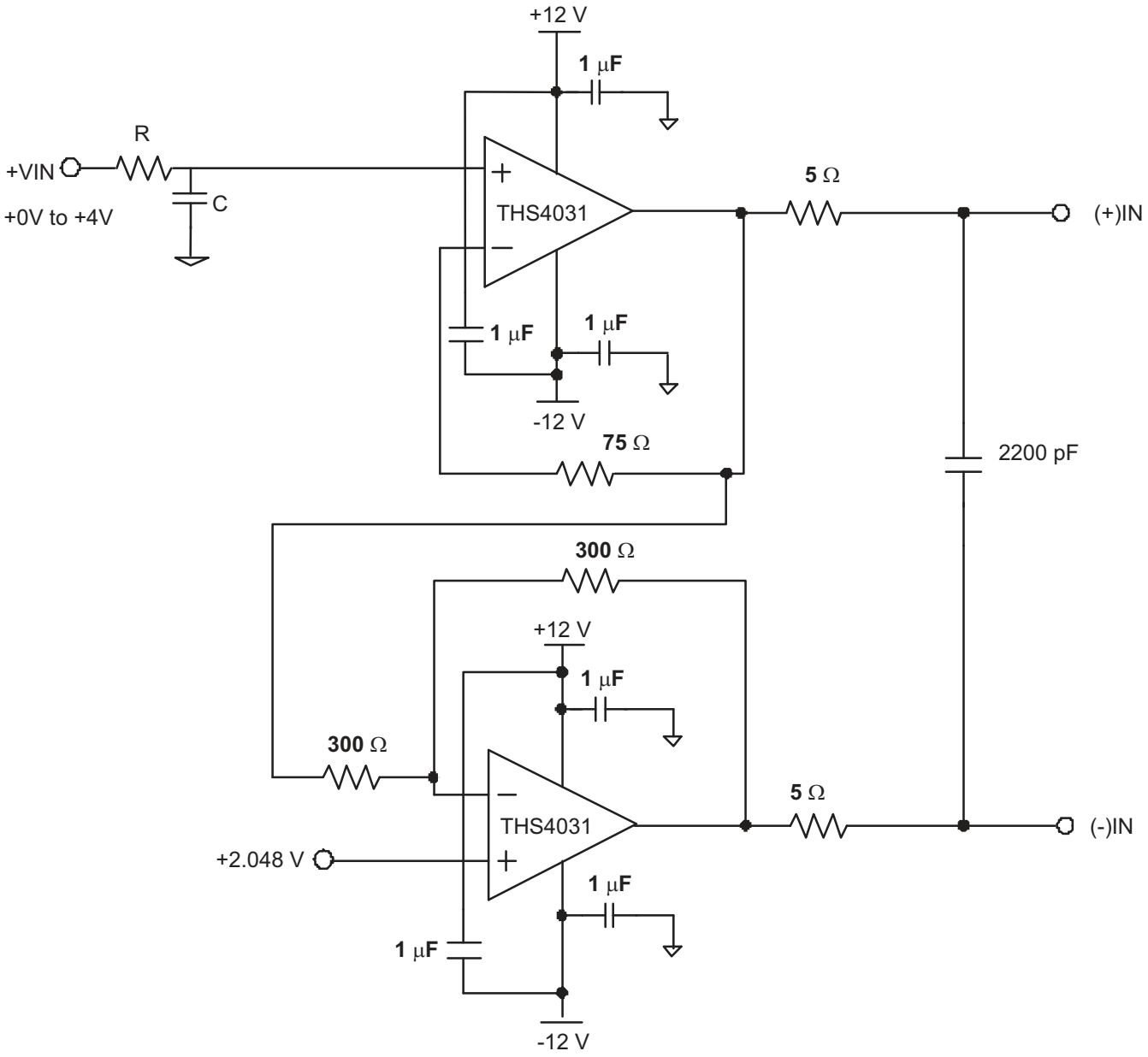



**Figure 39. Single-Ended Input, Differential Output Configuration**

In systems, where the input is differential, the THS4031 can be used in the inverting configuration with an additional DC bias applied to its + input so as to keep the input to the ADS8482 within its rated operating voltage range. The DC bias can be derived from the REF3220 or the REF3240 reference voltage ICs. The input configuration shown below is capable of delivering better than 97dB SNR and -103db THD at an input frequency of 100 kHz. In case band-pass filters are used to filter the input, care should be taken to ensure that the signal swing at the input of the band-pass filter is small so as to keep the distortion introduced by the filter minimal. In such cases, the gain of the circuit shown below can be increased to keep the input to the ADS8482 large to keep the SNR of the system high. Note that the gain of the system from the + input to the output of the THS4031 in such a configuration is a function of the gain of the AC signal. A resistor divider can be used to scale the output of the REF3220 or REF3240 to reduce the voltage at the DC input to THS4031 to keep the voltage at the input of the converter within its rated operating range.

## PRINCIPLES OF OPERATION (continued)

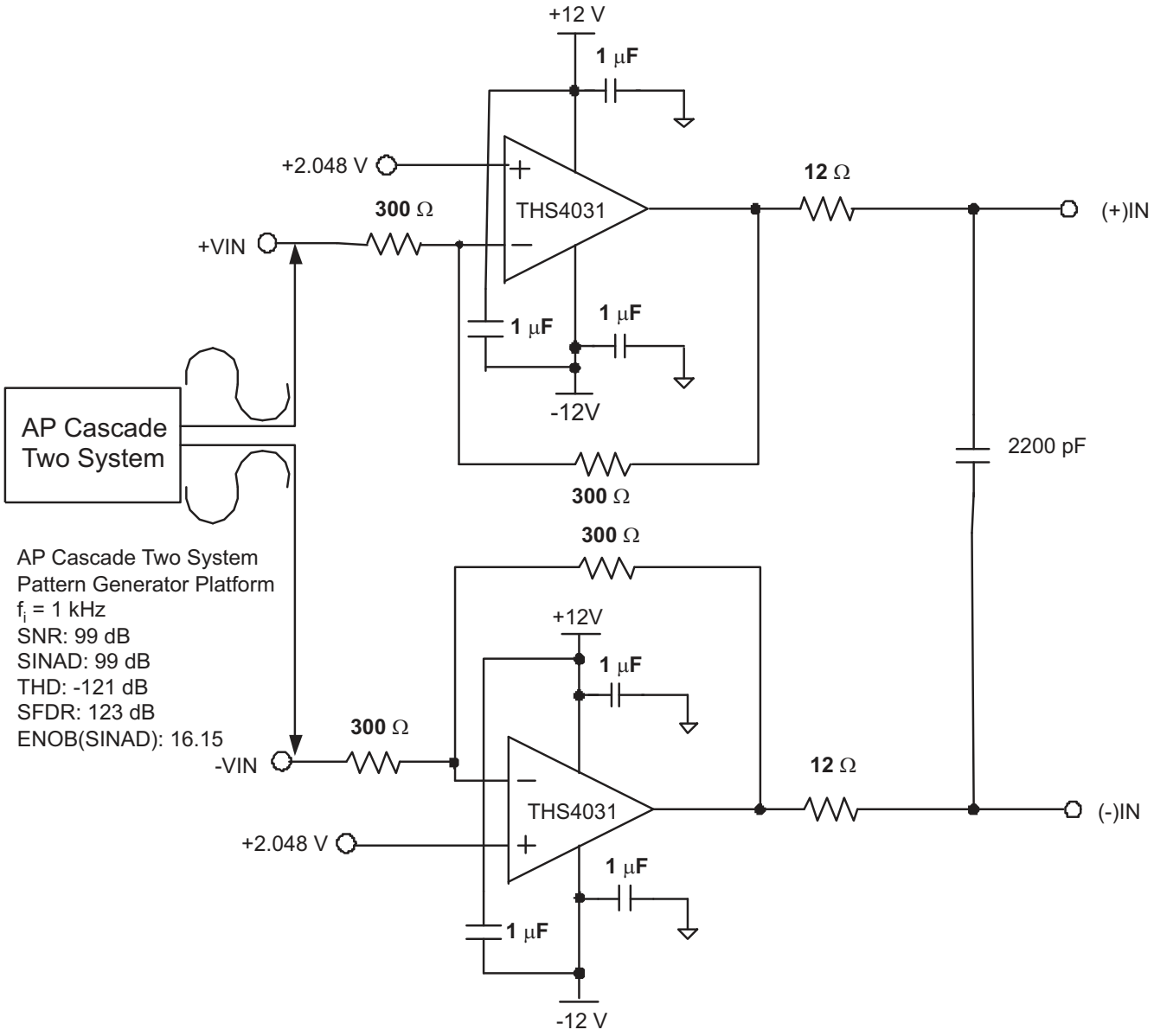



**Figure 40. Differential Input, Differential Output Configuration**

## DIGITAL INTERFACE

### Timing and Control

See the timing diagrams in the specifications section for detailed information on timing signals and their requirements.

The ADS8482 uses an internal oscillator generated clock which controls the conversion rate and in turn the throughput of the converter. No external clock input is required.

## PRINCIPLES OF OPERATION (continued)

Conversions are initiated by bringing the $\overline{\text{CONVST}}$ pin low for a minimum of 20 ns (after the 20 ns minimum requirement has been met, the $\overline{\text{CONVST}}$ pin can be brought high), while $\overline{\text{CS}}$ is low. The ADS8482 switches from the sample to the hold mode on the falling edge of the $\overline{\text{CONVST}}$ command. A clean and low jitter falling edge of this signal is important to the performance of the converter. The BUSY output is brought high immediately following $\overline{\text{CONVST}}$ going low. BUSY stays high throughout the conversion process and returns low when the conversion has ended.

Sampling starts with the falling edge of the BUSY signal when $\overline{\text{CS}}$ is tied low or starts with the falling edge of $\overline{\text{CS}}$ when BUSY is low.

Both $\overline{\text{RD}}$ and $\overline{\text{CS}}$ can be high during and before a conversion with one exception ($\overline{\text{CS}}$ must be low when $\overline{\text{CONVST}}$ goes low to initiate a conversion). Both the $\overline{\text{RD}}$ and $\overline{\text{CS}}$ pins are brought low in order to enable the parallel output bus with the conversion.

### Reading Data

The ADS8482 outputs full parallel data in straight binary format as shown in Table 1. The parallel output is active when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both low. There is a minimal quiet zone requirement around the falling edge of $\overline{\text{CONVST}}$. This is 50 ns prior to the falling edge of $\overline{\text{CONVST}}$ and 40 ns after the falling edge. No data read should attempted within this zone. Any other combination of $\overline{\text{CS}}$ and $\overline{\text{RD}}$ sets the parallel output to 3-state. BYTE and BUS18/$\overline{16}$ are used for multiword read operations. BYTE is used whenever lower bits on the bus are output on the higher byte of the bus. BUS18/$\overline{16}$ is used whenever the last two bits on the 18-bit bus is output on either bytes of the higher 16-bit bus. Refer to Table 1 for ideal output codes.

**Table 1. Ideal Input Voltages and Output Codes**

| DESCRIPTION | ANALOG VALUE | DIGITAL OUTPUT STRAIGHT BINARY | |
|---|---|---|---|
| Full scale range | $+V_{ref}$ | | |
| Least significant bit (LSB) | $2 \times (+V_{ref})/262144$ | BINARY CODE | HEX CODE |
| +Full scale | $(+V_{ref}) – 1$ LSB | 01 1111 1111 1111 1111 | 1FFFF |
| Midscale | 0 V | 00 0000 0000 0000 0000 | 00000 |
| Midscale – 1 LSB | 0 V – 1 LSB | 11 1111 1111 1111 1111 | 3FFFF |
| Zero | $–V_{ref}$ | 10 0000 0000 0000 0000 | 20000 |

The output data is a full 18-bit word (D17–D0) on DB17–DB0 pins (MSB–LSB) if both BUS18/$\overline{16}$ and BYTE are low.

The result may also be read on an 16-bit bus by using only pins DB17–DB2. In this case two reads are necessary: the first as before, leaving both BUS18/$\overline{16}$ and BYTE low and reading the 16 most significant bits (D17–D2) on pins DB17–DB2, then bringing BUS18/$\overline{16}$ high while holding BYTE low. When BUS18/$\overline{16}$ is high, the lower two bits (D1–D0) appear on pins DB3–DB2.

The result may also be read on an 8-bit bus for convenience. This is done by using only pins DB17–DB10. In this case three reads are necessary: the first as before, leaving both BUS18/$\overline{16}$ and BYTE low and reading the 8 most significant bits on pins DB17–DB10, then bringing BYTE high while holding BUS18/$\overline{16}$ low. When BYTE is high, the medium bits (D9–D2) appear on pins DB17–DB10. The last read is done by bringing BUS18/$\overline{16}$ high while holding BYTE high. When BUS18/$\overline{16}$ is high, the lower two bits (D1–D0) appear on pins DB11–DB10. The last read cycle is not necessary if only the first 16 most significant bits are of interest.

All of these multiword read operations can be performed with multiple active $\overline{\text{RD}}$ (toggling) or with $\overline{\text{RD}}$ held low for simplicity. This is referred to as the AUTO READ operation.

**Table 2. Conversion Data Read Out**

| BYTE | BUS18/$\overline{16}$ | DATA READ OUT | | | | |
|---|---|---|---|---|---|---|
| | | PINS DB17–DB12 | PINS DB11–DB10 | PINS DB9–DB4 | PINS DB3–DB2 | PINS DB1–DB0 |
| High | High | All One's | D1–D0 | All One's | All One's | All One's |
| Low | High | All One's | All One's | All One's | D1–D0 | All One's |

**Table 2. Conversion Data Read Out (continued)**

| BYTE | BUS18/$\overline{16}$ | DATA READ OUT | | | | |
|---|---|---|---|---|---|---|
| | | PINS DB17–DB12 | PINS DB11–DB10 | PINS DB9–DB4 | PINS DB3–DB2 | PINS DB1–DB0 |
| High | Low | D9–D4 | D3–D2 | All One's | All One's | All One's |
| Low | Low | D17–D12 | D11–D10 | D9–D4 | D3–D2 | D1–D0 |

## RESET

On power-up, internal POWER-ON RESET circuitry generates the reset required for the device. The first three conversions after power-up are used to load factory trimming data for a specific device to assure high accuracy of the converter. The results of the first three conversions are invalid and should be discarded.

The device can also be reset through the use of the combination fo $\overline{CS}$ and $\overline{CONVST}$. Since the BUSY signal is held at high during the conversion, either one of these conditions triggers an internal self-clear reset to the converter.

- Issue a $\overline{CONVST}$ when $\overline{CS}$ is low and the internal convert state is high. The falling edge of $\overline{CONVST}$ starts a reset.
- Issue a $\overline{CS}$ (select the device) while the internal convert state is high. The falling edge of $\overline{CS}$ causes a reset.

Once the device is reset, all output latches are cleared (set to zeroes) and the BUSY signal is brought low. A new sampling period is started at the falling edge of the BUSY signal immediately after the instant of the internal reset.

## LAYOUT

For optimum performance, care must be taken with the physical layout of the ADS8482 circuitry.

As the ADS8482 offers single-supply operation, it is often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to achieve good performance from the converter.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections and digital inputs that occur just prior to latching the output of the analog comparator. Thus, driving any single conversion for an n-bit SAR converter, there are at least n windows in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high power devices.

The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event.

On average, the ADS8482 draws very little current from an external reference as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. A 0.1-µF capacitor is recommended from pin 13 (REFIN) directly to pin 12 (REFM). REFM and AGND must be shorted on the same ground plane under the device.

The AGND and BDGND pins should be connected to a clean ground point. In all cases, this should be the analog ground. Avoid connections which are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout consists of an analog ground plane dedicated to the converter and associated analog circuitry.

As with the AGND connections, +VA should be connected to a 5-V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. Power to the ADS8482 should be clean and well bypassed. A 0.1-µF ceramic bypass capacitor should be placed as close to the device as possible. See Table 3 for the placement of the capacitor. In addition, a 1-µF to 10-µF capacitor is recommended. In some situations, additional bypassing may be required, such as a 100-µF electrolytic capacitor or even a Pi filter made up of inductors and capacitors-all designed to essentially low-pass filter the 5-V supply, removing the high frequency noise.

**Table 3. Power Supply Decoupling Capacitor Placement**

| POWER SUPPLY PLANE<br>SUPPLY PINS | CONVERTER ANALOG SIDE | CONVERTER DIGITAL SIDE |
|---|---|---|
| Pin pairs that require shortest path to decoupling capacitors | (7,8), (9,10), (16,17), (20,21), (22,23), (25,26) | (36,37) |
| Pins that require no decoupling | 24, 26 | 1 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS8482IBRGZT | NRND | VQFN | RGZ | 48 | 250 | RoHS & Green | Call TI | Level-2-260C-1 YEAR | -40 to 85 | ADS 8482I B | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

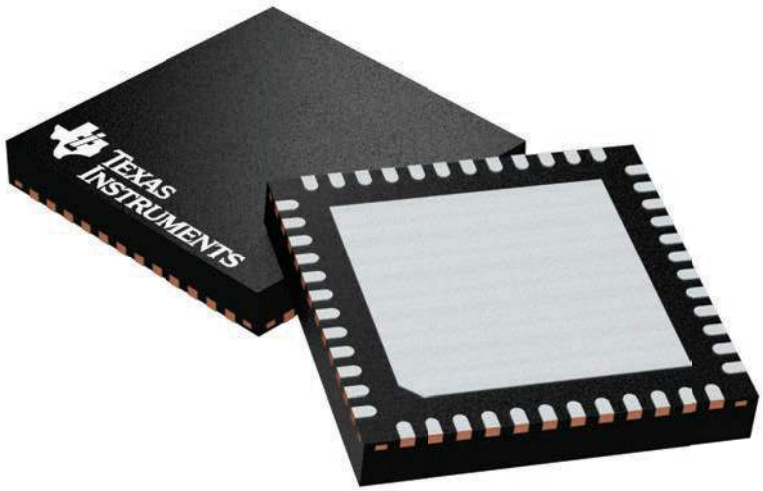
# GENERIC PACKAGE VIEW

## RGZ 48

## VQFN - 1 mm max height

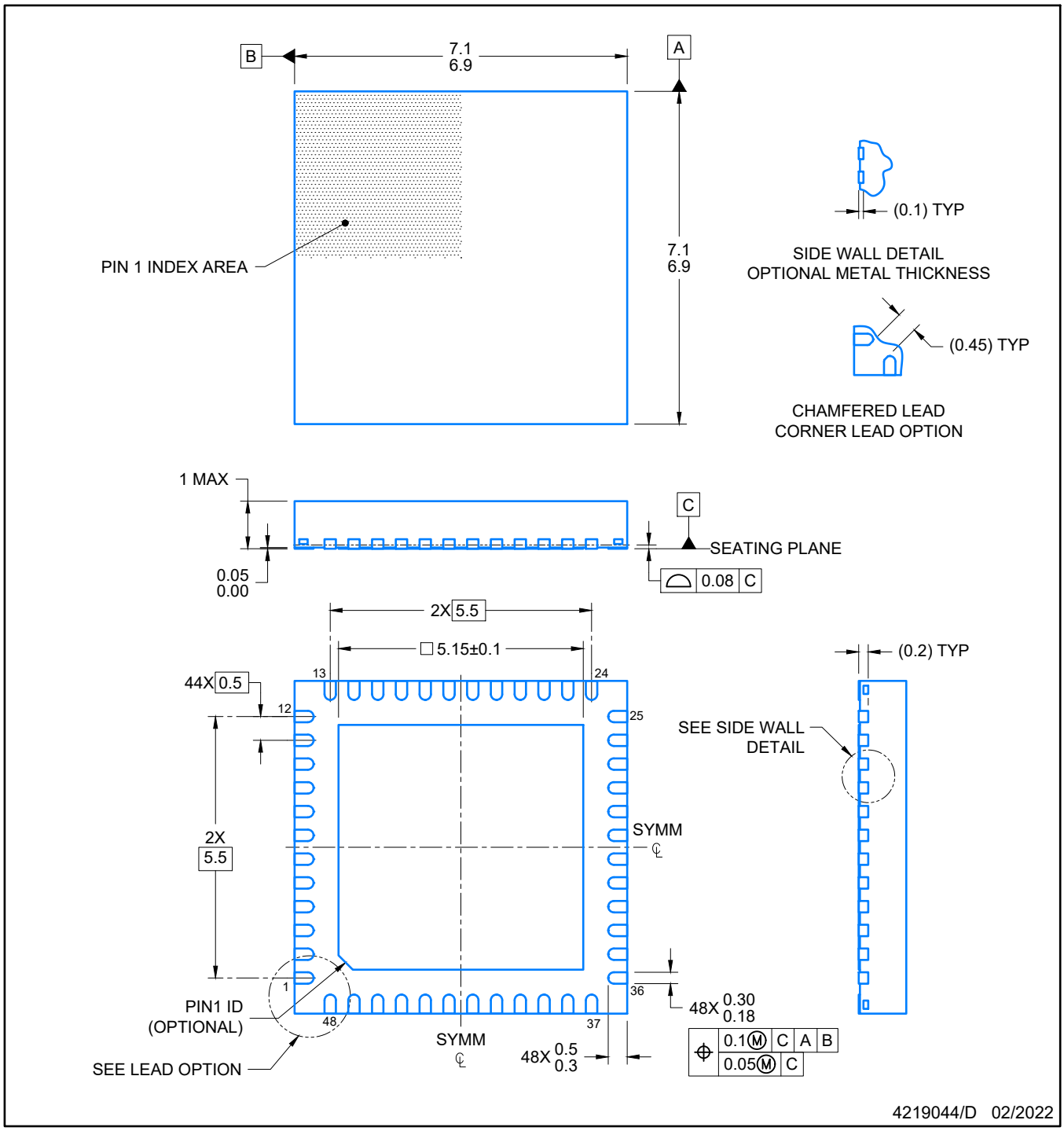
**7 x 7, 0.5 mm pitch**

PLASTIC QUADFLAT PACK- NO LEAD



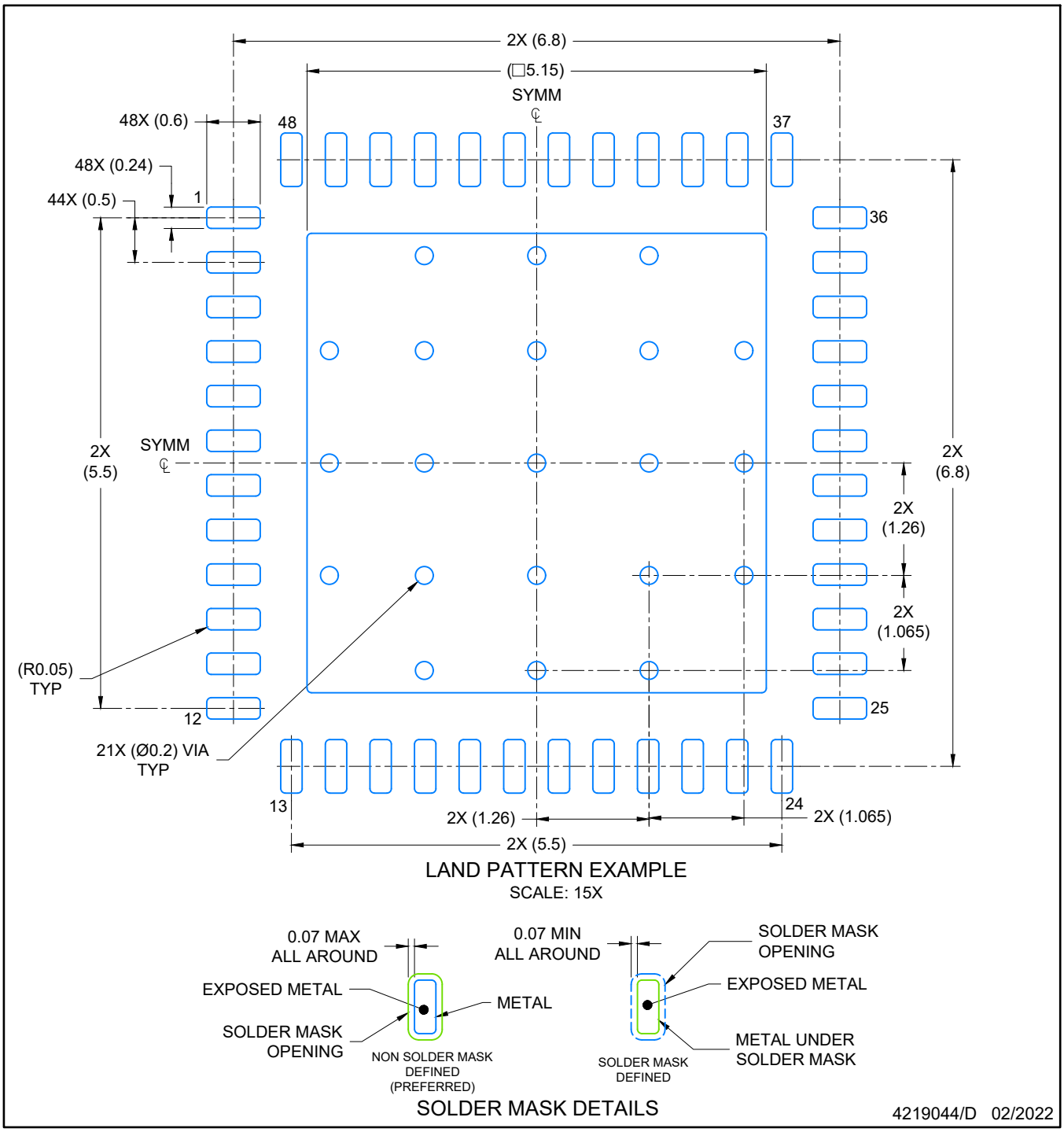

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A



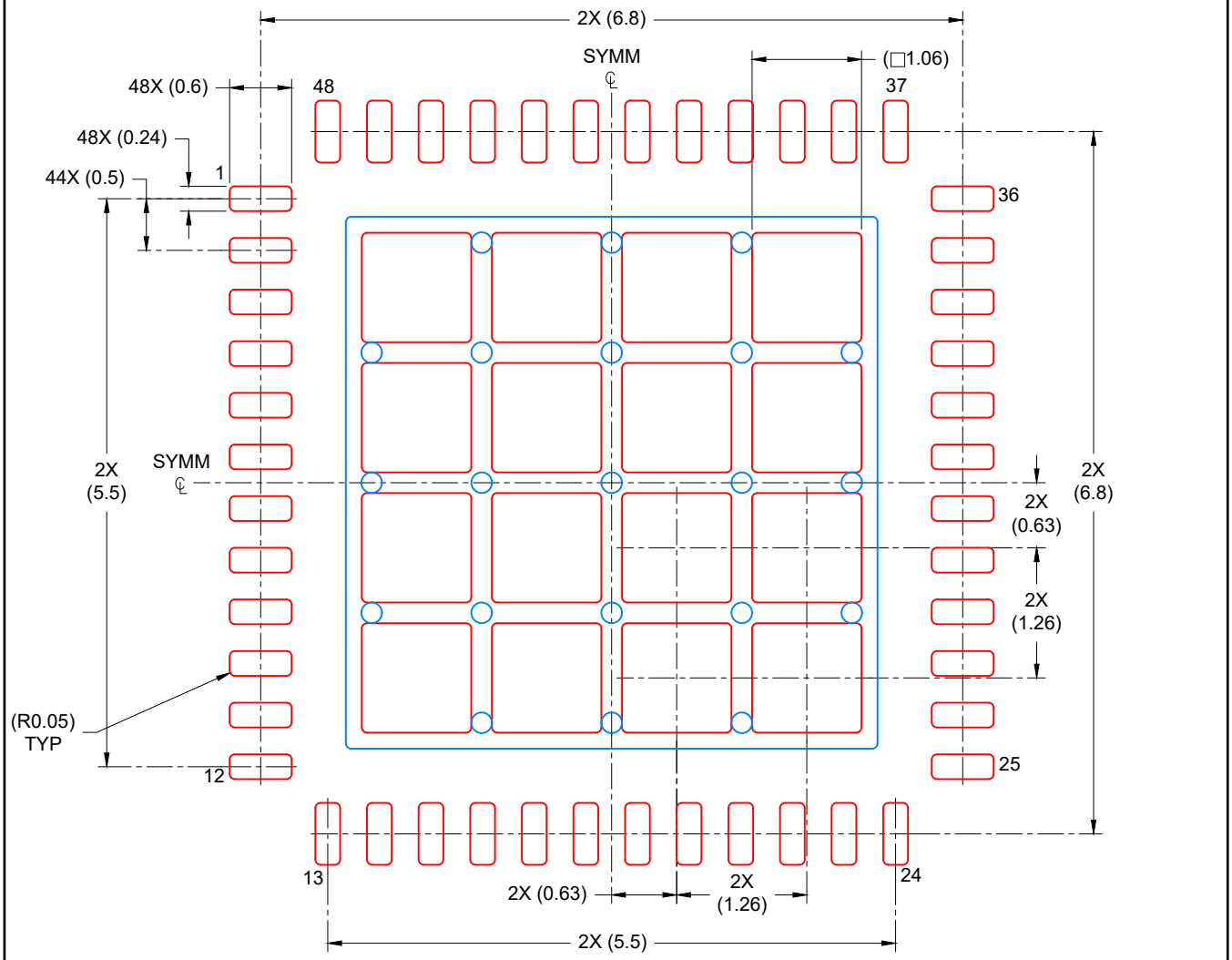

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

4219044/D 02/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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