16:1 LVCMOS/LVTTL-TO-LVPECL/LVDS CLOCK MULTIPLEXER

ICS859S1601I

General Description

The ICS859S1061I is an16:1 LVCMOS/LVTTL-to-LVPECL/ LVDS Clock Multiplexer which can operate up to 250MHz and is a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. Differential output levels can either be selected to LVDS or LVPECL. The ICS859S1061I has 16 selectable single-ended clock inputs. The fully differential architecture and low propagation delay make it ideal for use in clock distribution circuits. The select pins have internal pulldown resistors. The CLK_SEL3 pin is the most significant bit and the binary number applied to the select pins will select the same numbered data input (i.e., 0000 selects CLK0).

Features

- High speed 16:1 differential multiplexer
- One differential LVPECL or LVDS output pair
- Sixteen selectable LVCMOS/LVTTL clock inputs
- CLKx can accept the following input levels: LVCMOS and LVTTL
- Maximum output frequency: 250MHz
- Propagation delay: 1.0ns (typical)
- Full 3.3V or 2.5V supply modes
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

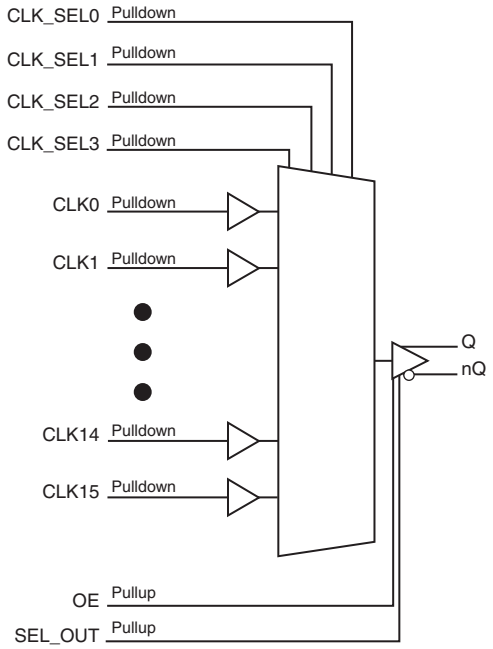
Table 1A. V_{CC_TAP} Function Table

Outputs		
Q/nQ	**Output Level Supply**	**V_{CC_TAP}**
LVPECL	2.5V	V_{CC}
LVPECL	3.3V	V_{CC}
LVDS	2.5V	V_{CC}
LVDS	3.3V	Float

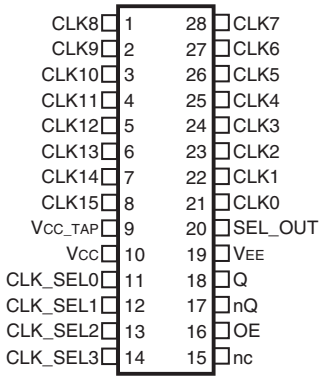
Table 1B. SEL_OUT Function Table

Input	Outputs
SEL_OUT	**Q/nQ**
1	LVPECL
0	LVDS

Block Diagram



Pin Assignment



ICS859S1061I

28-Lead TSSOP, 173MIL
4.4mm x 9.7mm x 0.925mm
package body
G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

Table 2. Pin Descriptions

Number	Name	Type		Description
1	CLK8	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
2	CLK9	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
3	CLK10	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
4	CLK11	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
5	CLK12	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
6	CLK13	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
7	CLK14	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
8	CLK15	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
9	V_{CC_TAP}	Power		Power supply pin. See Table 1A.
10	V_{CC}	Power		Power supply pin.
11, 12. 13, 14	CLK_SEL0, CLK_SEL1, CLK_SEL2, CLK_SEL3	Input	Pulldown	Clock select inputs. See Table 4A. LVCMOS / LVTTL interface levels.
15	nc	Unused		No connect.
16	OE	Input	Pullup	Output enable pin for Q/nQ outputs. See Table 4B. LVCMOS/LVTTL interface levels.
17, 18	nQ, Q	Output		Differential output pair. LVPECL or LVDS interface levels.
19	V_{EE}	Power		Negative supply pin.
20	SEL_OUT	Input	Pullup	Output select pin. When LOW, selects LVDS levels. When HIGH, selects LVPECL levels. LVCMOS/LVTTL interface levels. See Table 1B.
21	CLK0	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
22	CLK1	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
23	CLK2	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
24	CLK3	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
25	CLK4	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
26	CLK5	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
27	CLK6	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
28	CLK7	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 3. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 4A. Clock Input Function Table

Inputs				Outputs
CLK_SEL3	CLK_SEL2	CLK_SEL1	CLK_SEL0	Q/nQ
0	0	0	0	CLK0
0	0	0	1	CLK1
0	0	1	0	CLK2
0	0	1	1	CLK3
0	1	0	0	CLK4
0	1	0	1	CLK5
0	1	1	0	CLK6
0	1	1	1	CLK7
1	0	0	0	CLK8
1	0	0	1	CLK9
1	0	1	0	CLK10
1	0	1	1	CLK11
1	1	0	0	CLK12
1	1	0	1	CLK13
1	1	1	0	CLK14
1	1	1	1	CLK15

Table 4B. Output Enable Function Table

Input	
OE	Outputs
1	Q/nQ (default)
0	Clock stop, High/Low

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current Outputs, I_O (LVDS) Continuos Current Surge Current	 50mA 100mA 10mA 15mA
Package Thermal Impedance, θ_{JA}	77.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 5A. LVPECL Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{CC_TAP}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			40		mA

Table 5B. LVPECL Power Supply DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{CC_TAP}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			38		mA

Table 5C. LVDS Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			54		mA

Table 5D. LVDS Power Supply DC Characteristics, V_{CC} = V_{CC_TAP} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{CC_TAP}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			51		mA

Table 5E. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.465V	2		V_{CC} + 0.3	V
			V_{CC} = 2.625V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.465V	-0.3		0.8	V
			V_{CC} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	CLK[0:15], CLK_SEL[0:3]	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
		OE, SEL_OUT	V_{CC} = V_{IN} = 3.465V or 2.625V			-10	µA
I_{IL}	Input Low Current	CLK[0:15], CLK_SEL[0:3]	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA
		OE, SEL_OUT	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

Table 5F. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Current; NOTE 1			V_{CC} – 1.0		µA
V_{OL}	Output Low Current; NOTE 1			V_{CC} – 1.4		µA
V_{SWING}	Peak-to-peak Output Voltage Swing			0.6		V

NOTE 1: Outputs termination with 50Ω to V_{CC} – 2V.

Table 5G. LVDS DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	SEL_OUT = 0		370		mV
ΔV_{OD}	V_{OD} Magnitude Change	SEL_OUT = 0		40		mV
V_{OS}	Offset Voltage	SEL_OUT = 0		1.21		V
ΔV_{OS}	V_{OS} Magnitude Change	SEL_OUT = 0		50		mV

Table 5H. LVDS DC Characteristics, $V_{CC} = V_{CC\_TAP} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	SEL_OUT = 0		350		mV
ΔV_{OD}	V_{OD} Magnitude Change	SEL_OUT = 0		40		mV
V_{OS}	Offset Voltage	SEL_OUT = 0		1.18		V
ΔV_{OS}	V_{OS} Magnitude Change	SEL_OUT = 0		50		mV

AC Electrical Characteristics

Table 6A. LVPECL AC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1			1.0		ns
$t$jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.52MHz, Integration Range: 12kHz – 20MHz		0.20		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		200		ps
odc	Output Duty Cycle			50		%
$MUX_{ISOLATION}$	MUX Isolation	155.52MHz		33		dB

NOTE 1: Measured from $V_{CC}/2$ of the input to the differential output crossing point.

Table 6B. LVPECL AC Characteristics, $V_{CC} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1			1.1		ns
$t$jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.52MHz, Integration Range: 12kHz – 20MHz		0.22		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		200		ps
odc	Output Duty Cycle			50		%
$MUX_{ISOLATION}$	MUX Isolation	155.52MHz		34.5		dB

NOTE 1: Measured from $V_{CC}/2$ of the input to the differential output crossing point.

Table 6C. LVDS AC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1			1.0		ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.52MHz, Integration Range: 12kHz – 20MHz		0.22		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		200		ps
odc	Output Duty Cycle			50		%
$MUX_{ISOLATION}$	MUX Isolation	155.52MHz		51		dB

NOTE 1: Measured from V_{CC}/2 of the input to the differential output crossing point.

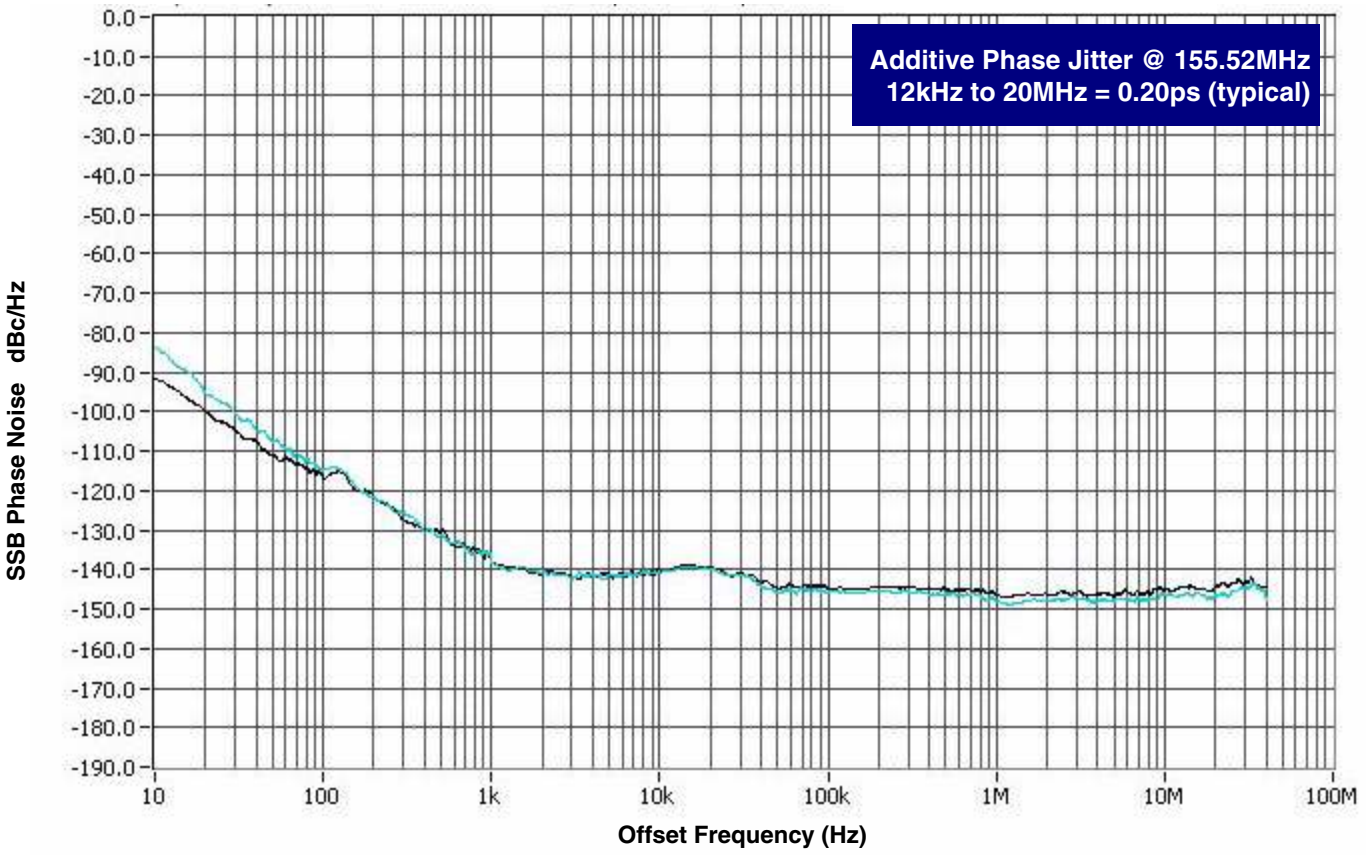
Table 6D. LVDS AC Characteristics, V_{CC} = V_{CC_TAP} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1			1.0		ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.52MHz, Integration Range: 12kHz – 20MHz		0.23		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		200		ps
odc	Output Duty Cycle			50		%
$MUX_{ISOLATION}$	MUX Isolation	155.52MHz		46.6		dB

NOTE 1: Measured from V_{CC}/2 of the input to the differential output crossing point.

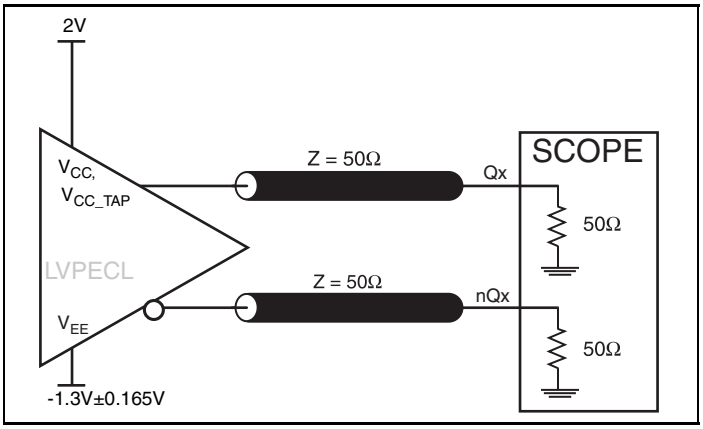
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

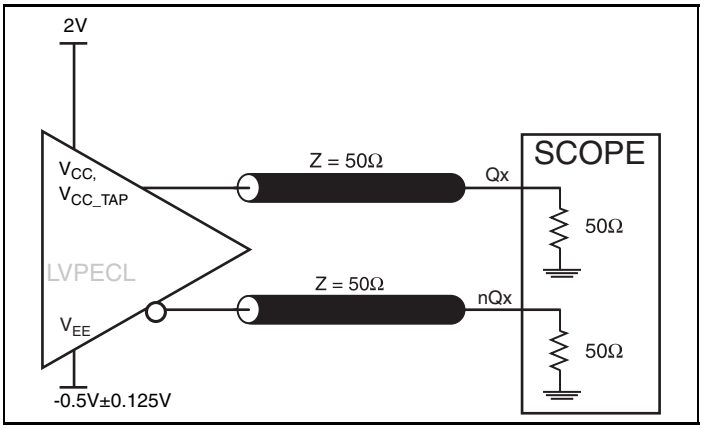


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

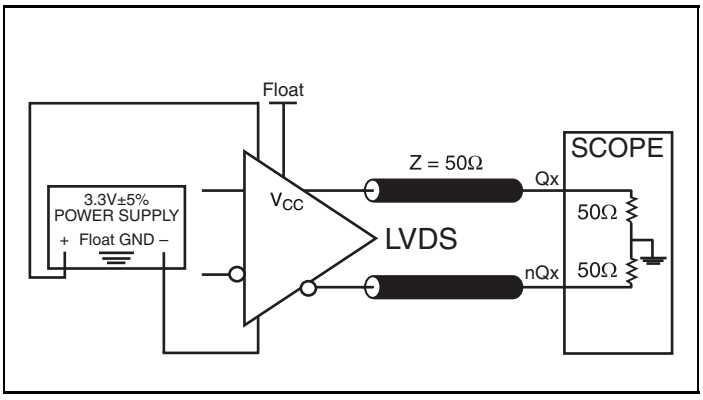
Parameter Measurement Information



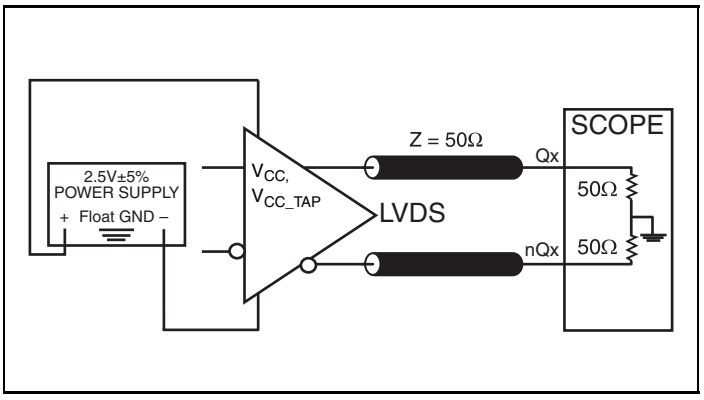
3.3V LVPECL Output Load AC Test Circuit



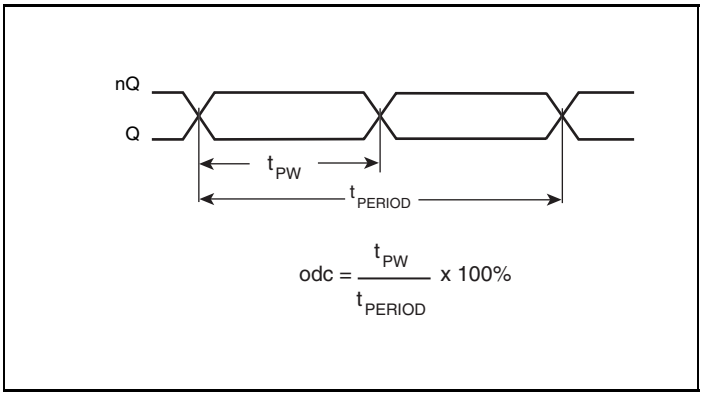
2.5V LVPECL Output Load AC Test Circuit



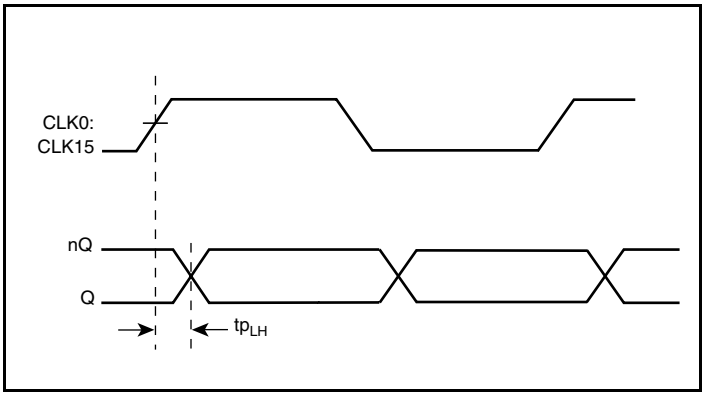
3.3V LVDS Output Load AC Test Circuit



2.5V LVDS Output Load AC Test Circuit

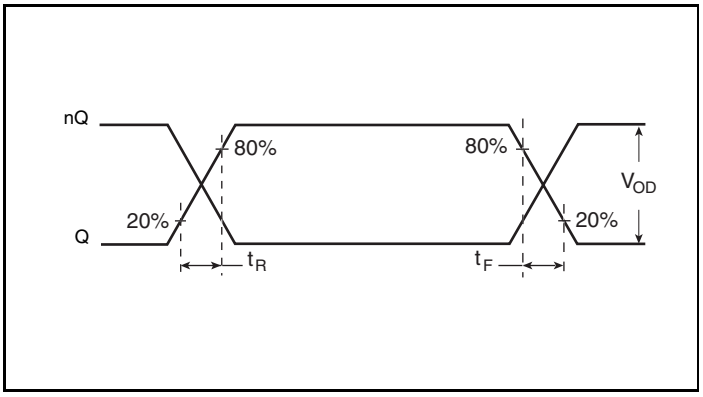


Output Duty Cycle/Pulse Width/Period

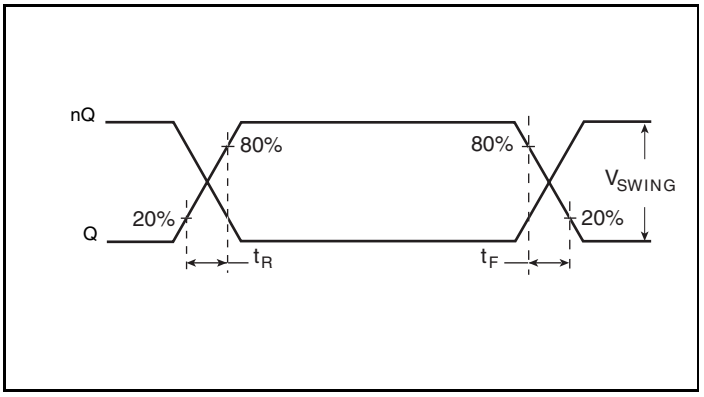


Propagation Delay

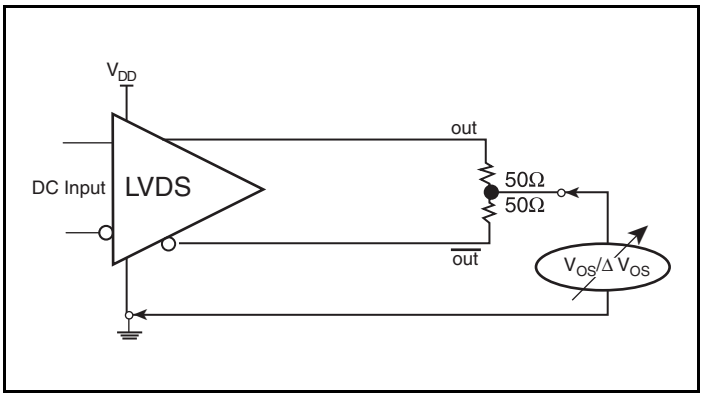
Parameter Measurement Information, continued



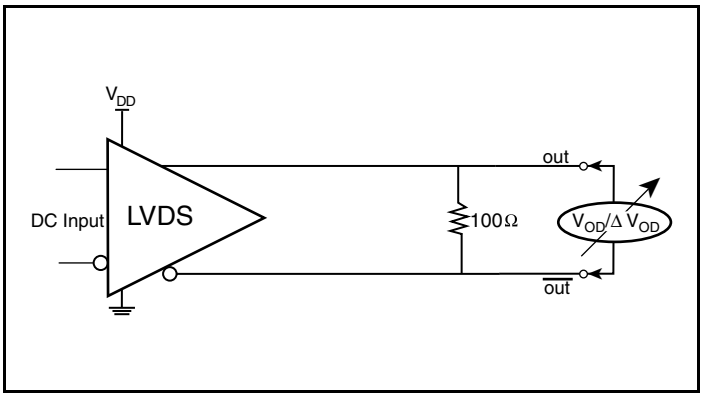
LVDS Output Rise/Fall Time



LVPECL Output Rise/Fall Time



Offset Voltage Setup



Differential Output Voltage Setup

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK Inputs

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Output

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Output

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

3.3V, 2.5V LVDS Driver Termination

A general LVDS interface is shown in *Figure 1.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input.

For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

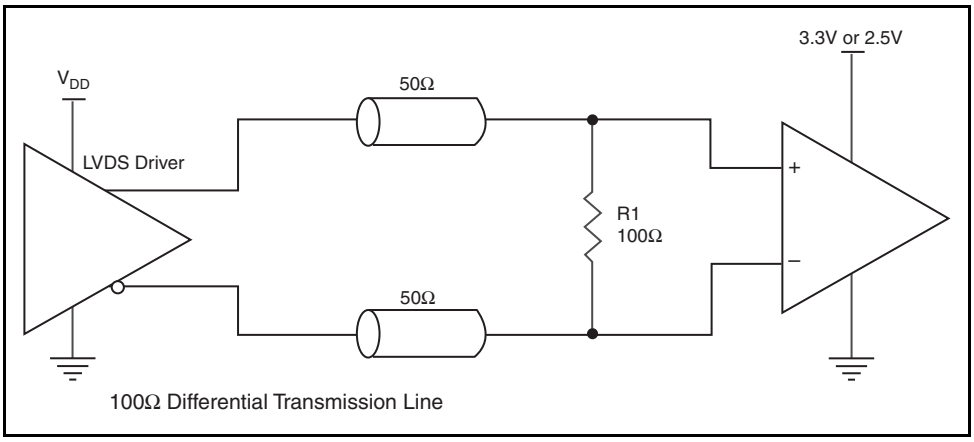


Figure 1. Typical LVDS Driver Termination

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

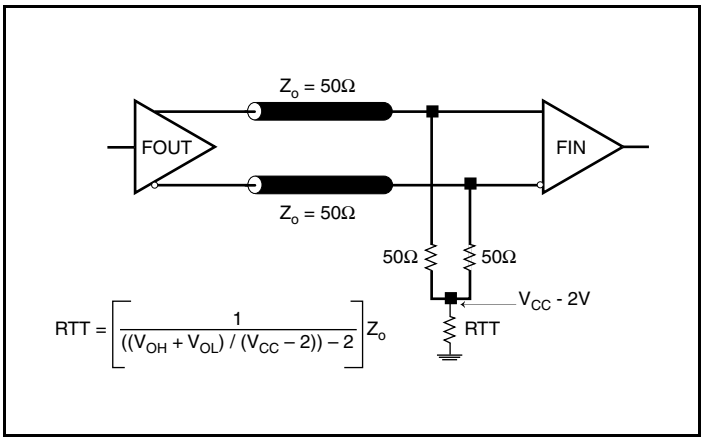


Figure 2A. 3.3V LVPECL Output Termination

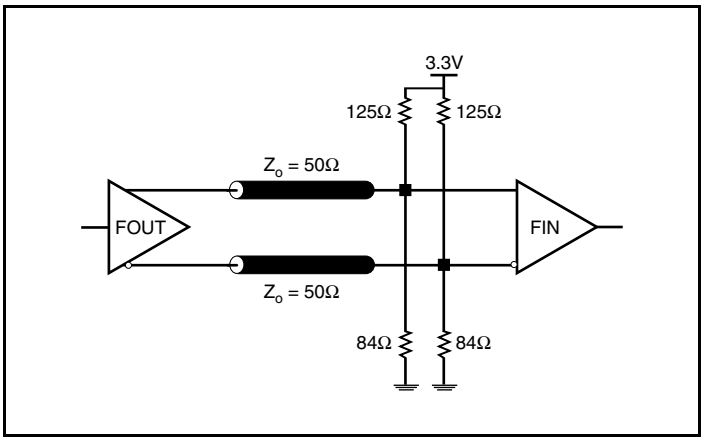


Figure 2B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 3A and *Figure 3B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 3B can be eliminated and the termination is shown in *Figure 3C.*

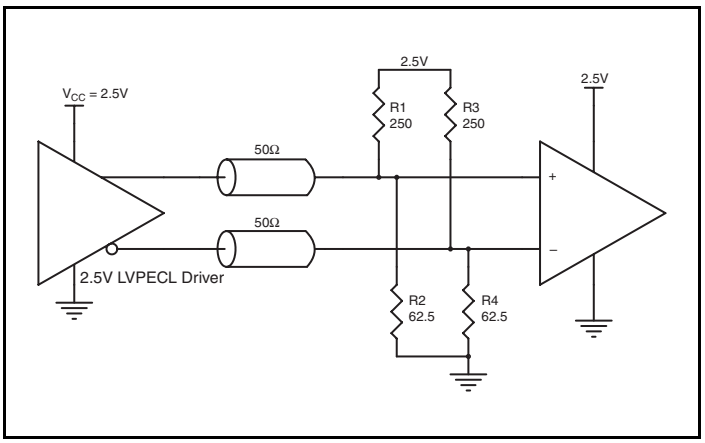


Figure 3A. 2.5V LVPECL Driver Termination Example

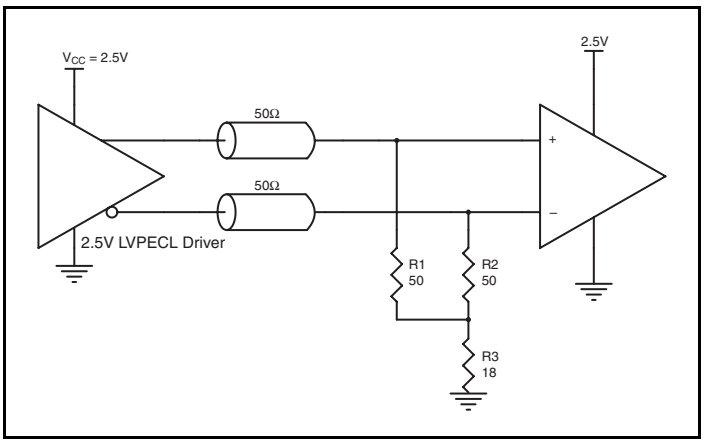


Figure 3B. 2.5V LVPECL Driver Termination Example

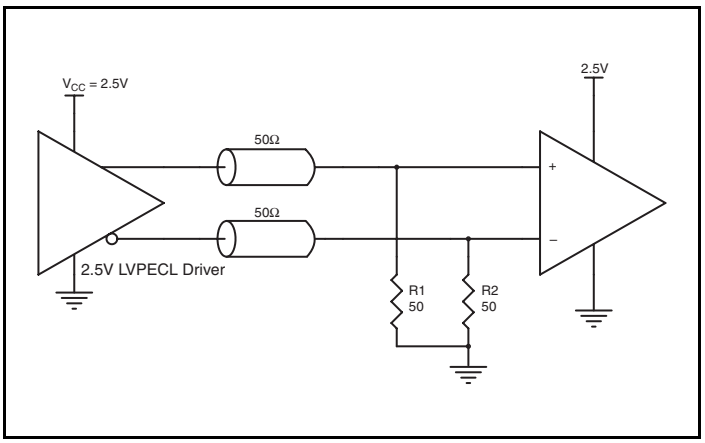


Figure 3C. 2.5V LVPECL Driver Termination Example

Power Considerations (3.3V LVPECL Outputs)

This section provides information on power dissipation and junction temperature for the ICS859S1601I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS859S1601I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 40mA = **138.6mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**

Total Power$_{\_MAX}$ (3.3V, with all outputs switching) = 138.6mW + 30mW = **168.6mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 77.1°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.169W * 77.1°C/W = 98°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 7. Thermal Resitance θ_{JA} for 28 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	77.1°C/W	69.7°C/W	65.8°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 4.*

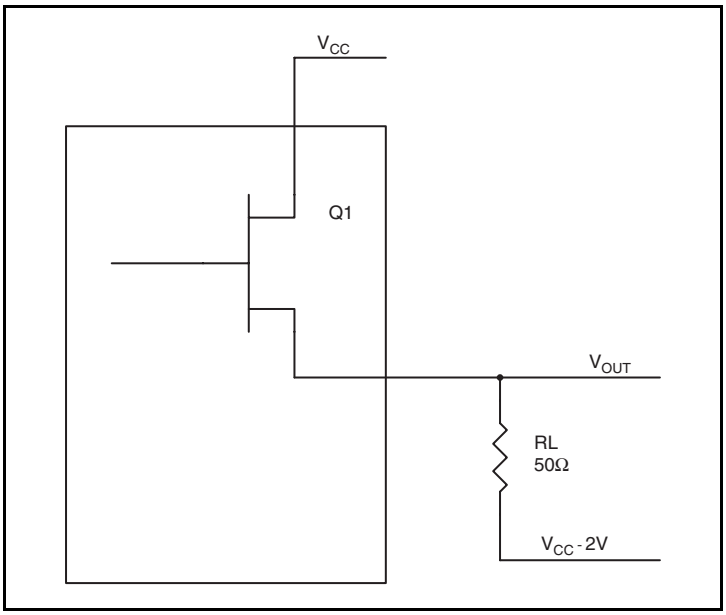


Figure 4. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **V_{CC_MAX} – 0.9V**
  ($V_{CC\_MAX} – V_{OH\_MAX}$) = **0.9V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **V_{CO_MAX} – 1.7V**
  ($V_{CC\_MAX} – V_{OL\_MAX}$) = **1.7V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

Pd_H = $[(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
[(2V – 0.9V)/50Ω] * 0.9V = **19.8mW**

Pd_L = $[(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
[(2V – 1.7V)/50Ω] * 1.7V = **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Power Considerations, (3.3V LVDS Outputs)

This section provides information on power dissipation and junction temperature for the ICS859S1601I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS859S1601I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power$_{_MAX}$ = V_{DD_MAX} * I_{EE_MAX} = 3.465V * 54mA = **187.11mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 77.1°C/W per Table 8 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.187W * 77.1°C/W = 99.4°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 8. Thermal Resistance θ_{JA} for 28 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	77.1°C/W	69.7°C/W	65.8°C/W

Reliability Information

Table 9. θ_{JA} vs. Air Flow Table for a 28 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	77.1°C/W	69.7°C/W	65.8°C/W

Transistor Count

The transistor count for ICS859S1601I is: 649

Package Outline and Package Dimensions

Package Outline - G Suffix for 28 Lead TSSOP

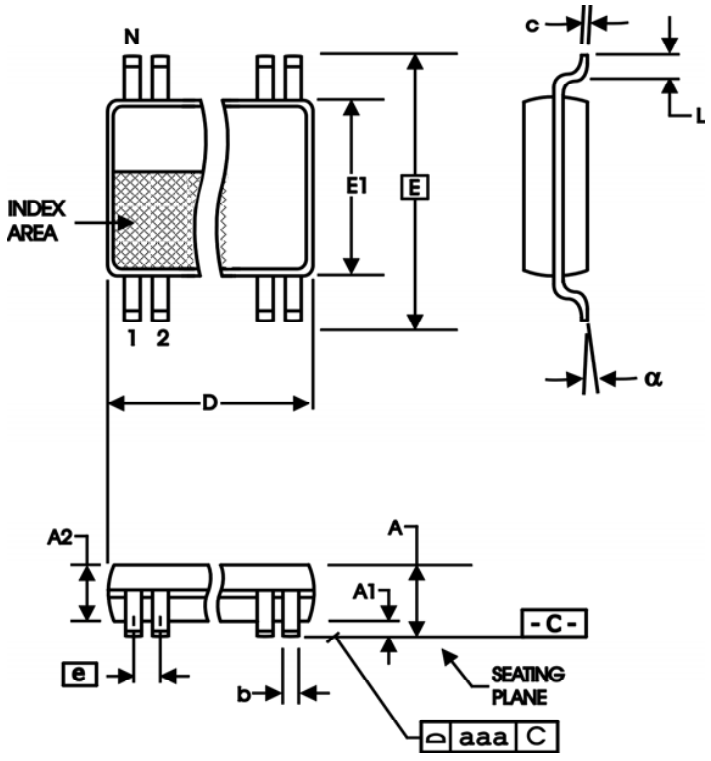


Table 10. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	28	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	9.60	9.80
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
859S1601BGI	TBD	28 Lead TSSOP	Tube	-40°C to 85°C
859S1601BGIT	TBD	28 Lead TSSOP	1000 Tape & Reel	-40°C to 85°C
859S1601BGILF	ICS859S1601BGIL	“Lead-Free” 28 Lead TSSOP	Tube	-40°C to 85°C
859S1601BGILFT	ICS859S1601BGIL	“Lead-Free” 28 Lead TSSOP	1000 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Contact Information:

www.IDT.com

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

Technical Support
netcom@idt.com
+480-763-2056

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800-345-7015 (inside USA)
+408-284-8200 (outside USA)