High Speed CMOS 8-Bit Bus Interface Register Tranceivers

QS54/74FCT646T
QS54/74FCT648T

QS54/74FCT2646T
QS54/74FCT2648T*

FEATURES/BENEFITS

- Pin and function compatible to the 74F646/8 74FCT646/8 and 74FCT646T/8T
- CMOS power levels: <7.5 mW static
- Available in DIP, SOIC, QSOP, ZIP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 646T, 648T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std, A, C, and D speed grades with 4.8 ns t_{PD} for D
- I_{OL} = 64 mA Com., 48 mA Mil.

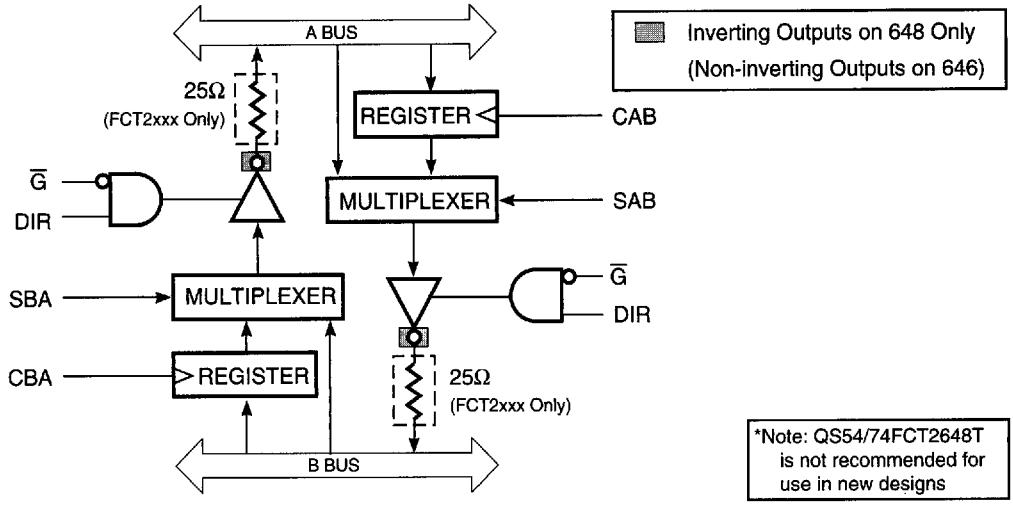
FCT-T 2646T, 2648T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std, A, C, and D speed grades with 4.8 ns t_{PD} for D
- I_{OL} = 12 mA Com.

DESCRIPTION

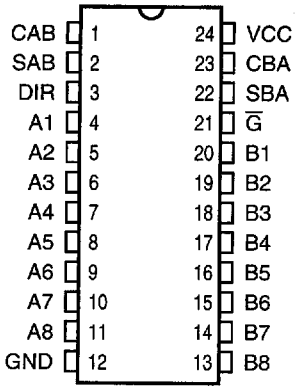
The QSFCT646T/648T and QSFCT2646T/648T are 8-bit high-speed CMOS TTL-compatible registered bus transceivers with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The 2646/8 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2646 series parts can replace the 646 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

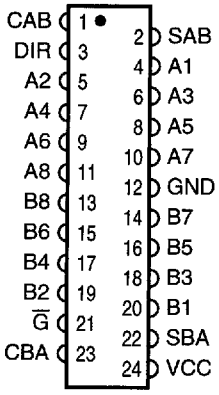


PIN CONFIGURATIONS (All Pins Top View)

PDIP, SOIC, QSOP, HQSOP



ZIP



PIN DESCRIPTION

Name	I/O	Description
A8-A1	I/O	A Bus
B8-B1	I/O	B Bus
CAB	I	Clock A to Register
CBA	I	Clock B to Register
SAB	I	A Bus or Reg to B
SBA	I	B Bus or Reg to A
DIR	I	Direction, A → B or B → A
$\overline{G}$	I	Output Enable

FUNCTION TABLE

Inputs						Outputs		Function	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A8-A1	B8-B1	646/2646	648/2648
H	—	—	—	—	—	Hi-Z	Hi-Z	Disabled	Disabled
L	L	—	—	—	—	A	Hi-Z	Output A	Output A
L	H	—	—	—	—	Hi-Z	B	Output B	Output B
—	—	↑	—	—	—	—	—	Load A Register	Load A Register
—	—	—	↑	—	—	—	—	Load B Register	Load B Register
—	—	—	—	L	—	—	—	A Bus → B Bus	$\overline{A}$ Bus → B Bus
—	—	—	—	H	—	—	—	A Reg → B Bus	$\overline{A}$ Reg → B Bus
—	—	—	—	—	L	—	—	B Bus → A Bus	$\overline{B}$ Bus → A Bus
—	—	—	—	—	H	—	—	B Reg → A Bus	$\overline{B}$ Reg → A Bus

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	−0.5V to +7.0V
DC Output Voltage V_{OUT}	−0.5V to +7.0V
DC Input Voltage V_{IN}	−0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	−3.0V
DC Input Diode Current with $V_{IN} < 0$	−20 mA
DC Output Diode Current with $V_{OUT} < 0$	−50 mA
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	−65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

CAPACITANCE

T_A = 25°C, f = 1 MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	SOIC	QSOP	PDIP	ZIP	Unit
—	4	4	5	7	pF
—	6	6	7	9	pF
1-11, 13-23	8	8	9	10	pF

Note: Capacitance is characterized but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Min	Max	Unit
Icc	Quiescent Power Supply Current	Vcc = Max., freq = 0 0V ≤ V_{IN} ≤ 0.2V or Vcc-0.2V ≤ V_{IN} ≤ Vcc	—	1.5	mA
ΔIcc	Supply Current per Input @ TTL HIGH	Vcc = Max., V_{IN} = 3.4V, freq = 0[2]	—	2.0	mA
Q_{CCD}	Supply Current per Input per MHz	Vcc = Max., Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or Vcc[3,4]	—	0.25	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% Military T_A = –55°C to 125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$	Input Current Input HIGH or LOW	V_{CC} = Max., $0 \le V_{IN} < V_{CC}$	—	—	5	µA
$\lvert I_{OZ} \rvert$	Off-State Output Current (Hi-Z)	V_{CC} = Max., $0 \le V_{IN} \le V_{CC}$	—	—	5	µA
I_{OS}	Short Circuit Current (FCTXXX)	V_{CC} = Max., V_{OUT} = GND(2,3)	–60	—	—	mA
I_{OR}	Current Drive (FCT2XXX)	V_{CC} = Max., V_{OUT} = 2.0V(3)	50	—	—	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18 mA, T_A = 25°C(3)	—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min. I_{OH} = –12 mA (MIL) I_{OH} = –15 mA (COM)	2.4 2.4	— —	— —	V
V_{OL}	Output LOW Voltage (FCTXXX)	V_{CC} = Min. I_{OL} = 48 mA (MIL) I_{OL} = 64 mA (COM)	— —	— —	0.55 0.55	V
V_{OL}	Output LOW Voltage (FCT2XXX- 25Ω)	V_{CC} = Min. I_{OL} = 12 mA (MIL) I_{OL} = 12 mA (COM)	— —	— —	0.50 0.50	V
R_{OUT}	Output Resistance (FCT2XXX- 25Ω)	V_{CC} = Min. I_{OL} = 12 mA (MIL) I_{OL} = 12 mA (COM)	— 20	25 28	— 40	Ω

Notes:
1. Typical values indicate Vcc = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, Vcc = 5.0V ± 5% Military T_A = –55°C to 125°C, Vcc = 5.0V ± 10%
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]		646 2646 Min	646 2646 Max	646A 2646A Min	646A 2646A Max	646C 2646C Min	646C 2646C Max	646D 2646D Min	646D 2646D Max	Unit
t_{PHLB}	Bus to Bus	Com	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.8	ns
t_{PLHB}	Delay, 646	Mil	2.0	11	2.0	7.7	1.5	6.0	—	—	
t_{PHLB}	Bus to Bus	Com	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.8	ns
t_{PLHB}	Delay, 2646	Mil	2.0	11	2.0	7.7	1.5	6.0	—	—	
t_{PZH}	Ouput Enable	Com	2.0	14	2.0	9.8	1.5	7.8	1.5	7.3	ns
t_{PZL}	Time, 646	Mil	2.0	15	2.0	10.5	1.5	8.9	—	—	
t_{PZH}	Output Enable	Com	2.0	14	2.0	9.8	1.5	7.8	1.5	7.3	ns
t_{PZL}	Time, 2646	Mil	2.0	15	2.0	10.5	1.5	8.9	—	—	
t_{PHZ}	Output Disable	Com[2]	2.0	9.0	2.0	6.3	1.5	6.3	1.5	6.3	ns
t_{PLZ}	Time	Mil[2]	2.0	11	2.0	7.7	1.5	7.7	—	—	
t_{PHLC}	Clock to Bus	Com	2.0	9.0	2.0	6.3	1.5	5.7	1.5	5.2	ns
t_{PLHC}	Delay, 646	Mil	2.0	10	2.0	7.0	1.5	6.3	—	—	
t_{PHLC}	Clock to Bus	Com	2.0	9.0	2.0	6.3	1.5	5.7	1.5	5.2	ns
t_{PLHC}	Delay, 2646	Mil	2.0	10	2.0	7.0	1.5	6.3	—	—	
t_{PHLS}	SBA/SAB to Bus	Com	2.0	11	2.0	7.7	1.5	6.2	1.5	5.8	ns
t_{PLHS}	Delay, 646	Mil	2.0	12	2.0	8.4	1.5	7.0	—	—	
t_{PHLS}	SBA/SAB to Bus	Com	2.0	11	2.0	7.7	1.5	6.2	1.5	5.8	ns
t_{PLHS}	Delay, 2646	Mil	2.0	12	2.0	8.4	1.5	7.0	—	—	
t_S	Data Setup Time	Com	4.0	—	2.0	—	2.0	—	2.0	—	ns
		Mil	4.5	—	2.0	—	2.0	—	—	—	
t_H	Data Hold Time	Com	2.0	—	1.5	—	1.5	—	1.5	—	ns
		Mil	2.0	—	1.5	—	1.5	—	—	—	
t_{PWH}	Clock Pulse Width	Com[2]	6.0	—	5.0	—	5.0	—	5.0	—	ns
t_{PWL}	HIGH or LOW	Mil[2]	6.0	—	5.0	—	5.0	—	—	—	

Notes:
1. Minimums guaranteed but not tested for all parameters except t_S and t_H.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.

TIMING REQUIREMENTS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, Vcc = 5.0V ± 5% Military T_A = –55°C to 125°C, Vcc = 5.0V ± 10%
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]		648 2648 Min	648 2648 Max	648A 2648A Min	648A 2648A Max	648C 2648C Min	648C 2648C Max	Unit
t_{PHLB}	Bus to Bus	Com	2.0	8.0	2.0	5.6	1.5	5.4	ns
t_{PLHB}	Delay, 648	Mil	2.0	9.0	2.0	6.3	1.5	6.0	
t_{PHLB}	Bus to Bus	Com	2.0	8.0	2.0	5.6	1.5	5.4	ns
t_{PLHB}	Delay, 2648	Mil	2.0	9.0	2.0	6.3	1.5	6.0	
t_{PZH}	Ouput Enable	Com	2.0	15	2.0	10.5	1.5	7.8	ns
t_{PZL}	Time, 648	Mil	2.0	18	2.0	12.6	1.5	8.9	
t_{PZH}	Output Enable	Com	2.0	15	2.0	10.5	1.5	7.8	ns
t_{PZL}	Time, 2648	Mil	2.0	18	2.0	12.6	1.5	8.9	
t_{PHZ}	Output Disable	Com[2]	2.0	9.0	2.0	6.3	1.5	6.3	ns
t_{PLZ}	Time	Mil[2]	2.0	11	2.0	7.7	1.5	7.7	
t_{PHLC}	Clock to Bus	Com	2.0	9.0	2.0	6.3	1.5	5.7	ns
t_{PLHC}	Delay, 648	Mil	2.0	10	2.0	7.0	1.5	6.3	
t_{PHLC}	Clock to Bus	Com	2.0	9.0	2.0	6.3	1.5	5.7	ns
t_{PLHC}	Delay, 2648	Mil	2.0	10	2.0	7.0	1.5	6.3	
t_{PHLS}	SBA/SAB to Bus	Com	2.0	11	2.0	7.7	1.5	6.2	ns
t_{PLHS}	Delay, 648	Mil	2.0	12	2.0	8.4	1.5	7.0	
t_{PHLS}	SBA/SAB to Bus	Com	2.0	11	2.0	7.7	1.5	6.2	ns
t_{PLHS}	Delay, 2648	Mil	2.0	12	2.0	8.4	1.5	7.0	
t_S	Data Setup Time	Com	4.0	—	2.0	—	2.0	—	ns
		Mil	4.5	—	2.0	—	2.0	—	
t_H	Data Hold Time	Com	2.0	—	1.5	—	1.5	—	ns
		Mil	2.0	—	1.5	—	1.5	—	
t_{PWH}	Clock Pulse Width	Com[2]	6.0	—	5.0	—	5.0	—	ns
t_{PWL}	HIGH to LOW	Mil[2]	6.0	—	5.0	—	5.0	—	

Notes:
1. Minimums guaranteed but not tested for all parameters except ts and t_H.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.