MAX22195

High-Speed, Octal, Industrial Digital Input with Parallel Output

General Description

The MAX22195 translates eight 24V industrial digital inputs to eight CMOS-compatible, parallel outputs. Propagation delay from input-to-output is less than 300ns for all channels. Current-limiters on each digital input greatly reduce power dissipation compared to traditional resistive inputs. The accuracy of these current-limiters minimizes power dissipation while ensuring compliance with the IEC 61131-2 standard. A current-setting resistor allows the MAX22195 to be configured for Type 1, Type 2, or Type 3 inputs. Additionally, the MAX22195 has energyless field-side LED drivers to meet the indicator light requirement of IEC 61131-2 with no additional power dissipation.

The MAX22195 provides a 3.3V integrated voltage regulator. The internal LDO accepts the field supply V_{DD24} from 7V to 65V. The internal LDO output can supply up to 25mA of current in addition to powering the basic MAX22195 requirements. This MAX22195 LDO current can be used to power digital isolators and other field-side circuits. Alternatively, the MAX22195 can be powered from a 3.0V to 5.5V supply connected to V_{DD3} pin.

The MAX22195 includes an open-drain READY output that asserts high to indicate the MAX22195 is functional. If the V_{DD24} field-side supply voltage is too low, or a fault in the current-setting resistor is detected, or the device reaches an over-temperature condition, the READY signal is set to high-impedance.

Applications

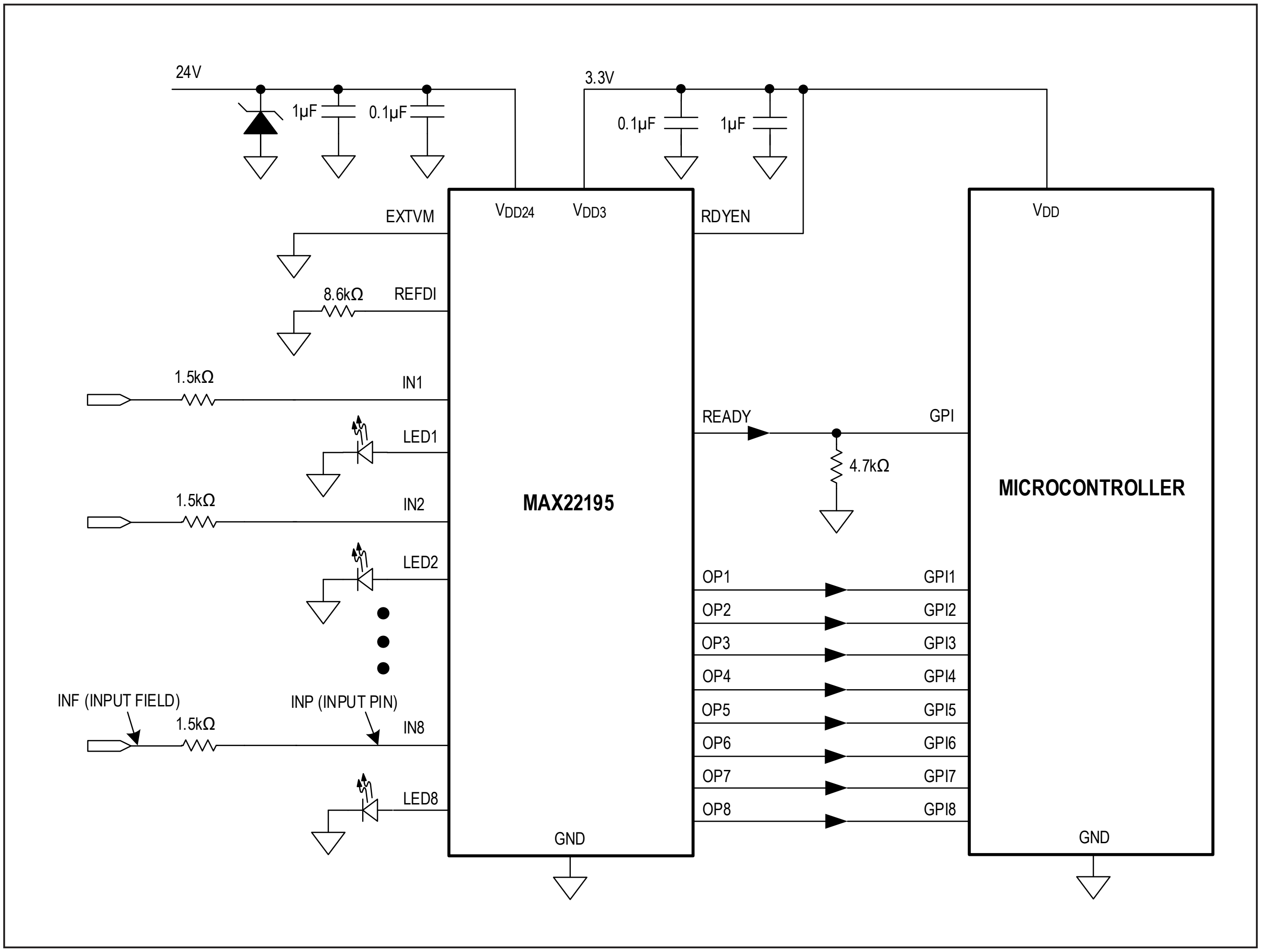
- Programmable Logic Controllers
- Industrial Automation
- Process Automation
- Building Automation

Benefits and Features

- High-Speed, Industrial Digital Inputs
  - 300ns Maximum Propagation Delay
  - ±10ns Maximum Channel-to-Channel Skew
  - Parallel Output for Simultaneous Signal Delivery
- High Integration Reduces BOM Count and Board Space
  - Operates Directly from Field Supply (7V to 65V)
  - Compatible with 3.3V or 5V Logic
  - 5mm x 5mm, 32-TQFN Package
- Low Power and Low Heat Dissipation
  - Low Quiescent Current (1.2mA Maximum)
  - Accurate Input Current-Limiters
  - Energyless Field-Side LED Drivers
- Fault Tolerant with Built-In Diagnostics
  - Integrated Field-Side Supply Monitor
  - Integrated Over-Temperature Monitor
  - Current-Setting Resistor Monitor
- Configurability Enables Wide Range of Applications
  - Configurable IEC 61131-2 Types 1, 2, 3 Inputs
  - Configurable Input Current Limiting from 0.56mA to 3.97mA
- Robust Design
  - ±1kV Surge Tolerant using Minimum 1kΩ Resistor
  - ±8kV Contact ESD and ±15kV Air Gap ESD Using Minimum 1kΩ Resistor
  - -40°C to +125°C Ambient Operating Temperature

***Ordering Information** appears at end of data sheet.*

Octal Digital Input with Parallel Output



Absolute Maximum Ratings

V_{DD3} to GND ....-0.3V to +6V
V_{DD24} to GND..-0.3V to +70V
OP1–OP8 ....-0.3V to V_{DD3} + 0.3V
IN1–IN8 to GND ....-40V to +40V
REFDI to GND..-0.3V to V_{DD3} + 0.3V
READY, RDYEN to GND..-0.3V to +6V
EXTVM to GND..-0.3V to +6V
LED1–LED8 to GND ....-0.3V to +6V

Continuous Power Dissipation
Multilayer Board T_A = +70°C....................................2222mW
Derate above +70°C..27.80mW/°C
Operating Temperature Range......................................+125°C
Maximum Junction Temperature ....+150°C
Storage Temperature Range........................... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering(reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 32 TQFN	
Package Code	T3255+6
Outline Number	21-0140
Land Pattern Number	90-0603
THERMAL RESISTANCE, MULTILAYER BOARD	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	3°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

V_{DD3} to GND = +3.0V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. C_L on OP1-OP8 = 15pF. Typical values are at V_{DD3} to GND = +3.3V, V_{DD24} to GND = +24V, Field Inputs IN1-IN8 = +24V, and T_A = +25°C. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Supply Voltage	V_{DD24}	Normal operation	7		65	V
	V_{DD3}	Powered from an external power supply	3.0		5.5	V
Supply Current Powered from V_{DD24}	I_{DD24}	V_{DD24} = 24V, IN1-IN8 = 0V, LED_ = GND, no load on OP1-OP8		0.6	1.2	mA
Supply Current Powered from V_{DD3}	I_{DD3}	V_{DD3} = 3.3V, IN1-IN8 = 0V, LED_ = GND, no load on OP1-OP8, V_{DD24} floating		0.6	1.2	mA
V_{DD3} Undervoltage-Lockout Threshold	V_{UVLO3}	Powered from V_{DD3}, V_{DD3} rising V_{DD24} floating	2.4		2.9	V
V_{DD3} Undervoltage-Lockout Threshold Hysteresis	$V_{UVHYST3}$			0.07		V
V_{DD24} READY Threshold	V_{READY_24VR}	V_{DD24} rising, EXTVM = GND	13.8	14.6	15.4	V
	V_{READY_24VF}	V_{DD24} falling, EXTVM = GND	13.3	14.1	15.0	V
V_{DD24} Undervoltage-Lockout Threshold	V_{UVLO24}	V_{DD24} rising	6.0		6.8	V
V_{DD24} Undervoltage-Lockout Threshold Hysteresis	$V_{UVHYST24}$			0.45		V
Regulator Output Voltage	V_{DD3}	I_{LOAD} = 1mA, V_{DD24} = 7V to 65V	3.0	3.3	3.6	V
Line Regulation	dV_{DDLINE}	I_{LOAD} = 1mA, V_{DD24} = 12V to 24V		0		mV
Load Regulation	dV_{DDLOAD}	I_{LOAD} = 1mA to 10mA, V_{DD24} = 12V		1		mV
Short-Circuit Current Limit	I_{DD24_SC}	V_{DD24} current when V_{DD3} short to GND, V_{DD24} = 12V	28	37.5	50	mA
VDD24 MONITOR						
EXTVM Glitch Filter				3		µs
EXTVM Threshold Off to On	$V_{24TH\_OFF\_ON}$	V_{DD24} rising	0.77	0.81	0.84	V
EXTVM Threshold On to Off	$V_{24TH\_ON\_OFF}$	V_{DD24} falling	0.74	0.79	0.82	V
External EXTVM Selection Threshold	EXTVM_SEL			0.3		V
External EXTVM Selectable V_{DD24} Threshold	EXTVM_VDD24		10		30	V
EXTVM Leakage Current	I_{EXTVM_L}		-1		1	µA
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold	T_{SHDN}	V_{DD3} internal regulator off		165		°C
Thermal-Shutdown Hysteresis	T_{SHDN_HYS}			10		°C

DC Electrical Characteristics (continued)

V_{DD3} to GND = +3.0V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. C_L on OP1-OP8 = 15pF. Typical values are at V_{DD3} to GND = +3.3V, V_{DD24} to GND = +24V, Field Inputs IN1-IN8 = +24V, and T_A = +25°C. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT LIMITING SETTING						
REFDI Voltage	V_{REFDI}			0.61		V
Current-Limit Setting Resistor	R_{REFDI}		5.2	8.6	36	kΩ
REFDI Pin Short	REFDI_S	Increasing current at pin REFDI		550		µA
		Decreasing current at pin REFDI		548		µA
REFDI Pin Open	REFDI_O	Increasing current at pin REFDI		4.46		µA
		Decreasing current at pin REFDI		7.21		µA
IC INPUTS (TYPE 1, 2, 3)						
Input Current Limit		-40V < $V_{IN\_}$ < 0V, $V_{IN\_}$ at IN1 - IN8 pins		100		µA
LED On-State Current	I_{LED_ON}	R_{REFDI} = 8.6kΩ, V_{LED} = 3V	1.5			mA
DI Leakage, Current Sources Disabled	I_{DI_LEAK}	IN1 – IN8 = 28V	40	58	80	µA
		IN1 – IN8 = 6V	8	11.4	16	
Input Threshold Low-to-High	V_{THP+}	IN1 – IN8		5.6	6	V
Input Threshold High-to-Low	$V_{THP\_}$	IN1 – IN8	4.4	4.7		V
Input Threshold Hysteresis	$V_{INPHYST}$	IN1 – IN8		0.9		V
FIELD INPUTS TYPE 1, 3: (EXTERNAL SERIES RESISTOR R_{IN} = 1.5KΩ, R_{REFDI} = 8.6KΩ)						
Field-Input Current Limit	I_{INLIM}	6V (V_{THP+} MAX) ≤ VIN_ at the pin ≤ 28V, LED on, R_{REFDI} = 8.6kΩ (Note 2)	2.15	2.40	2.65	mA
Field Input Threshold Low-to-High	V_{INF+}	R_{REFDI} = 8.6kΩ, 1.5kΩ external series resistor			10	V
Field Input Threshold High-to-Low	V_{INF-}	R_{REFDI} = 8.6kΩ, 1.5kΩ external series resistor	8			V
FIELD INPUTS TYPE 2: (EXTERNAL SERIES RESISTOR R_{IN} = 1KΩ , R_{REFDI} = 5.2KΩ)						
Field-Input Current Limit	I_{INLIM}	6V (V_{THP+} MAX) ≤ VIN_ at the pin ≤ 28V, LED on, R_{REFDI} = 5.2kΩ (Note 2)	3.55	3.97	4.39	mA
Field Input Threshold Low-to-High	V_{INF+}	R_{REFDI} = 5.2kΩ, 1kΩ external series resistor			10	V
Field Input Threshold High-to-Low	V_{INF-}	R_{REFDI} = 5.2kΩ, 1kΩ external series resistor	8			V
LOGIC INPUT (RDYEN)						
Input Logic-High Voltage	V_{IH}		0.7 x V_{DD3}			V
Input Logic-Low Voltage	V_{IL}				0.3 x V_{DD3}	V
Input Pulldown Resistance	R_{PD}			199		kΩ

DC Electrical Characteristics (continued)

V_{DD3} to GND = +3.0V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. C_L on OP1-OP8 = 15pF. Typical values are at V_{DD3} to GND = +3.3V, V_{DD24} to GND = +24V, Field Inputs IN1-IN8 = +24V, and T_A = +25°C. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC OUTPUT (OP1-OP8, READY)						
Output Logic-High Voltage	V_{OH}	Sourcing 4mA	V_{DD3} - 0.4			V
Output Logic-Low Voltage	V_{OL}	Sinking 4mA			0.4	V
DYNAMIC CHARACTERISTICS (OP1-OP8)						
Propagation Delay Low-to-High (Figure 1)	t_{PDLH}	IN_ to OP_, R_{IN} = 1.5kΩ, IN_ = 11V and 36V			300	ns
Propagation Delay High-to-Low (Figure 1)	t_{PDHL}	IN_ to OP_, R_{IN} = 1.5kΩ, IN_ = 11V and 36V			300	ns
Propagation Delay Skew Channel-to-Channel (Figure 1)	t_{PDSKEW_CH}	IN_ to OP_, R_{IN} = 1.5kΩ, IN_ = 11V and 36V	-10		10	ns
Propagation Delay Skew Part-to-Part (Figure 1)	t_{PDSKEW_PART}	IN_ to OP_, R_{IN} = 1.5kΩ, IN_ = 11V and 36V, All conditions are the same between parts	-200		+200	ns
Propagation Delay Jitter	t_{PDJ_R}	Output Rising, V_{DD3} = 3.3V, IN_ = 24V		40		ps
	t_{PDJ_F}	Output Falling, V_{DD3} = 3.3V, IN_ = 24V		50		ps
Detectable Pulse Width (Figure 1)	t_{PW}	IN_ to OP_, R_{IN} = 1.5kΩ, IN_ = 11V and 36V	220			ns
Pulse Width Distortion	PWD	$\lvert t_{PDLH} - t_{PDHL} \rvert$	0		180	ns

Note 1: All units are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: External resistor REFDI is selected to set any desired current limit between 0.56mA to 3.97mA (typical values). The current limit accuracy of ±10.6% is guaranteed for values greater or equal to 2mA.

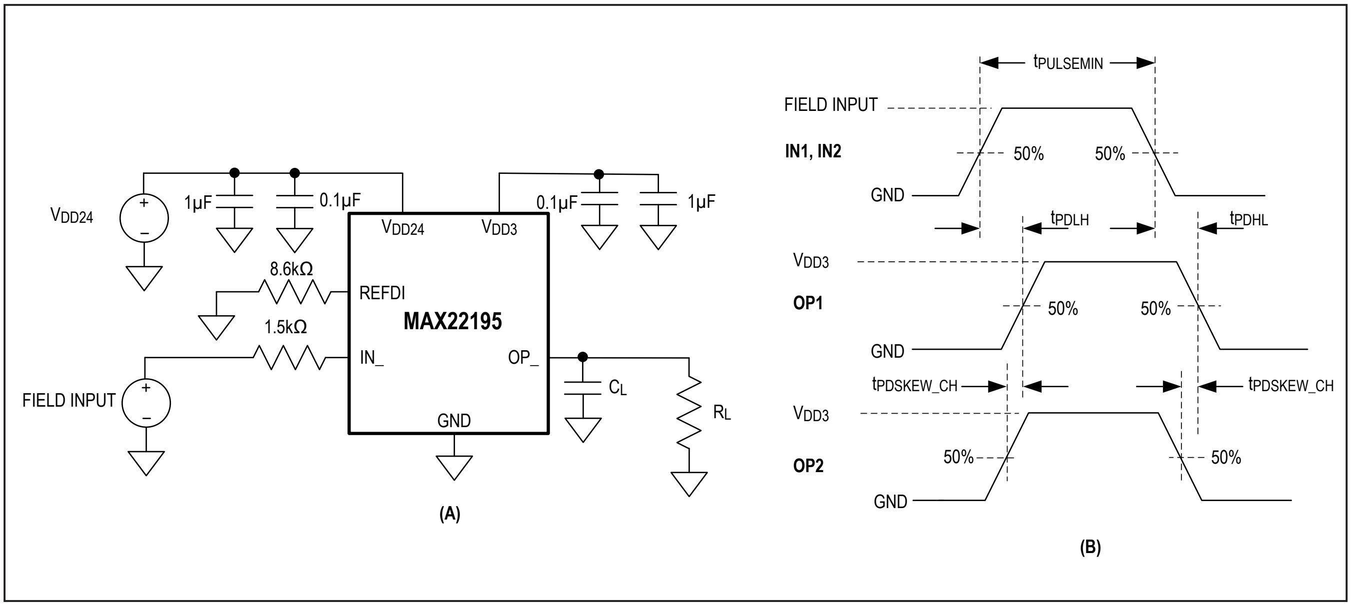


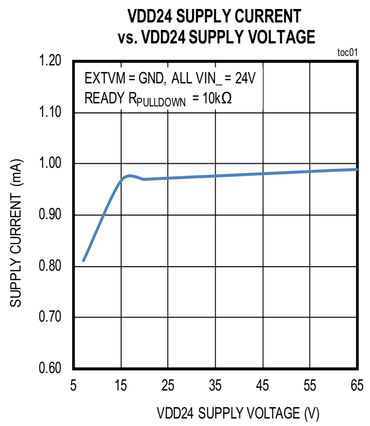
Figure 1. Test Circuit (A) and Timing Diagram (B)

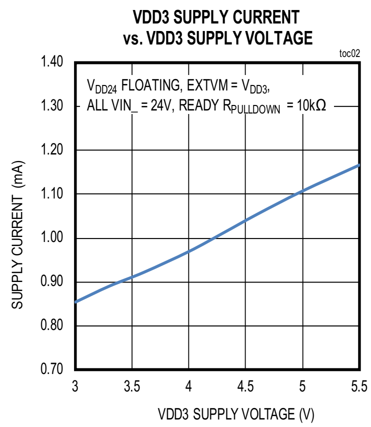
ESD and EMC Characteristics

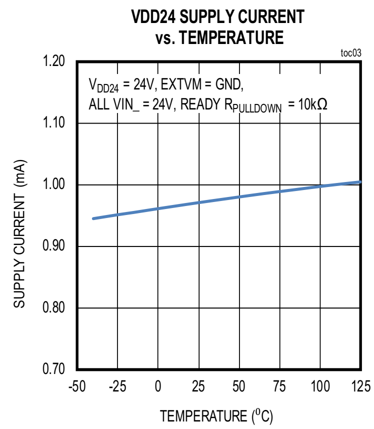
PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Surge	Line-to-Line	IEC 61000-4-5, 1.2/50µs pulse, minimum 1kΩ resistor in series with IN1–IN8	±2	kV
	Line-to-Ground	IEC 61000-4-5, 1.2/50µs pulse, minimum 1kΩ resistor in series with IN1–IN8	±1	
ESD	Human Body Model	All Pins	±2	
	Contact Discharge	IEC 61000-4-2, minimum 1kΩ resistor in series with IN1–IN8	±8	
	Air-Gap Discharge	IEC 61000-4-2, minimum 1kΩ resistor in series with IN1–IN8	±15	

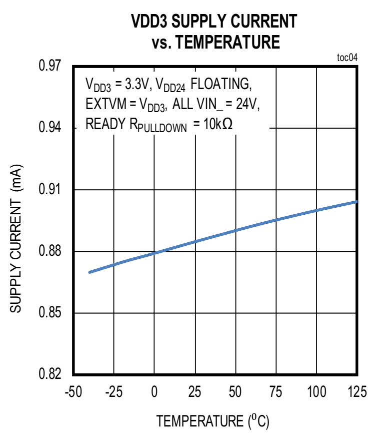
Typical Operating Characteristics

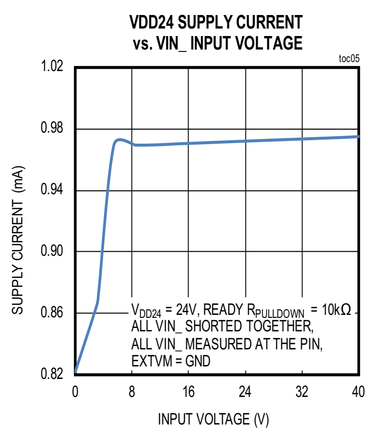
(V_{DD24} = 24V, V_{DD3} = 3.3V, T_A = +25°C, R_{REFDI} = 8.6kΩ or 5.2kΩ, R_{IN} = 1.5kΩ or 1kΩ, unless otherwise noted.)

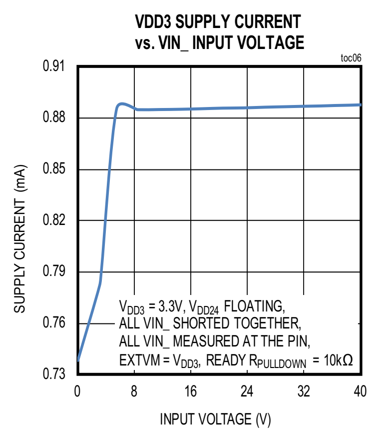


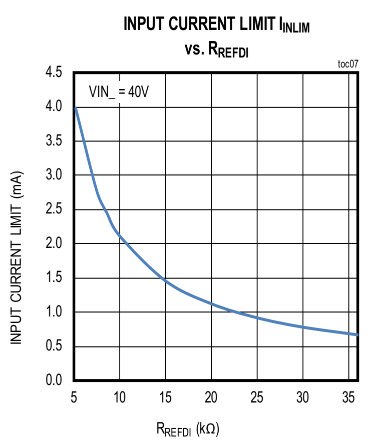


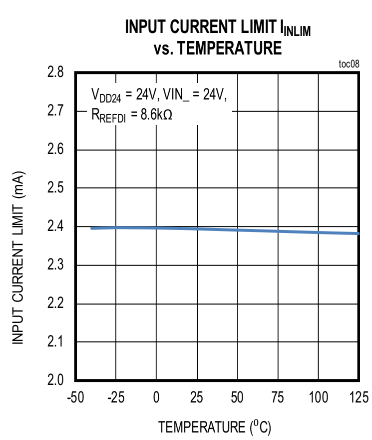


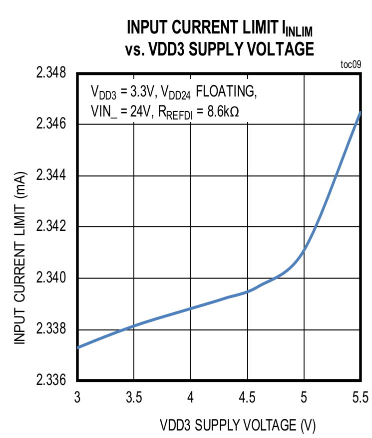






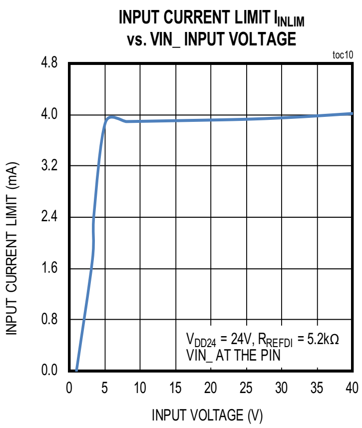


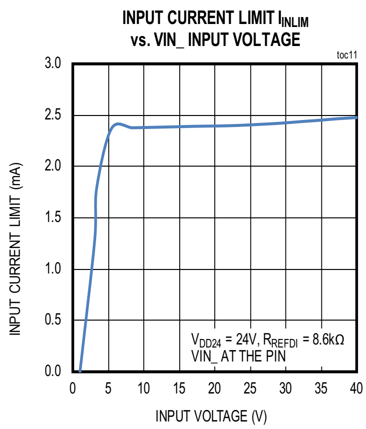


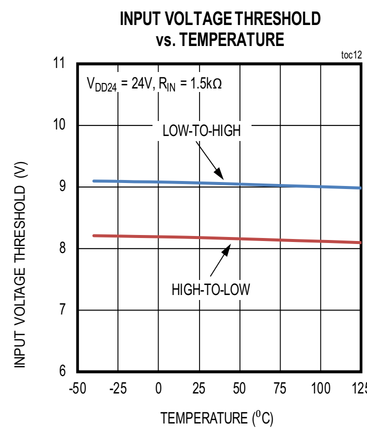


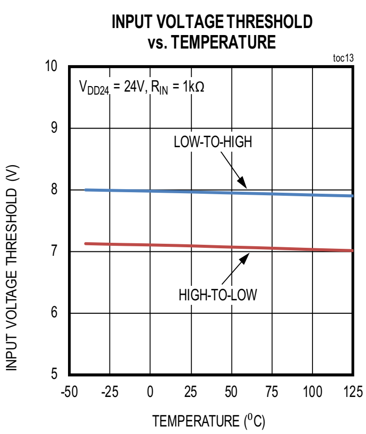
Typical Operating Characteristics (continued)

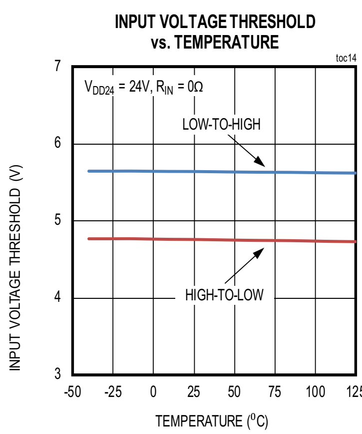
(V_{DD24} = 24V, V_{DD3} = 3.3V, T_A = +25°C, R_{REFDI} = 8.6kΩ or 5.2kΩ, R_{IN} = 1.5kΩ or 1kΩ, unless otherwise noted.)

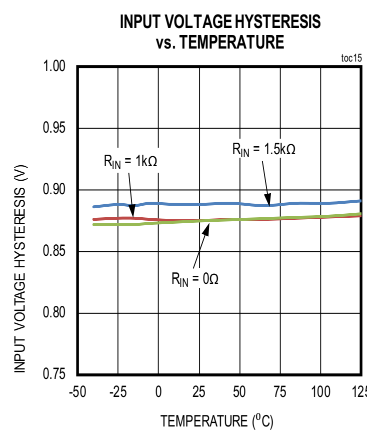


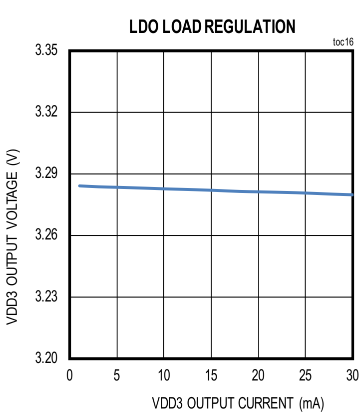


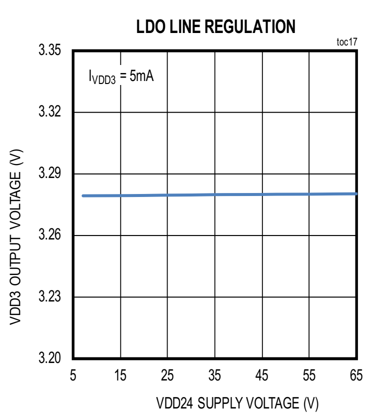


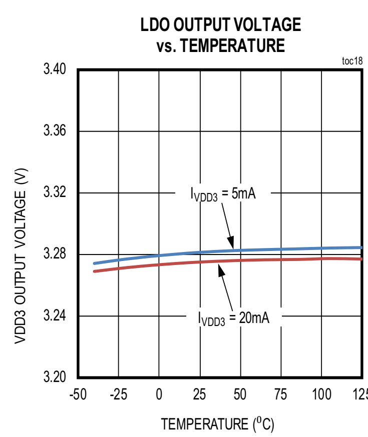








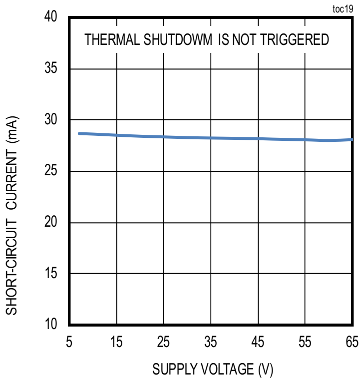




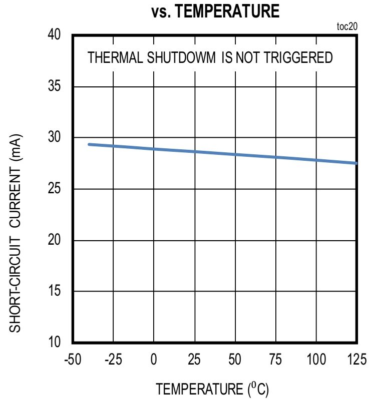
Typical Operating Characteristics (continued)

(V_{DD24} = 24V, V_{DD3} = 3.3V, T_A = +25°C, R_{REFDI} = 8.6kΩ or 5.2kΩ, R_{IN} = 1.5kΩ or 1kΩ, unless otherwise noted.)

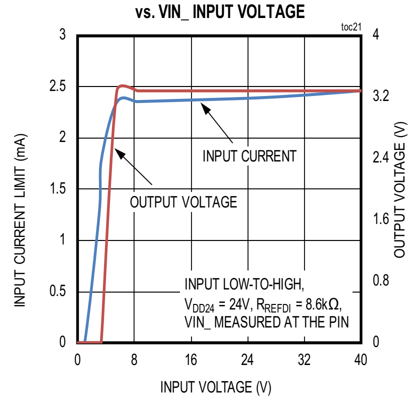
LDO SHORT-CIRCUIT CURRENT vs. VDD24 SUPPLY VOLTAGE



LDO SHORT-CIRCUIT CURRENT vs. TEMPERATURE



INPUT CURRENT LIMIT I_{INLIM} AND OUTPUT VOLTAGE vs. VIN_ INPUT VOLTAGE



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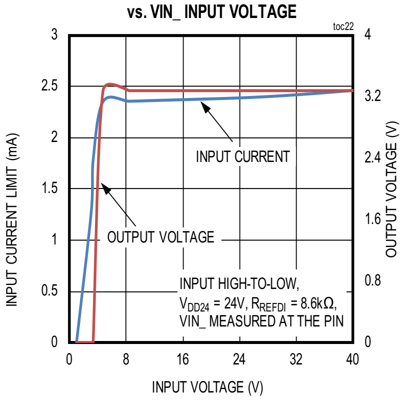
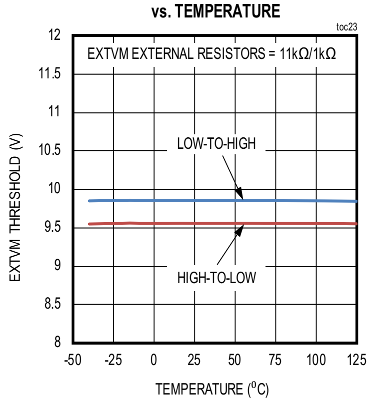
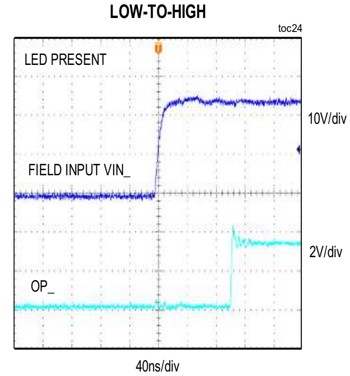


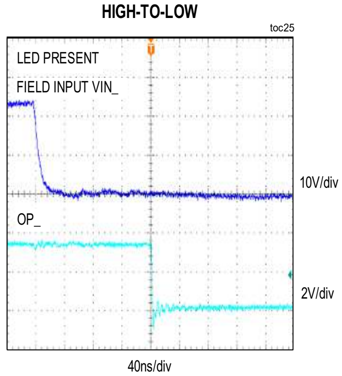
EXTVM THRESHOLD VOLTAGE vs. TEMPERATURE



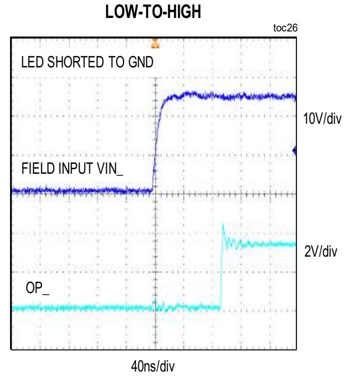
PROPAGATION DEALY LOW-TO-HIGH



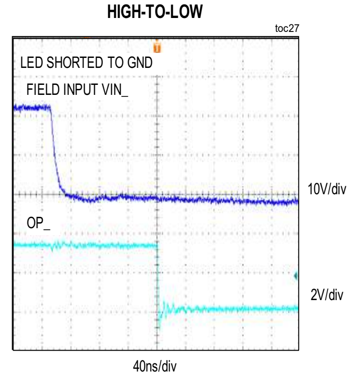
PROPAGATION DEALY HIGH-TO-LOW



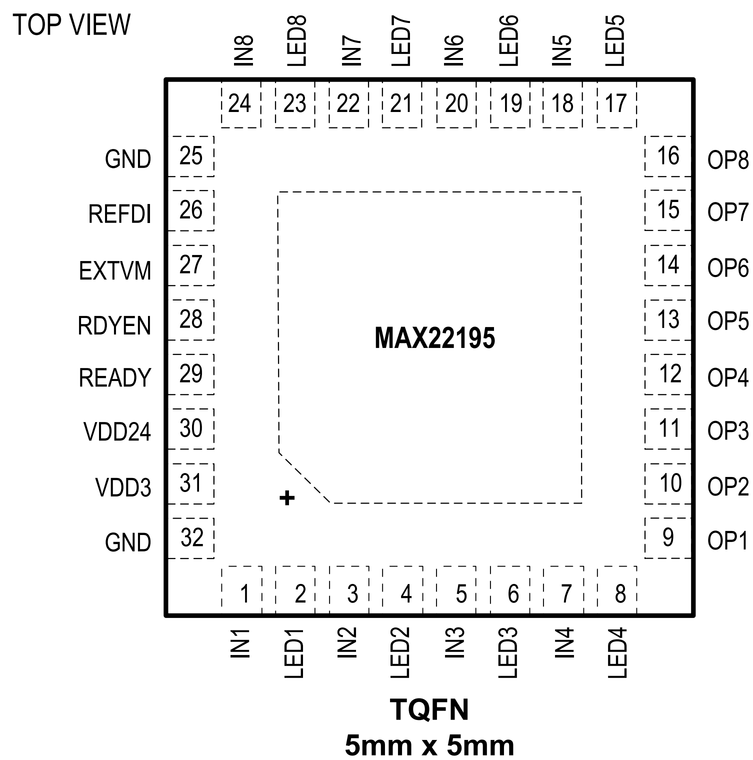
PROPAGATION DEALY LOW-TO-HIGH



PROPAGATION DEALY HIGH-TO-LOW



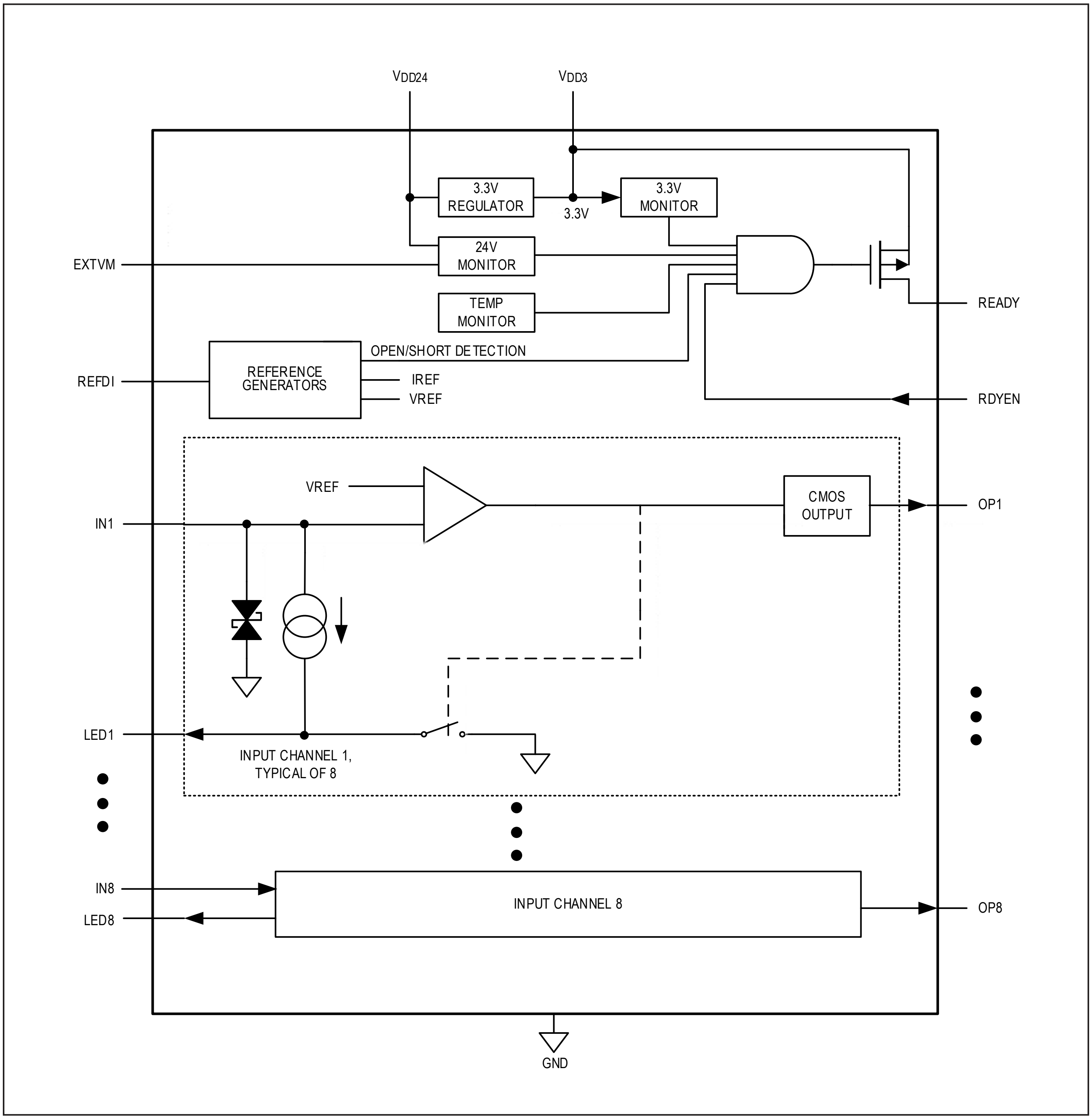
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
POWER SUPPLY		
30	V_{DD24}	24V Field Supply. Bypass to GND with 0.1μF capacitor in parallel with 1μF capacitor.
31	V_{DD3}	3.3V output from integrated LDO when powered from V_{DD24}, or 3.0 - 5.5V supply input when V_{DD24} not driven. Bypass to GND with 0.1μF capacitor in parallel with 1μF capacitor. If powering V_{DD3} from an external supply, leave V_{DD24} floating. V_{DD3} output is turned off during thermal shutdown.
25, 32	GND	Ground Return for All Signals and the Power Supplies
EP	-	Exposed Pad. Connect to GND. Solder entire exposed pad area to ground plane with multiple vias for best thermal performance. EP = exposed pad on the back of the package
ANALOG PINS		
27	EXTVM	Connect EXTVM to GND to use internal thresholds (14V, typical) for V_{DD24} voltage monitoring. Connect EXTVM to external resistive divider to set external thresholds for V_{DD24} voltage monitoring. Connect EXTVM to V_{DD3} to disable V_{DD24} voltage monitoring at READY pin if the device is powered by V_{DD3}.
26	REFDI	Digital Input Current-Limit Reference Resistor. For 24V Type 1 and Type 3 inputs, place a 8.6kΩ resistor from REFDI to GND. For Type 2 inputs, place a 5.2kΩ resistor from REFDI to GND.
INPUT PINS		
1,3,5,7,18, 20,22,24	IN1-IN8 respectively	Field Inputs. For 24V Type 1 and Type 3 inputs, place a 1.5kΩ resistor between the field input and IN_ pin. For Type 2 inputs, place a 1kΩ resistor between the field input and IN_ pin. Capacitors for filtering should not be connected to the IN_ pins. See the *Surge Protection of Field Inputs* section for further information.
2,4,6,8,17, 19,21,23	LED1-LED8 respectively	Energyless LED Driver Outputs. Connect to GND if LEDs are not used.
LOGIC PINS		
9,10,11,12, 13,14,15,16	OP1-OP8 respectively	Logic Outputs. Indicate the state (high or low) of IN1-IN8. High level is V_{DD3}. Low level is GND. If thermal shutdown is triggered, OP1-OP8 are high-impedance.
28	RDYEN	Ready Enable. Has a weak internal pulldown. Assert high to enable the READY output. Cascade the READY signal of multiple devices through a single isolator or a microcontroller input pin by connecting the READY output of each device to the RDYEN input of the next device in the chain. READY from the last device in the chain drives the isolator input, or the microcontrol GPI.
29	READY	Open-drain output. Connect a pulldown resistor between READY and GND pin. Assert high to indicate the device is functional and the outputs are valid. The following conditions must be met for READY to assert high: 1. V_{DD3} is above the UVLO threshold. 2. REFDI is not open or shorted to GND. 3. MAX22195 is not in Thermal Shutdown. 4. RDYEN is high. 5. V_{DD24} is valid if the device is powered by V_{DD24} and EXTVM is not connected to V_{DD3}.

Functional/Block Diagram



Detailed Description

The MAX22195 senses the state (on, high or off, low) of each input (IN1-IN8). The voltages at the IN1–IN8 input pins are compared against internal references to determine whether the sensor is on (logic 1) or off (logic 0). Placing a 8.6kΩ current-setting resistor between REFDI and GND, and a 1.5kΩ resistor in series with each input ensures that the current at the on and off trip points as well as the voltage at the trip points satisfy the requirements of IEC 61131-2 for Type 1 and Type 3 inputs (Figure 2). The current sunk by each input pin rises linearly with input voltage until the level set by the current-limiter is reached; any voltage increase beyond this point does not increase the input current. Limiting the input current ensures compliance with IEC 61131-2 while significantly reducing power dissipation compared to traditional resistive inputs.

The current-setting resistor R_{REFDI} can be calculated using this equation:

$$I_{INLIM}\ [mA] = V_{IN} / 517\ [V/k\Omega] + 20.5 / R_{REFDI}\ [V/k\Omega]$$

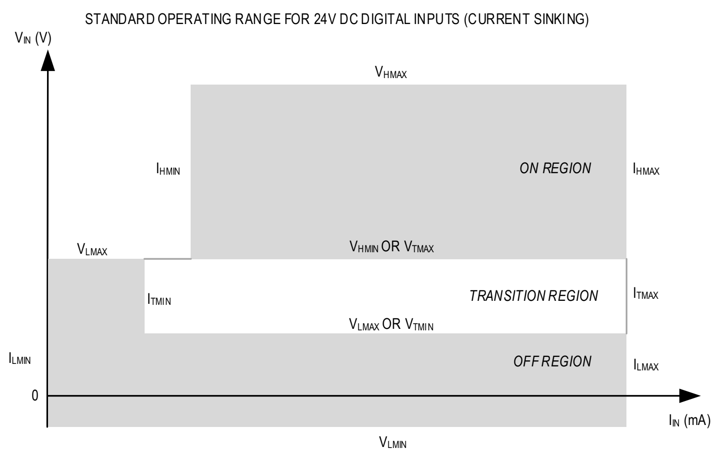
where V_{IN} is 5.6V at the input pin during production test for the typical value of Type 1 and 3, and Type 2 current limits.

RDYEN and READY Monitor

The READY output is used to signal a logic-side controller that the field-side circuit is working. This allows the controller to distinguish from a valid reading of eight low inputs or an invalid reading caused by a field-side fault such as loss of power. The READY output is asserted high when the following five conditions are met: the UVLO voltage threshold for V_{DD3} is exceeded; the V_{DD24} field supply requirement is met as set by internal thresholds or EXTVM external thresholds if enabled; the device is not in thermal shutdown; current through the REFDI pin is in a reasonable range (7.21µA to 550µA); and the RDYEN is high.

Ready Enable RDYEN is used to cascade other READY signals through to a single digital isolation channel or a microcontroller GPI pin. Connect the READY output of one device to the RDYEN input of the next device in the chain. Connect the final READY output to a digital isolator or a microcontroller GPI pin. All READY signals must be high for the final READY signal to go high. READY is an open-drain PMOS output, driven to V_{DD3} for a high output and set at high-impedance for a low output. Refer to *Typical Application Circuits* for details.

Outputs OP1 - OP8 are high-impedance only when thermal shutdown is triggered.



Type of Limit	Type 1 Limits						Type 2 Limits						Type 3 Limits					
	Off Region		Transition		On Region		Off Region		Transition		On Region		Off Region		Transition		On Region	
	VL (V)	IL (mA)	VT (V)	IT (mA)	VH (V)	IH (mA)	VL (V)	IL (mA)	VT (V)	IT (mA)	VH (V)	IH (mA)	VL (V)	IL (mA)	VT (V)	IT (mA)	VH (V)	IH (mA)
Max	15/5	15	15	15	30	15	11/5	30	11	30	30	30	11/5	15	11	15	30	15
Min	-3	ND	5	0.5	15	2	-3	ND	5	2	11	6	-3	ND	5	1.5	11	2

ND = NOT DEFINED

Figure 2. Switching Characteristics for IEC 61131-2 Type 1, 2, and 3 24VDC Digital Inputs

External VDD24 Voltage Monitor

The EXTVM input controls how the V_{DD24} field supply affects the READY output. When EXTVM is connected to V_{DD3}, the status of the V_{DD24} field supply becomes a don't-care in the decision to assert READY. This is useful when the MAX22195 is being powered directly from a 3.3V supply on V_{DD3} and V_{DD24} is not in use. When EXTVM is connected to GND, the voltage on V_{DD24} must be above the nominal 14V threshold before READY asserted high. To use an user-defined V_{DD24} supply voltage threshold, use an external resistive divider to apply an analog voltage directly to EXTVM. The voltage at EXTVM must be greater than the threshold, 0.81V (V_{REF}) nominal, before READY asserted high. Figure 3 shows an example of the V_{DD24} being monitored with the use of external resistive divider to set a nominal threshold before READY asserted high.

$$V_{DD24} = V_{REF} (1 + (R2/R1))$$

Short/Open Detection at REFDI Pin

Short or open detection at REFDI pin is implemented by monitoring the current set by REFDI pin.When more than 550µA current is detected, meaning a short at REFDI, the 2mA minimum input current is not guaranteed, and field input low-to-high and high-to-low thresholds are changed. When less than 7.21µA current is detected, meaning an open at REFDI, the 2mA minimum input current is not guaranteed. When open or short at REFDI pin is detected, the READY pin is not asserted.

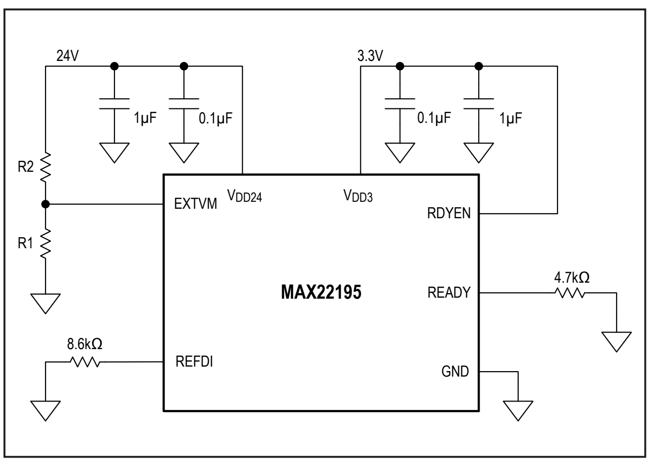


Figure 3. User-Defined VDD24 Threshold Set by EXTVM and External Resistive Divider

Energyless LED Drivers

When IN_ is determined to be on, its input current is diverted to the LED_ pin and flows from that pin to GND. Placing an LED between LED_ and GND provides an indication of the input state without increasing overall power dissipation. If the indicator LEDs are not used, connect LED_ to GND.

Type 2 Sensor Inputs

The additional input current (6mA min) and associated power dissipation of Type 2 input require the use of two MAX22195 inputs in parallel. The current of each channel is set to a nominal 3.97mA (7.9mA total) by placing a 5.2kΩ resistor from REFDI to GND. The proper voltage drop across the input resistor is maintained by reducing the resistance from 1.5kΩ to 1kΩ for each MAX22195 input channel. If lower input current is desired, the REFDI resistor can be increased to 5.76kΩ or higher as long as the 6mA minimum input current for Type 2 is met. For proper surge protection, it is important that each MAX22195 input has its own resistor. Any two MAX22195 channels may be used; they need not be continuous (Figure 4). Either channel may be read to determine the input state. The additional power dissipation from this Type 2 configuration reduces the maximum ambient operating temperature to 120°C, when all inputs are at 30V, and the MAX22195s are powered from a 30V field supply and there is no additional load on V_{DD3}.

Thermal Considerations

The MAX22195 will operate at an ambient temperature of 125°C on a properly designed multilayer PC board. Operating at higher voltages, or with heavy output loads such as optical isolators will increase power dissipation and reduce the maximum allowable operating temperature. See *Package Information* section and *Absolute Maximum Ratings* section for safety operation temperature and maximum power dissipation.

The MAX22195 is in thermal shutdown when the thermal shutdown temperature threshold is exceeded. During thermal shutdown, the internal voltage regulator, input channels, REFDI circuitry are all turned off, and outputs OP1-OP8 are high-impedance.

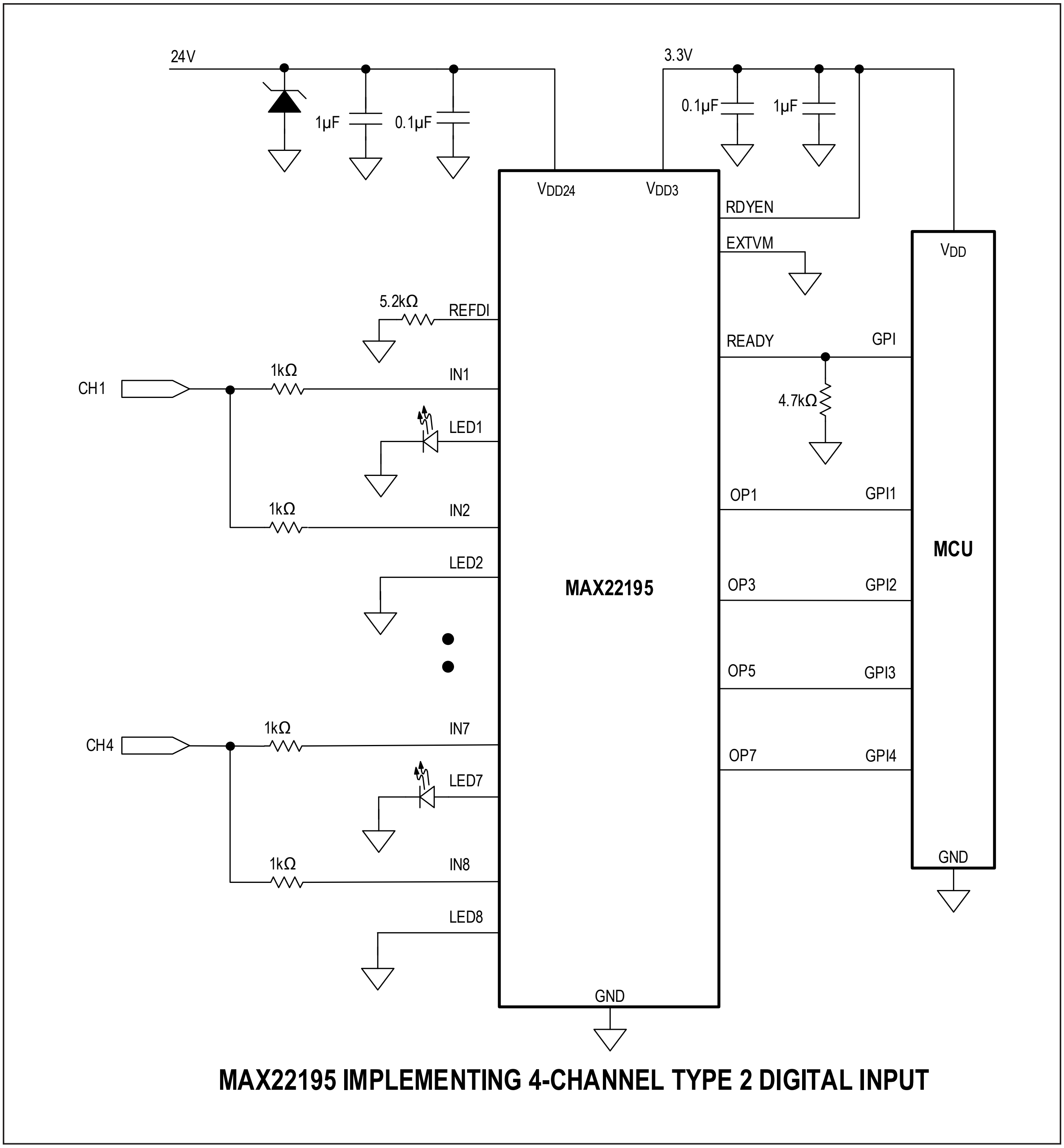


Figure 4. Implementing Type 2 Digital Inputs with MAX22195

Applications Information

Power Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DD24} and V_{DD3} with a 0.1μF low-ESR ceramic capacitor in parallel with 1μF ceramic capacitor to GND, respectively. Place the bypass capacitors as close as possible to the power supply input pins.

Powering MAX22195 with V_{DD3}

The MAX22195 can alternatively be powered using a 3.0 – 5.5V supply connected to the V_{DD3} pin. In this case, a 24V supply is no longer needed, the V_{DD24} pin must be left unconnected and EXTVM pin is connected to V_{DD3} to disable the V_{DD24} voltage monitoring, see *Typical Application Circuits* for details. This configuration has lower power consumption and heat dissipation since the on-chip LDO voltage regulator is disabled (the V_{DD24} undervoltage lockout is below threshold and automatically disables the LDO).

PCB Layout Recommendations

The PCB designer should follow some critical recommendations in order to get the best performance from the design.

- Keep the input/output traces as short as possible. Avoid using vias on the signals to make low-inductance paths.
- Have a solid ground plane underneath the entire exposed pad (EP) area with multiple thermal vias for best thermal performance.
- In order to achieve the highest EFT performance, it is recommended to have the GND plane around the REFDI traces, and isolate the REFDI traces from all input traces, especially IN8, as much as possible. For example, route input traces and REFDI traces on two different layers and have a GND plane on the inner layers in between.

IEC 61131-2 EMC Requirement

The MAX22195 is required to operate reliably in harsh industrial environments. The device can meet the transient immunity requirements as specified in IEC 61131-2, including Electrostatic Discharge (ESD) per IEC 61000-4-2, Electrical Fast Transient/Burst (EFT) per IEC 61000-4-4, and Surge Immunity per IEC 61000-4-5. Maxim's proprietary process technology provides robust input channels and field supply with internal ESD structures and high Absolute Maximum Ratings (see the *Absolute Maximum Ratings* section), but external components are also required to absorb excessive energy from ESD and surge transients. The circuit with external components shown in Figure 5 allows the device to meet and exceed the transient immunity requirements as specified in IEC 61131-2 and related IEC 61000-4-x standards. The system shown in Figure 5, using the components shown in Table 1, is designed to be robust against ESD, EFT, and Surge specifications as listed in Table 2. In all these tests, the part or DUT is soldered onto a properly designed application board (e.g., the MAX22195EVKIT#) with necessary external components.

Table 1. Recommended Components for EMC compliance

COMPONENT	DESCRIPTION	REQUIRED/RECOMMENDED
C1	1μF, 100V ceramic capacitor	Required
C2	0.1μF, 100V low-ESR ceramic capacitor	Required
C3	1μF, 10V ceramic capacitor	Required
C4	0.1μF, 10V low-ESR ceramic capacitor	Required
C5	3.3nF, safety rated Y capacitor (2220)	Recommended
D1	Unidirectional TVS diode SMBJ33A (42Ω) or SM30T39AY (2Ω)	Recommended
R1	1.5kΩ or 1kΩ, 1W pulse withstanding resistor (CMB0207 or similar)	Required
All other Resistors	0603, 0.1W resistors	Required
All LEDs	LEDs for visual input status indication	Recommended

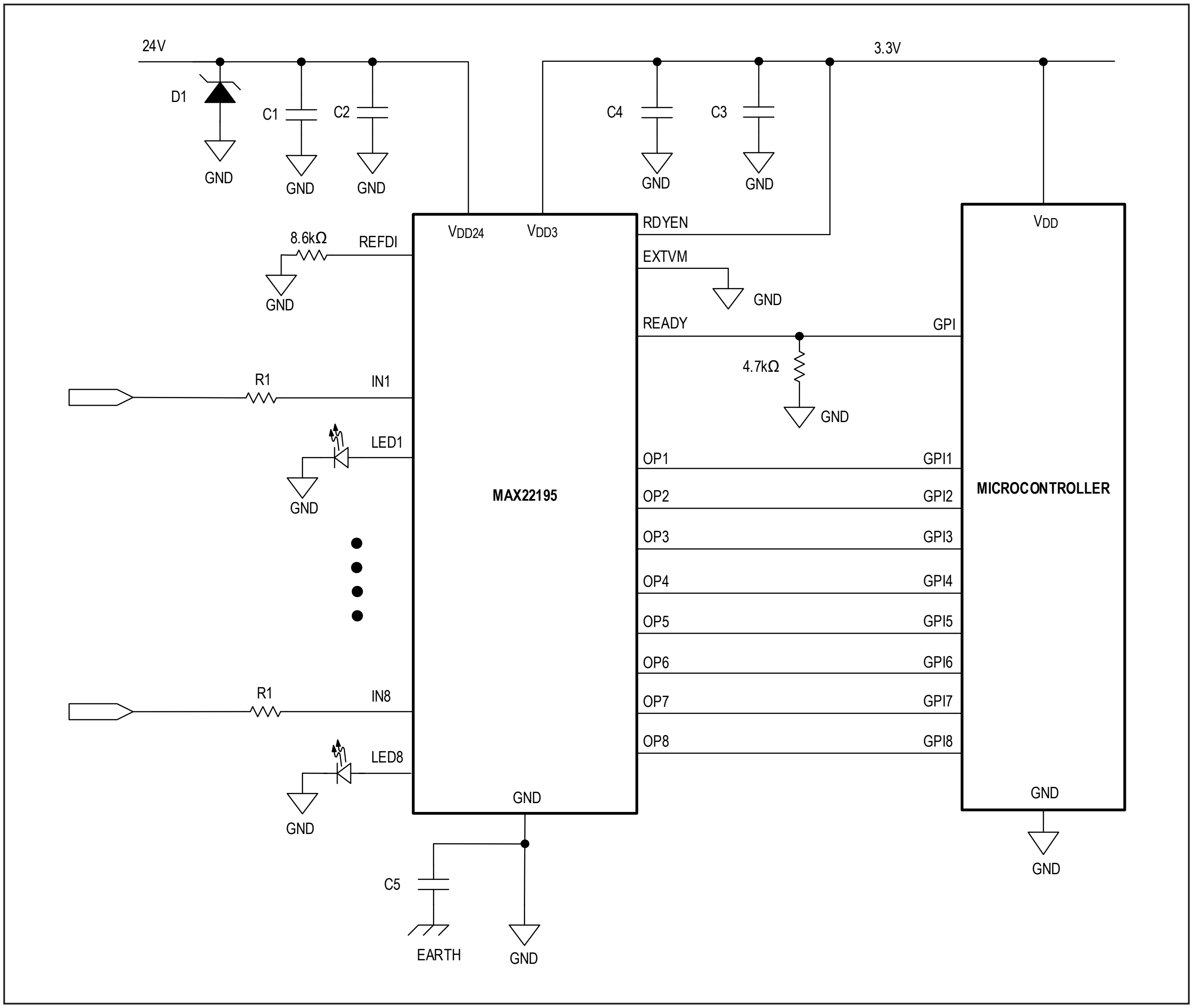


Figure 5. Typical EMC Protection Circuit for the MAX22195

ESD Protection of Field Inputs

The input resistor limits the energy into the MAX22195 IN_ pins and protects the internal ESD structure from excessive transient energy. An input series resistor is required and should be rated to withstand such ESD levels. The MAX22195 input channels can withstand up to ±8kV ESD contact discharge and ±15kV ESD air-gap discharge with an input series resistor of 1kΩ or larger. The input resistor value shifts the field voltage switching threshold scaled by the input current; thus, it determines the input characteristics of the application. The package of the resistor should be large enough to prevent the arcing across the two resistor pads. Arcing depends on the ESD level applied to the field input and the application pollution degree.

EFT Protection of Field Inputs

The input channels can withstand up to ±2kV, 5kHz, or 100kHz fast transients (Figure 7) with performance criterion A, normal operation within specification limits. The MAX22195 outputs OP1–OP8 and READY signal operate as normal without any loss of function or performance. With EFT levels up to ±4kV, outputs OP1–OP8 still operate as normal, but the READY signal is corrupted; thus, giving a criterion B performance with temporary degradation of the READY function.

A capacitive coupling clamp is used to couple the fast transients (burst) from the EFT generator to the field inputs of the MAX22195 without any galvanic connection to the MAX22195 input pins.

Surge Protection of Field Inputs

In order to protect the IN_ pins against 1kV/42Ω, 1.2/50µs surges (Figure 8 and Figure 9), two options exist. The first option is to use a series pulse-withstanding resistor as shown in the various application diagrams in the data sheet. A pulse resistor greater or equal to 1kΩ should be used for safe operation. The pulse resistor should support dissipation of the surge energy. Examples of suitable resistors are CMB0207 MELF or CRCW-IF thick film as well as others. The resistor value is defined by the Type 1, 2, 3, or other input characteristics. Capacitors for filtering should not be connected to the IN_ pins.

The second option, which can result in a smaller overall footprint, is to use a bidirectional TVS to GND at the field input with a low-power series resistor, greater or equal to 1kΩ. The TVS must be able to absorb the surge energy and has the function of limiting the peak voltage so that the resistor only sees a low differential voltage. Suitable TVS with a small footprint are SPT02-236 or PDFN3-32, offering protection against 1kV/42Ω surge.

Surge Protection of 24V Supply

In order to protect the V_{DD24} pin against 500V/42Ω, 1.2/50µs surges (Figure 8), a SMBJ33A TVS can be applied to the V_{DD24} pin.

Table 2. Transient Immunity Test Results

TEST		RESULT	
IEC 61000-4-2 Electrostatic Discharge (ESD)	Contact ESD	±8kV	
	Air-Gap ESD	±15kV	
IEC 61000-4-4 Electrical Fast Transient / Burst (EFT)	Line-to-Ground	±2kV	READY and OP1-OP8 operate without degradation of performance
		±4kV	OP1-OP8 operate without degradation of performance; READY signal is corrupted
IEC 61000-4-5 Surge Immunity	Line-to-Ground	±1kV	
	Line-to-Line	±2kV	
	Power Supply	±500V	

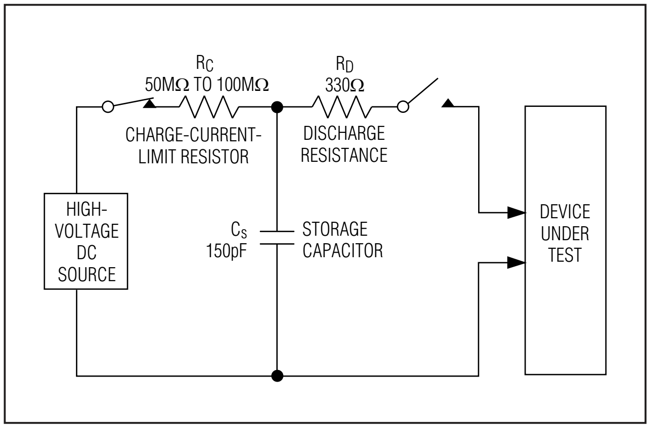


Figure 6a. Test Circuit

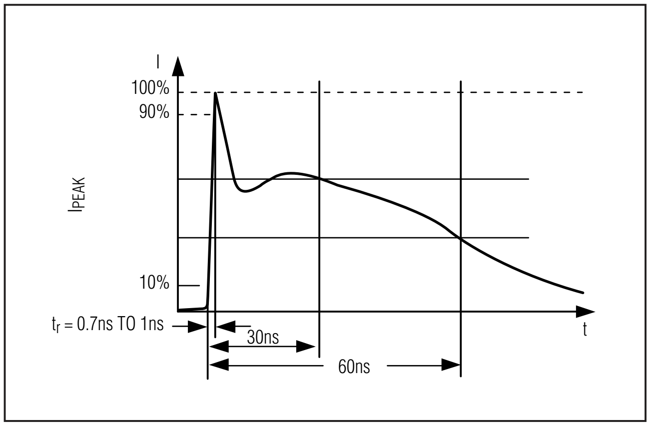


Figure 6b. Test Waveform

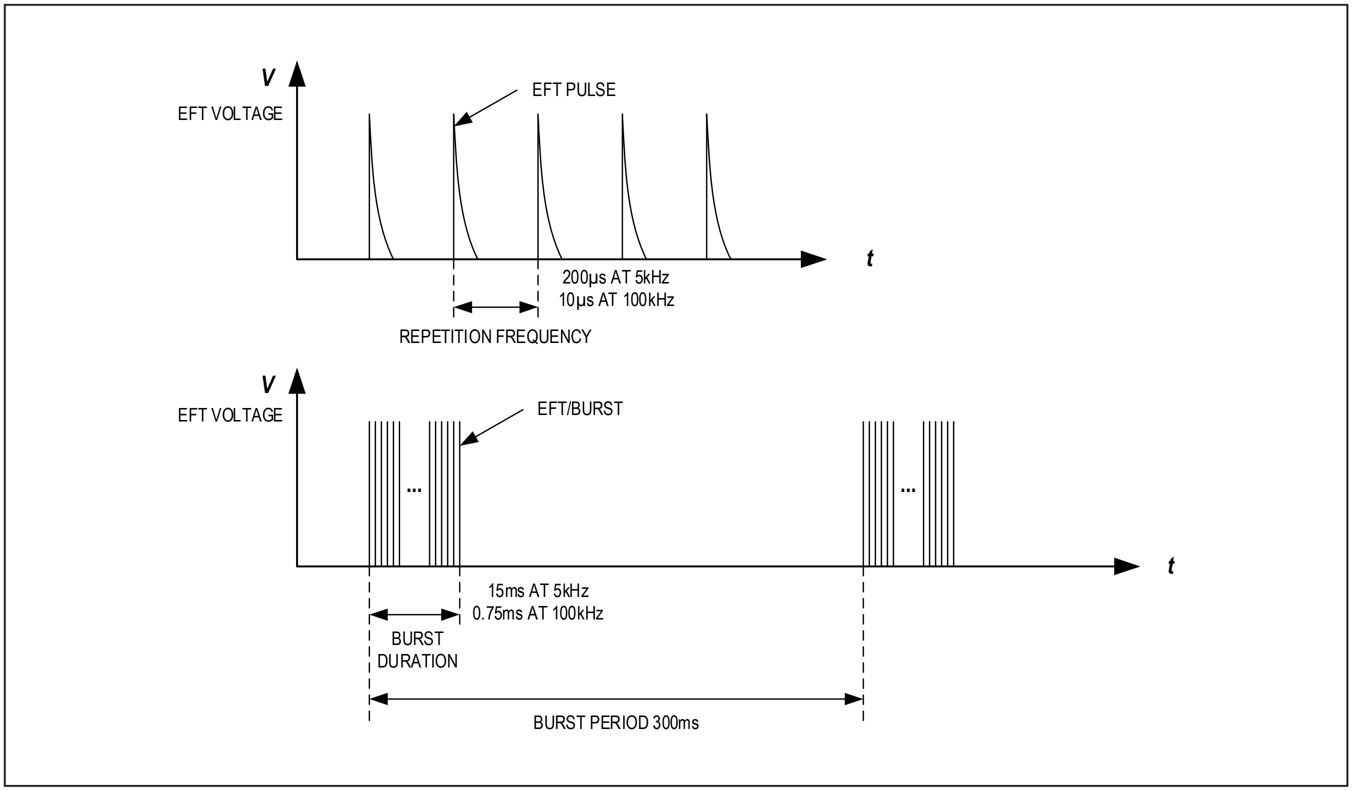


Figure 7. Electrical Fast Transient/Burst Waveform

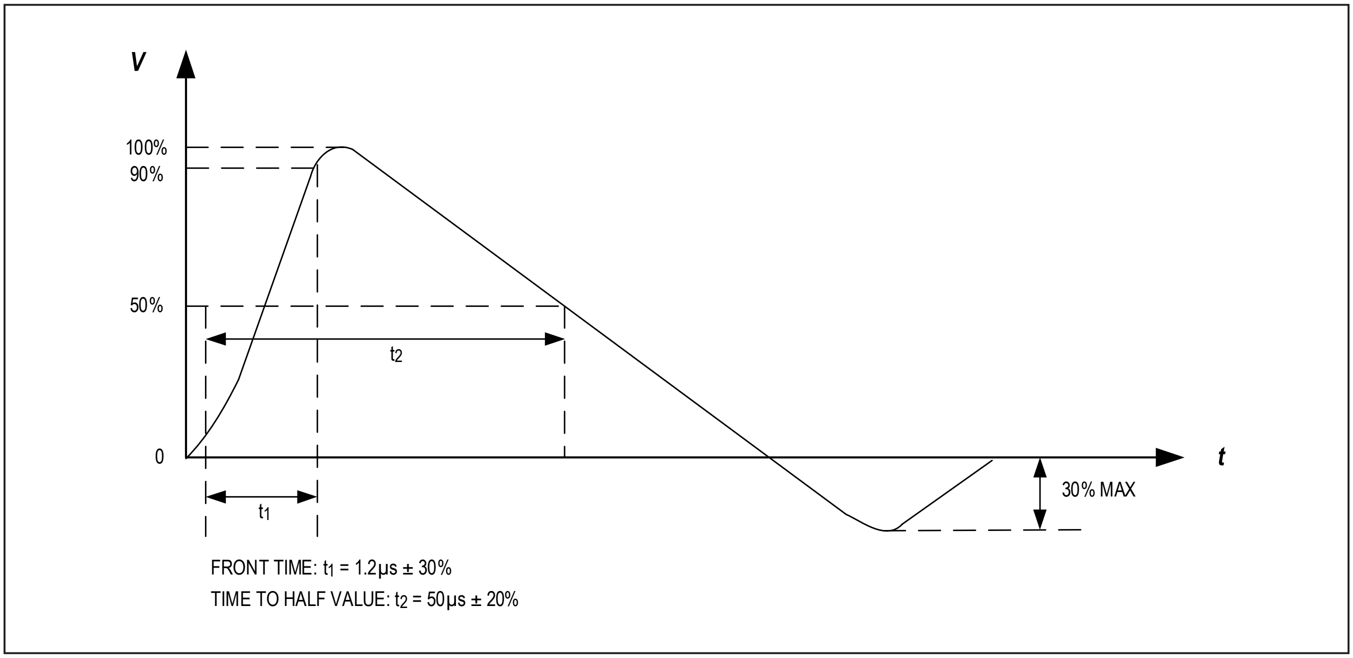


Figure 8. 1.2/50µs Surge Voltage Waveform

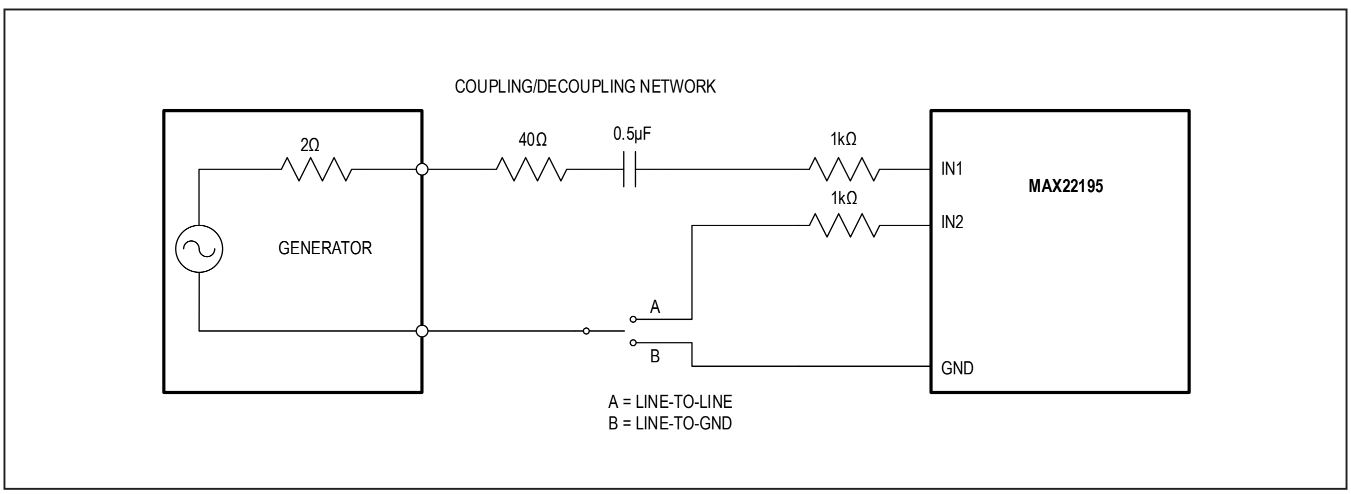
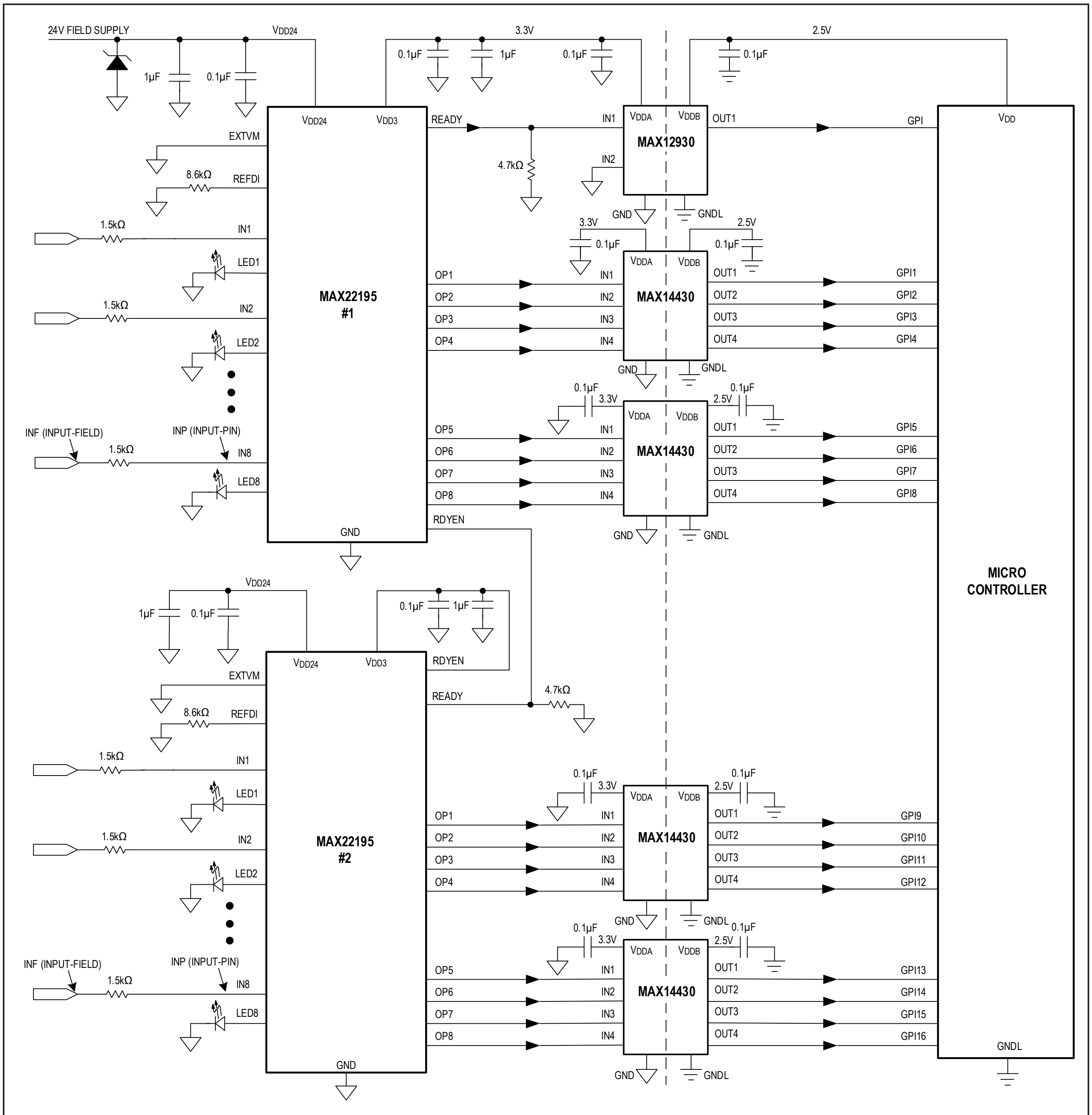


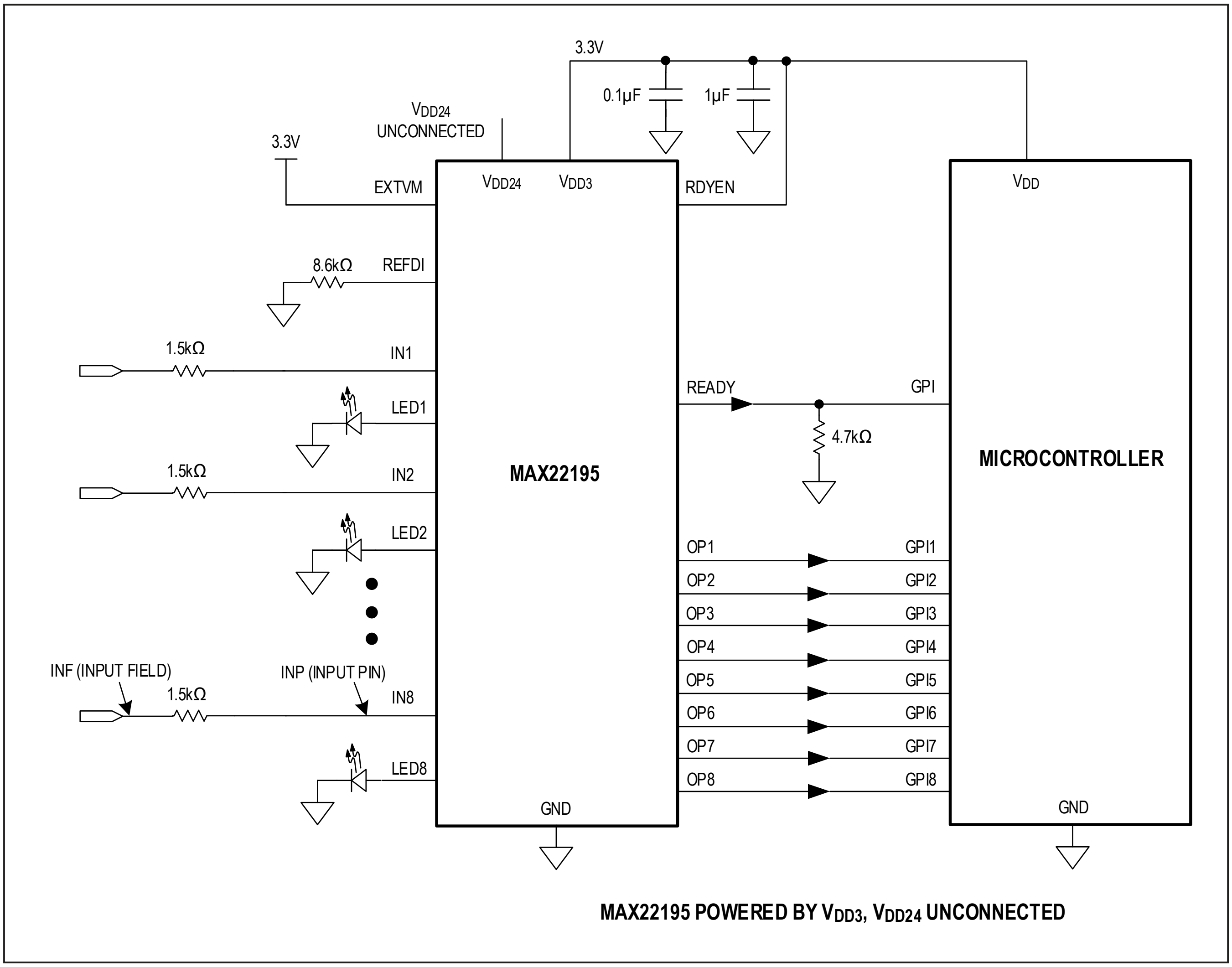
Figure 9. Surge Testing Method

Typical Application Circuits



ISOLATED 16–CHANNEL TYPE 1/3 DIGITAL INPUT

Typical Application Circuits (continued)



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX22195ATJ+	-40°C to +125°C	32-TQFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/18	Initial release	—
1	7/18	Updated *Benefits and Features* section, *Electrical Characteristics* table, *Pin Description* table, *Detailed Description* section, and Figure 5	1, 4, 5, 11, 14
2	9/18	Updated the *ESD and EMC Characteristics* table and the *Detailed Description* section	7, 14
3	1/19	Updated *ESD and EMC Characteristics* table, and *PCB Layout Recommendations*, and *IEC61000-4-4 Electrical Fast Transient/Burst (EFT)* sections; corrected typos	7, 17, 19–20
4	4/19	Updated the *General Description, Electrical Characteristics, Pin Description, RDYEN and READY Monitor, Short/Open Detection at REFDI Pin, Energyless LED Drivers, Thermal Considerations, IEC 61000-4-4 Electrical Fast Transient/Burst (EFT)* and *IEC 61000-4-5 Surge Immunity sections*, and Table 1; replaced Table 3.	1, 6, 12, 14 15, 17, 19–21
5	9/20	Updated the *Pin Description* and *Power Supply Decoupling* sections, Table 1 and new Table 2; updated the Octal Digital Input with Parallel Output, Figures 4–5, 7–9, and the Typical Application Circuits; removed the *Surge Protection, EMC Standard Compliance, Test Levels and Methodology, IEC 61000-4-2 Electrostatic Discharge (ESD), Contact discharge Method, Air Gap Discharge Method, IEC 61000-4-4 Electrical Fast Transient/Burst (EFT)* and *IEC 61000-4-5 Surge Immunity* sections; removed the existing Table 2 and renumbered subsequent tables; renamed the *Typical Operating Circuits Typical Application Circuits;* added the *IEC61131-2 EMC Requirement, ESD Protection of Field Inputs; EFT Protection of Field Inputs, Surge Protection of Field Inputs,* and *Surge Protection of 24V Supply* sections	2, 12, 15–23
6	3/21	Updated the *Powering MAX22195 with* V_{DD3} Section, Table 1, and MAX22195 *Typical Application Circuit* (*Powered by* V_{DD3}).	17, 23

