# APS12170

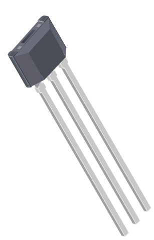
## Two-Wire Continuous Time Hall-Effect Latch

### FEATURES AND BENEFITS

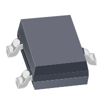
- Symmetrical latch switch points
- Automotive-grade ruggedness and fault tolerance
  - □ Extended AEC-Q100 Grade 0 qualification
  - □ Reverse-battery and 40 V load dump protection
  - □ Operation from –40°C to 175°C junction temperature
  - □ High EMC immunity, ±12 kV HBM ESD
  - □ Undervoltage lockout
  - □ Overvoltage clamping protection
  - □ Resistant to physical stress
- Operation from unregulated supplies, 3.8 to 16 V
- Continuous-time operation
  - □ Fast power-on time
  - □ Low EMI emissions
  - □ Low latency
  - □ Regulator stability without a bypass capacitor
- Current mode output—voltage controlled
- Solid-state reliability
- Industry-standard packages and pinouts

### PACKAGES:

*Not to scale*



3-pin SIP (suffix UA)



3-pin SOT23W (suffix LH)

### DESCRIPTION

The APS12170 is a two-wire, planar Hall-effect sensor integrated circuit (IC) operating under a continuous-time sensing architecture. The devices are extremely fast responding with lower levels of emissions (EMI) than a design using chopper stabilization.

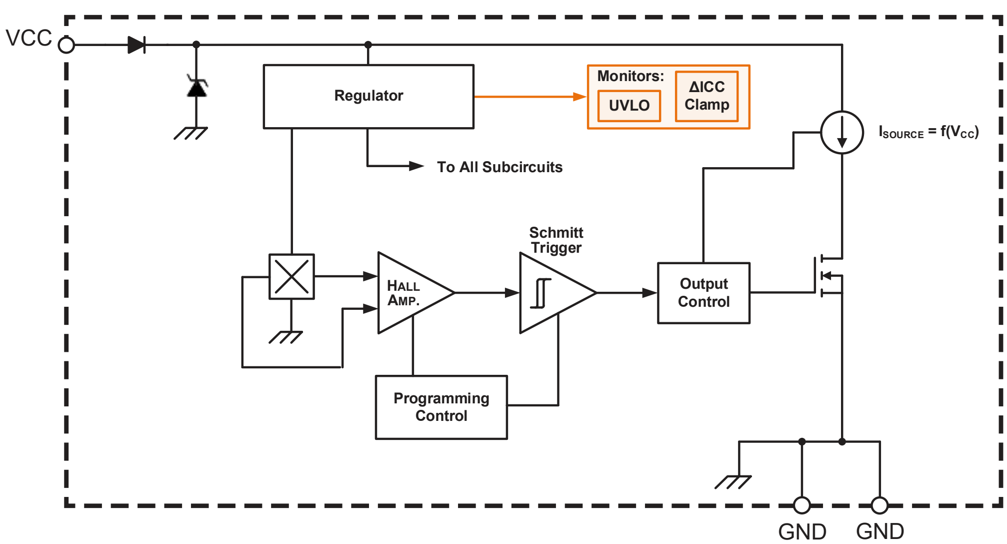
This Hall-effect latch IC features extended AEC-Q100 qualification and is ideal for high-temperature operation up to 175°C junction temperatures. In addition, the APS12170 includes a number of features designed specifically to maximize system robustness, such as reverse-battery protection, overvoltage, and EMC protection.

A south pole and a north pole of sufficient strength are both necessary to actuate the device. The devices include on-board transient protection for all pins, permitting operation directly from a vehicle battery or regulator with supply voltages from 3.8 to 16 V.

Two package styles provide a choice of through-hole or surface mounting. Package type LH is a modified 3-pin SOT23W surface-mount package, while UA is a three-pin ultramini SIP for through-hole mounting. Both packages are lead (Pb) free and RoHS compliant, with 100% matte-tin-plated leadframes.

### APPLICATIONS

- Seat/window motors
- Sun roof/convertible top/liftgate/tailgate actuation
- Automotive and industrial safety systems




**Functional Block Diagram**

## SELECTION GUIDE

| Part Number | Packing [1] | Mounting | Branding | $B_{RP}$ (Min) | $B_{OP}$ (Max) |
|---|---|---|---|---|---|
| APS12170LLHALX | 13-in. reel, 10000 pieces/reel | 3-pin SOT23W surface mount | AAL | –175 G | 175 G |
| APS12170LLHALT [2] | 7-in. reel, 3000 pieces/reel | 3-pin SOT23W surface mount | | | |
| APS12170LUAA | Bulk, 500 pieces/bag | 3-pin SIP through hole | | | |

[1] Contact Allegro for additional packing options.
[2] Available through authorized Allegro distributors only.

## ABSOLUTE MAXIMUM RATINGS

| Characteristic | Symbol | Notes | Rating | Units |
|---|---|---|---|---|
| Supply Voltage [1] | $V_{CC}$ | $T_J < T_{J(max)}$ | 30 | V |
| | $V_{CCS}$ | 1 minute, $T_A$ = 85°C, $I_{CC} = I_{CC(HIGH)}$, $R_{SENSE}$ = 182 ±1% (Ω) | 24 | V |
| | | 1 minute (jump start) $T_A$ = 25°C, $I_{CC} = I_{CC(HIGH)}$, $R_{SENSE}$ = 182 ±1% (Ω) | 26 | V |
| | | 0.5 seconds (load dump), $T_A$ = 25°C, $I_{CC} = I_{CC(HIGH)}$, $R_{SENSE}$ = 182 ±1% (Ω) | 40 | V |
| Reverse Supply Voltage [1] | $V_{RCC}$ | | –30 | V |
| Forward Supply Current [1] | $I_{CC}$ | | 52.5 | mA |
| Reverse Supply Current [1] | $I_{RCC}$ | | –10 | mA |
| Magnetic Flux Density [2] | B | | Unlimited | – |
| Maximum Junction Temperature | $T_J(max)$ | | 165 | °C |
| | | For 1000 hours | 175 | °C |
| Storage Temperature | $T_{stg}$ | | –65 to 170 | °C |

[1] Unless specifically noted, this rating does not apply to extremely short voltage transients such as conducted immunity and/or ESD. Those events have individual ratings, specific to the respective transient voltage event. Rating is based on anticipated performance.
[2] Guaranteed by design.

## ESD PERFORMANCE

| Characteristic | Symbol | Notes | Rating | Units |
|---|---|---|---|---|
| ESD Voltage | $V_{ESD(HBM)}$ | Human Body Model according to AEC-Q100-002 | ±12 | kV |

## TRANSIENT PROTECTION CHARACTERISTICS: Valid for $T_A$ = 25°C

| Characteristic | Symbol | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Supply Zener Clamp Voltage | $V_Z$ | $I_{CC} = I_{CC(LOW)}$ + 1.0 mA | 32 | – | – | V |
| Supply Zener Current [1] | $I_Z$ | $V_Z$ = 32 V | – | – | 10.5 | mA |
| Reverse Supply Zener Clamp Voltage | $V_{RZ}$ | $I_{CC}$ = –0.5 mA | – | – | –30 | V |
| Reverse Supply Current | $I_{RCC}$ | $V_{RCC}$ = –30 V | –10 | – | – | mA |

[1] Maximum current limit is equal to the maximum $I_{CC}$ + 3 mA.



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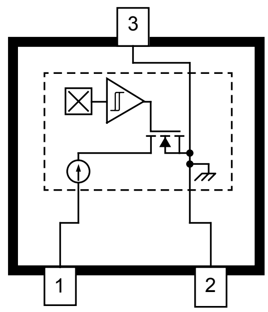
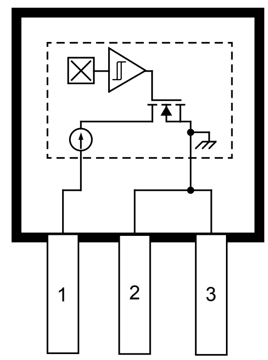
## PINOUT DIAGRAMS AND TERMINAL LIST TABLE




**LH Package,**
**3-Pin SOT23W Pinout**

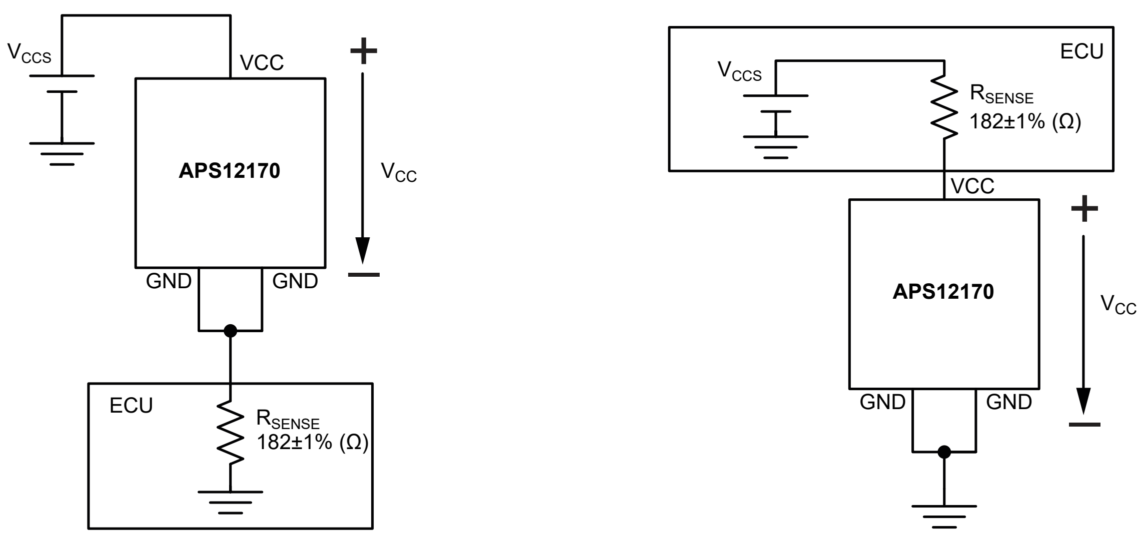



**UA Package,**
**3-Pin SIP Pinout**

### Terminal List

| Number | Package Name | | Function [1] |
|---|---|---|---|
| | LH | UA | |
| 1 | VCC | VCC | Connects power supply to chip |
| 2 | GND | GND | Ground |
| 3 | GND | GND | Ground |

[1] Pins 2 and 3 are tied together internally and the device will operate with either pin 2 or 3 grounded externally; however, grounding both pins externally will improve EMC robustness.




**(A) Low-Side Sensing** **(B) High-Side Sensing**

**Figure 1: Typical Application Circuits**



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**ELECTRICAL CHARACTERISTICS:** Valid for $T_A$ = –40°C to 150°C, unless otherwise specified

| Characteristics | Symbol | Test Conditions | Min. | Typ. [1] | Max. | Unit |
|---|---|---|---|---|---|---|
| **ELECTRICAL CHARACTERISTICS** | | | | | | |
| Supply Voltage [2] | $V_{CC}$ | UA, $T_J$ < 175°C | 3.8 | – | 16 | V |
| | | LH, $T_J$ < 175°C | 3.8 | – | 13 | V |
| | $V_{CCS}$ [3][8] | UA, $T_A$ = 25°C | 7 | – | 24 | V |
| | | LH, $T_A$ = 25°C | 7 | – | 21 | V |
| | | UA, $T_A$ = –40°C to 85°C | 7 | – | 19.5 | V |
| | | LH, $T_A$ = –40°C to 85°C | 7 | – | 16 | V |
| | | UA, $T_A$ = –40°C to 110°C | 7 | – | 16 | V |
| | | LH, $T_A$ = –40°C to 110°C | 7 | – | 13 | V |
| | | UA, $T_A$ = –40°C to 125°C, $I_{CC(HIGH)}$ Duty Cycle < 65% | 7 | – | 16 | V |
| | | LH, $T_A$ = –40°C to 125°C, $I_{CC(HIGH)}$ Duty Cycle < 65% | 7 | – | 13 | V |
| | | UA, $T_A$ = –40°C to 130°C, $I_{CC(HIGH)}$ for ≤ 250 hours (lifetime) | 7 | – | 16 | V |
| | | LH, TA = –40°C to 130°C, $I_{CC(HIGH)}$ for ≤ 250 hours (lifetime) | 7 | – | 13 | V |
| Supply Current | $I_{CC(LOW)}$ | B < $B_{RP}$ | 4.5 | – | 7.5 | mA |
| | $I_{CC(HIGH)}$ | B > $B_{OP}$ | – | $I_{CC(LOW)}$ + $\Delta I_{CC}$ | – | mA |
| Proportional Supply Current [4][5] | $\Delta I_{CC}$ | $V_{CC}$ ≤ 7.3 V | –10% | $V_{CC}$ / 400 Ω | 10% | mA |
| | | $V_{CC}$ > 7.3 V | –7% | $V_{CC}$ / 400 Ω | 7% | mA |
| Proportional Current Clamp [5][6][7] | $\Delta I_{CCclamp}$ | $V_{CC\Delta ICCL}$ < $V_{CC}$ < $V_{CC\Delta ICCH}$, Foldback Enabled, $T_A$ = 25°C | – | 40 | – | mA |
| Proportional Current Clamp, Supply Voltage Level [5] | $V_{CC\Delta ICCH}$ | $V_{CC}$ increasing | – | 19 | 21 | V |
| | $V_{CC\Delta ICCL}$ | $V_{CC}$ decreasing | 16.5 | 18 | – | V |
| Power-On Time | $t_{ON}$ | B > $B_{OP}$ + 5 G or B < $B_{RP}$ – 5 G, $dV_{CC}/dt$ < 0.8 V/μs | – | – | 4 | μs |
| | | B > $B_{OP}$ + 5 G or B < $B_{RP}$ – 5 G | – | – | 8 | μs |
| Power-On State, Output | POS | $V_{CC}$ ≥ $V_{CC}$(min), t < $t_{ON}$ | | $I_{CC(HIGH)}$ | | – |
| Undervoltage Lockout | $V_{UVLO}$ | $V_{CC}$ decreasing; for $V_{UVLO}$ < $V_{CC}$ < $V_{CC(min)}$, $B_{OP}$ and $B_{RP}$ are not guaranteed | – | 2.5 | – | V |
| Power-Off Voltage | $V_{SD}$ | $V_{CC}$ decreasing; for $V_{SD}$ < $V_{CC}$ < $V_{UVLO}$, the device output is in the POS | – | 2.25 | – | V |
| Output Response Time [8] | $t_D$ | 250 G step in 1 μs, 182 Ω $R_{SENSE}$ only (low side) | – | 3.3 | 5 | μs |
| Output Slew Rate, Rising [9][10] | $dI/dt_{RISING}$ | $V_{CC}$ = 12 V, $R_{SENSE}$ = 182 ±1% Ω, $C_S$ = 12 pF, No $C_{BYP}$ | – | 25 | – | mA/μs |
| Output Slew Rate, Falling [9][10] | $dI/dt_{FALLING}$ | $V_{CC}$ = 12 V, $R_{SENSE}$ = 182 ±1% Ω, $C_S$ = 12 pF, No $C_{BYP}$ | – | 48 | – | mA/μs |

[1] Typical data are at $T_A$ = 25°C and $V_{CC}$ = 12 V, unless otherwise noted; for design information only.
[2] Maximum voltage must be adjusted for power dissipation and junction temperature, see Power Derating section.
[3] $V_{CCS}$ is defined as $V_{CC}$ + $V_{DROP}$ where $V_{DROP}$ is f($R_{SENSE}$), $R_{SENSE}$ = 182 ±1% Ω, $I_{CC}$ = $I_{CC(HIGH)}$.
[4] Measured as difference in high and low output states, $V_{CC}$ < $V_{CC\Delta ICCH}$.
[5] Independent of external $R_{SENSE}$ value.
[6] Set internally; independent of value of external $R_{SENSE}$.
[7] "Foldback enable" means foldback is enabled when $V_{CC}$ > $V_{CC\Delta ICCH}$
[8] Guaranteed by device design and characterization.
[9] Change in current, dI, is the difference between 10% and 90% of $I_{CC(HIGH)}$ – $I_{CC(LOW)}$; dt is the time period between those two points.
[10] $C_S$ is the oscilloscope capacitance.



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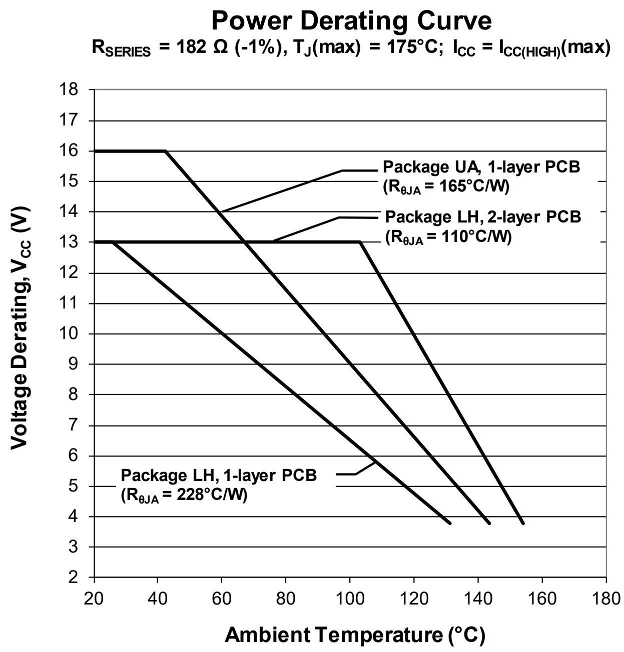
**OPERATING CHARACTERISTICS:** Valid over full operating voltage and ambient temperature ranges

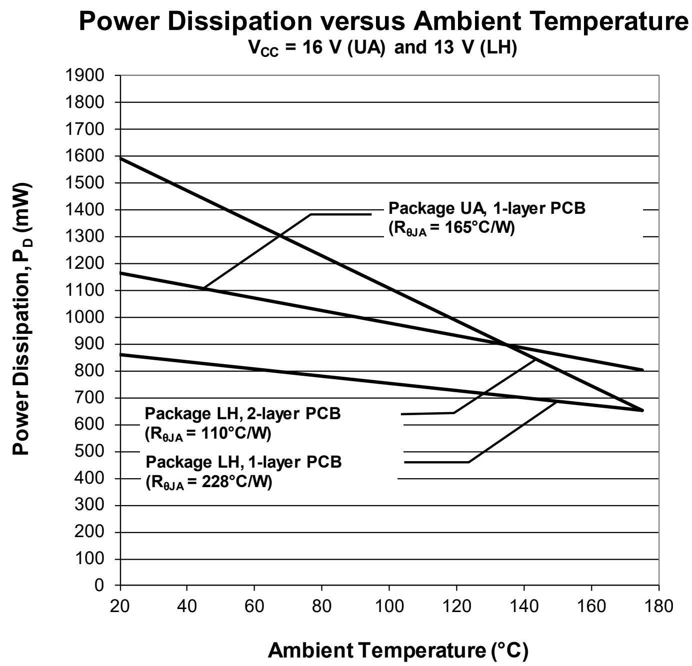
| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit [1] |
|---|---|---|---|---|---|---|
| **MAGNETIC CHARACTERISTICS** | | | | | | |
| Operate Point | $B_{OP}$ | South pole adjacent to branded face of device | 50 | – | 175 | G |
| Release Point | $B_{RP}$ | North pole adjacent to branded face of device | –175 | – | –50 | G |
| Hysteresis | $B_{HYS}$ | $B_{OP} – B_{RP}$ | 100 | – | 350 | G |
| Offset | $B_{OFF}$ | $(B_{OP} + B_{RP}) / 2$ | –50 | – | 50 | G |

[1] 1 G (gauss) = 0.1 mT (millitesla).

**THERMAL CHARACTERISTICS:** May require derating at maximum conditions; see Applications section

| Characteristic | Symbol | Test Conditions | Value | Units |
|---|---|---|---|---|
| Package Thermal Resistance | $R_{\theta JA}$ | Package LH, 1-layer PCB with copper limited to solder pads | 228 | °C/W |
| | | Package LH, 2-layer PCB with 0.463 in² of copper area each side connected by thermal vias | 110 | °C/W |
| | | Package UA, 1-layer PCB with copper limited to solder pads | 165 | °C/W |



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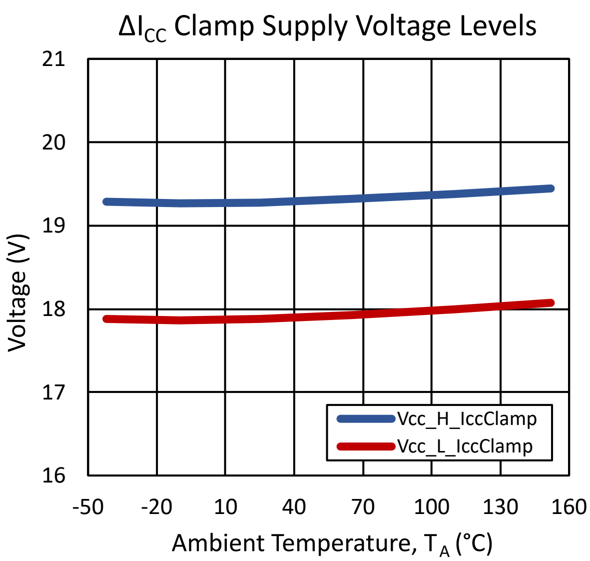
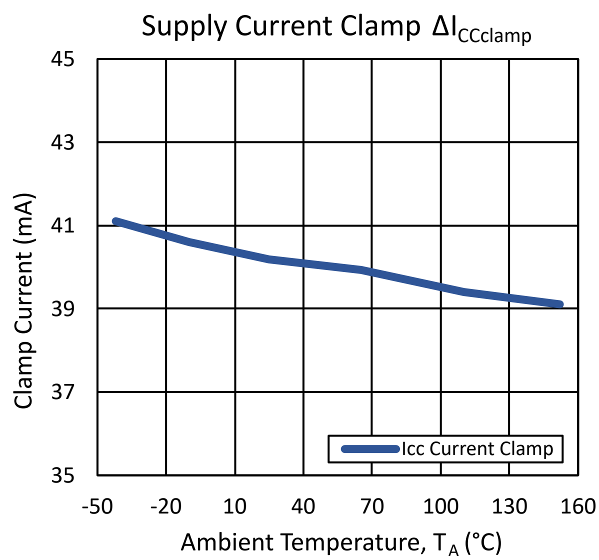
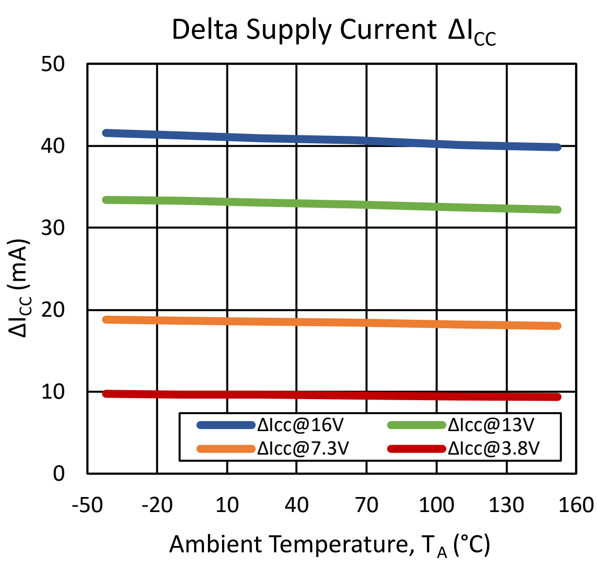
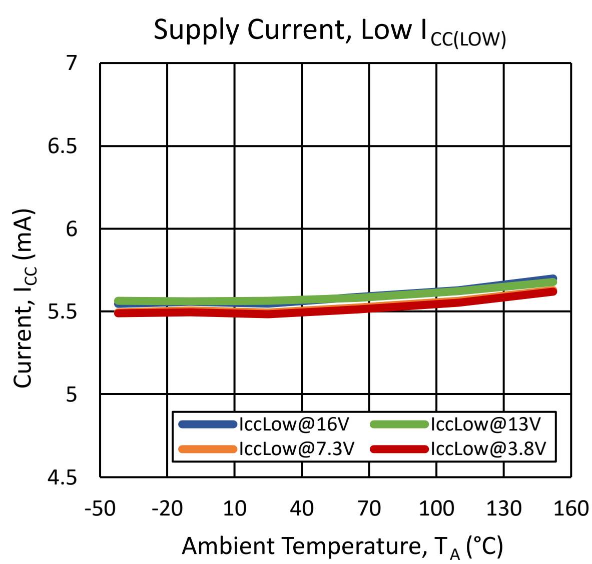
## CHARACTERISTIC PERFORMANCE

### Electrical Characteristics



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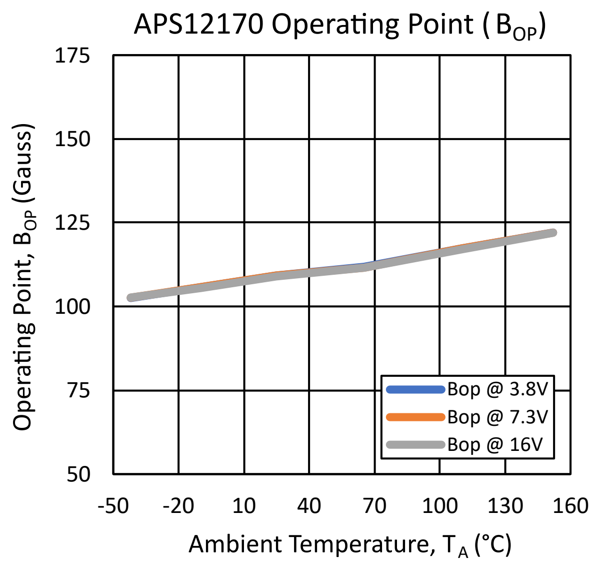
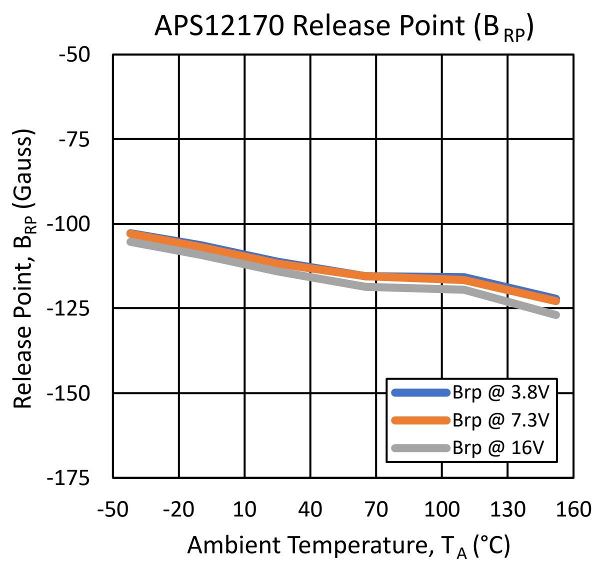
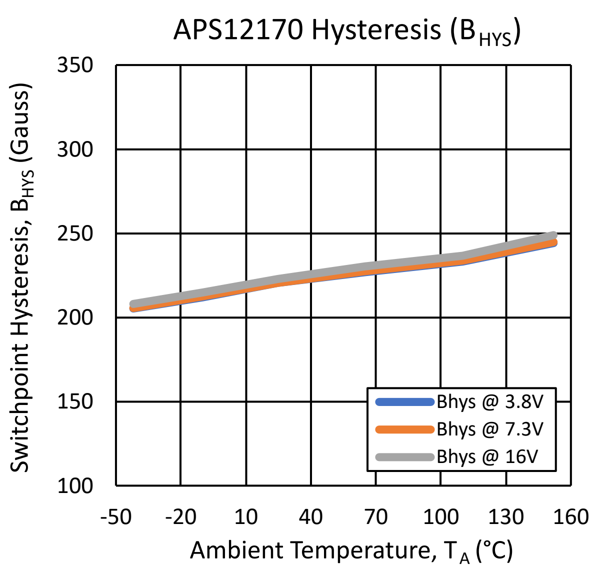
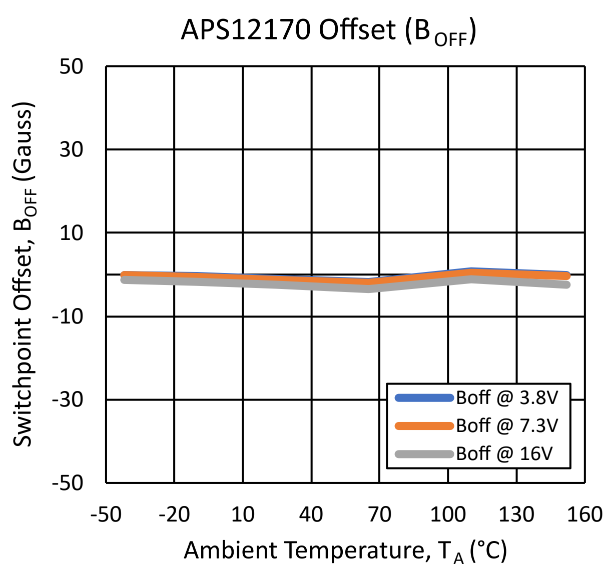
## CHARACTERISTIC PERFORMANCE (continued)

### Magnetic Characteristics



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## FUNCTIONAL DESCRIPTION

### Operation

The output of these devices switches high to $I_{CC(HIGH)}$ when a magnetic field perpendicular to the Hall element exceeds the operate point threshold, $B_{OP}$ (see Figure 2). When the magnetic field is reduced below the release point, $B_{RP}$, the device output goes low to $I_{CC(LOW)}$. The midpoint between $B_{OP}$ and $B_{RP}$ is denoted as the offset, $B_{OFF}$, of the device. A device with 0 G $B_{OFF}$ indicates that $B_{OP} = –B_{RP}$. The difference in the magnetic operate and release points is the hysteresis, $B_{HYS}$, of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

Removal of the magnetic field will leave the device output latched in $I_{CC(HIGH)}$ if the last crossed switch point is $B_{OP}$, or latched in $I_{CC(LOW)}$ if the last crossed switch point is $B_{RP}$.

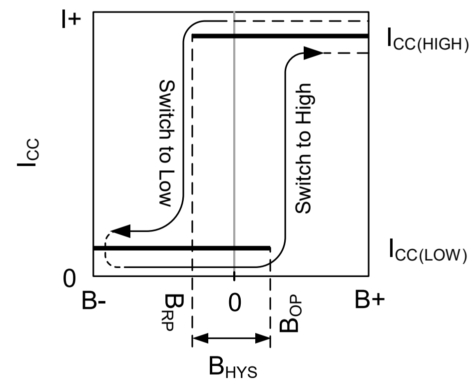


**Figure 2: Switching Behavior of Latches**

**On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength, and the B– direction indicates increasing north polarity field strength.**

### Two-Wire Interface

The voltage-controlled current output is configured for two-wire applications, requiring one less wire for operation than switches with the traditional open-collector output. Additionally, the system designer inherently gains basic diagnostics because there is always output current flowing, which should be in either of two ranges under normal operation, shown in Figure 3 as $I_{CC(HIGH)}$ and $I_{CC(LOW)}$. Any current level not within these ranges indicates a fault condition.

If $I_{CC} > I_{CC(HIGH)}$(max), then a short condition exists, and if $I_{CC} < I_{CC(LOW)}$(min), then an open condition exists. Any value of $I_{CC}$ between the allowed ranges for $I_{CC(HIGH)}$ and $I_{CC(LOW)}$ indicates a general fault condition. A user may choose to set a range of allowable supply current values based on the operating supply voltage. This unique two-wire interface protocol is backward compatible with legacy systems using two-wire switches.

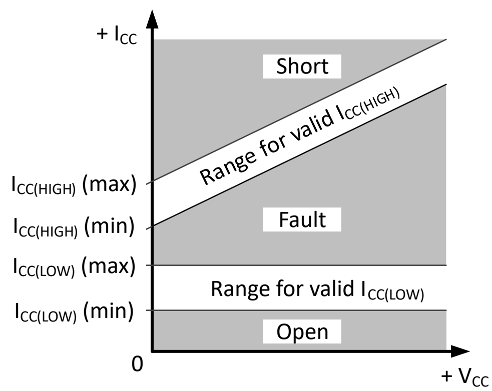


**Figure 3: Diagnostic Characteristics of Supply Current Values**

### Output Polarity

The output signal may be read as a voltage, $V_{SENSE}$, by using a sense resistor, $R_{SENSE}$, placed either in series with VCC or with GND (refer to Figure 1). When $R_{SENSE}$ is placed in series with GND, the output signal voltage is in phase with $I_{CC}$. When $R_{SENSE}$ is placed in series with VCC, the output signal voltage is inverted relative to $I_{CC}$. Table 1 lists possible combinations of sense resistor placement and resulting logic states.

**Table 1: Output Signal Polarity**

| $R_{SENSE}$ Location (Refer to Figure 1) | $I_{CC}$ State* | $V_{SENSE}$ Logic State |
|---|---|---|
| High Side (VCC Pin Side) | High | Low |
| | Low | High |
| Low Side (GND Pin Side) | High | High |
| | Low | Low |

* $I_{CC}$ state High ($I_{CC(HIGH)}$) corresponds with B > $B_{OP}$ and Low ($I_{CC(LOW)}$) corresponds with B < $B_{RP}$.



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## POWER-ON/OFF BEHAVIOR

Device power-on occurs once $t_{ON}$ has elapsed. During the time prior to $t_{ON}$, and after $V_{CC} \geq V_{CC}$(min), the output state is $I_{CC(HIGH)}$. After $t_{ON}$ has elapsed, the output will correspond with the applied magnetic field for $B > B_{OP}$ or $B < B_{RP}$. See Figure 4 for an example.

Powering-on the device in the hysteresis range (less than $B_{OP}$ and higher than $B_{RP}$) will give an output state of $I_{CC(HIGH)}$. The correct state is attained after the first excursion beyond $B_{OP}$ or $B_{RP}$.

During conditions where the supply voltage drops below $V_{CC}$(min) but remains above $V_{UVLO}$, (e.g. $V_{UVLO} < V_{CC} < V_{CC}$(min)), the IC will continue to switch, however $B_{OP}/B_{RP}$ specifications are not guaranteed. The region between the $V_{UVLO}$ and $V_{SD}$ thresholds is where the IC will disengage operation of the output and revert to the power-on state. If the supply voltage falls below $V_{SD}$, the output will become invalid and the device turns off.

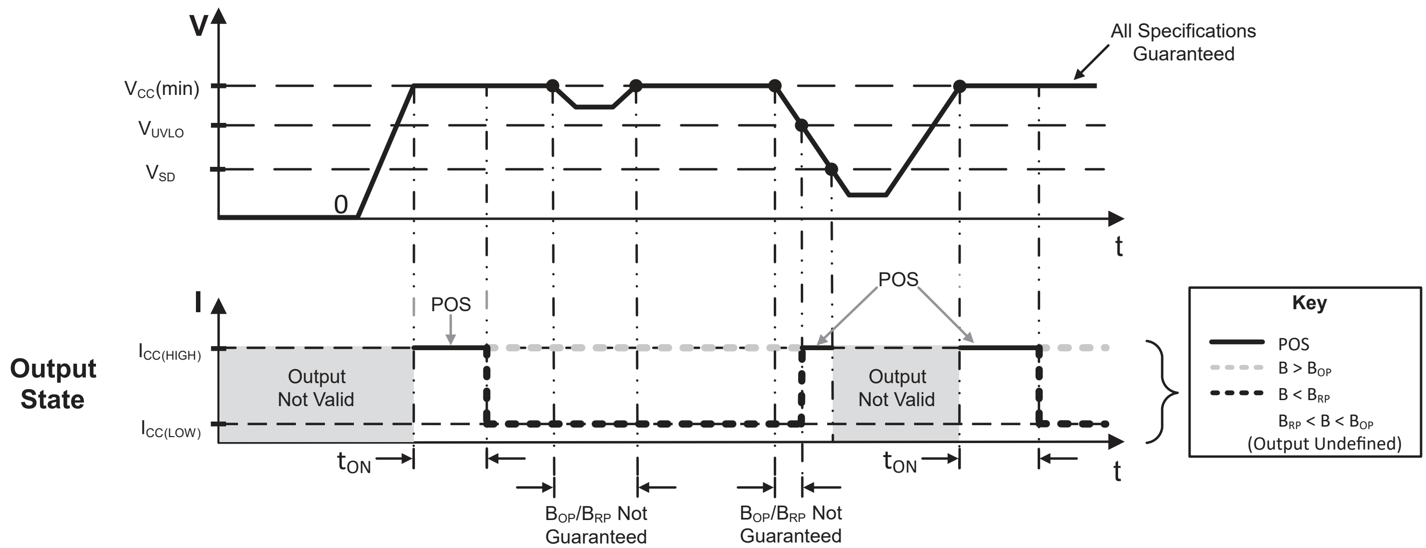


**Figure 4: Power-On and Power-Off Timing Diagram**



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## APPLICATIONS

The APS12170 has a current mode output that corresponds with the plot in Figure 5. The high supply current level, $I_{CC(HIGH)}$, is a function of the system supply voltage, $V_{CCS}$, and the supply voltage across the device pins, $V_{CC}$. The low supply current level, $I_{CC(LOW)}$, is regulated to within a narrow range of 4.5 to 7.5 mA.

These devices are sensitive in the direction perpendicular to the branded face, as depicted in Figure 6.

For further information, extensive applications information on magnets and Hall-effect sensors is available in:

- *Hall-Effect IC Applications Guide, AN27701,*
- *Hall-Effect Devices: Guidelines for Designing Subassemblies Using Hall-Effect Devices AN27703.1*
- *Soldering Methods for Allegro's Products – SMD and Through-Hole, AN26009*
- *Digital Position Sensor ICs—Continuous-Time to Chopper-Stabilized Cross-Reference Guide, AN296125*

All are provided on the Allegro website:

**https://www.allegromicro.com/en/insights-and-innovations**

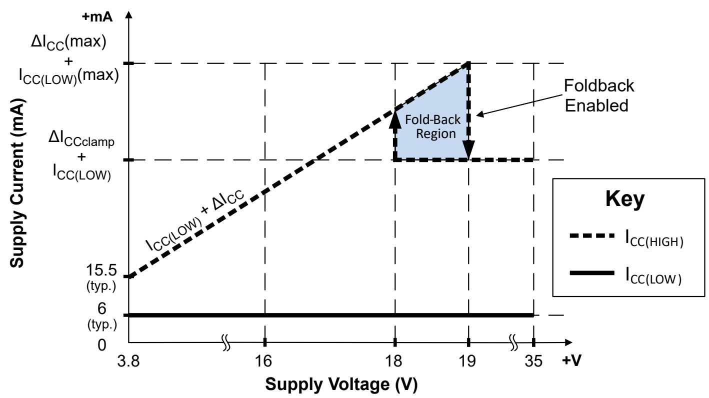


**Figure 5: Supply Current Diagram (using circuits shown in Figure 1)**

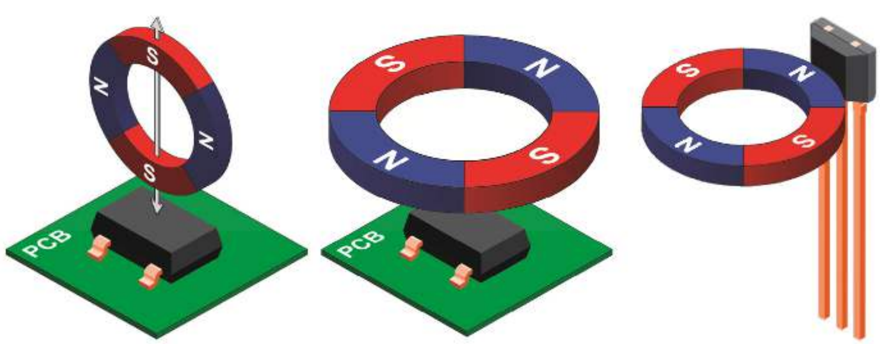


**Figure 6: Sensing Configurations**



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## CONTINUOUS-TIME BENEFITS

Continuous-time devices, such as the APS12170, offer the fastest available power-on settling time and frequency response. Battery management is an example where continuous-time is often required. In these applications, $V_{CC}$ is duty-cycled with a very small duty cycle in order to conserve power (refer to Figure 7). The duty cycle is controlled by the power-on time, $t_{ON}$, of the device. Because continuous-time devices have the fastest power-on time, compared to their chopper-stabilized counterpart, they are the clear choice for such applications.

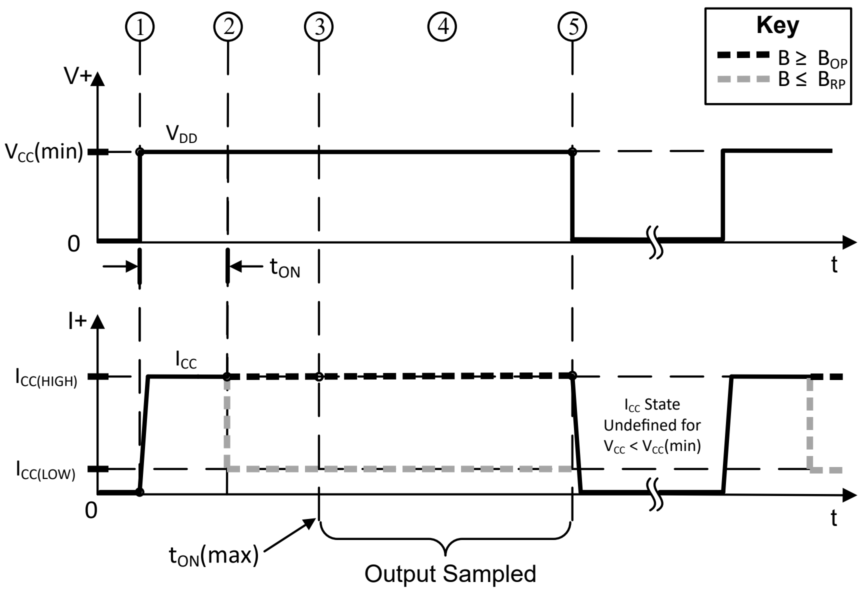


**Figure 7: Continuous Time Operation Example**

This figure illustrates the use of a technique which duty-cycles the VCC power supply in order to conserve battery power

1. Power is applied to the device.
2. The output assumes a valid state at a time prior to the maximum Power-on Time, $t_{ON}$(max).
3. The maximum power-on time, $t_{ON}$(max), has elapsed the device output is now valid.
4. After the output is valid, the control unit reads the output.
5. Power is removed from the device.



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## POWER DERATING

The device must be operated below the maximum junction temperature of the device, $T_J$(max). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating $T_J$. (Thermal data is also available on the Allegro MicroSystems website.)

Thermal Resistance (junction to ambient), $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices, traces, and board layout. Thermal resistance from the die junction to the device case, $R_{\theta JC}$, is a relatively small component of $R_{\theta JA}$. Ambient air temperature, $T_A$, and air motion are significant external factors in determining a reliable thermal operating point.

The APS12170 is permitted to operate up to $T_J$ = 175°C. An operating device will increase $T_J$ according to equations 1, 2, and 3 below. This allows an estimation of the maximum ambient operating temperature.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: $T_A$= 25°C, $V_{CC}$ = 12 V, $I_{CC}$ = 6 mA, and $R_{\theta JA}$ = 165°C/W, then:

$$P_D = (V_{CC} \times I_{CC}) = (12\ V \times 6\ mA) = 72\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 72\ mW \times 165°C/W = 11.9°C$$

$$T_J = T_A + \Delta T = 25°C + 11.9°C = 36.9°C$$

A worst-case estimate for the maximum ambient temperature permitted during operation can be completed by considering the maximum die junction temperature and thermal components.

For example, given the conditions $R_{\theta JA}$ = 228°C/W, $T_J$(max) = 175°C, $V_{CC}$(max) = 13 V, $I_{CC}$(max) = 42.3 mA, the power dissipation required for the IC supply is shown below:

$$P_D = V_{CC} \times I_{CC} = 13\ V \times 42.3\ mA = 550\ mW$$

Next, by inverting using equation 2:

$$\Delta T = P_D \times R_{\theta JA} = 550\ mW \times 228°C/W = 125.4°C$$

Finally, by inverting equation 3 with respect to voltage:

$$T_A(est) = T_J(max) - \Delta T = 175°C - 125.4°C = 49.6°C$$

In the above case, there is sufficient power dissipation capability to operate up to $T_A$(est). The example indicates that $T_A$(max) can be as high as 49.6°C without exceeding $T_J$(max). However, the $T_A$(max) rating of the devices is 150°C; the APS12170 performance is not guaranteed above $T_A$ = 150°C.



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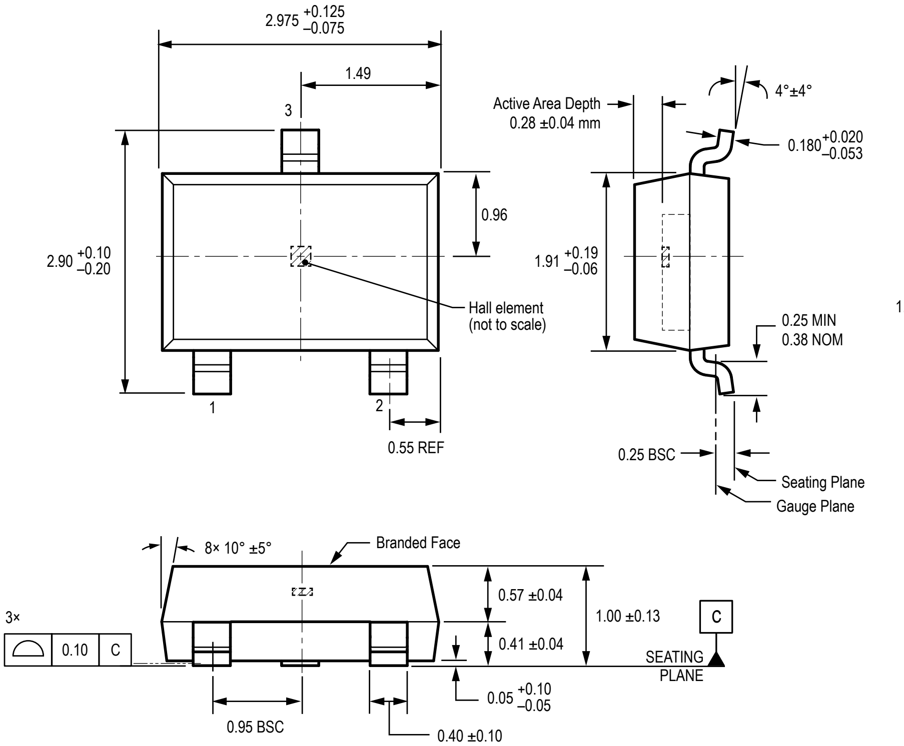
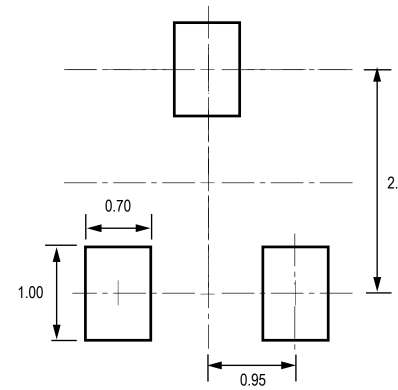
## Package LH, 3-Pin (SOT-23W)

### For Reference Only – Not for Tooling Use

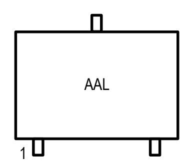
(Reference Allegro DWG-0000628, Rev. 1)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown




PCB Layout Reference View

All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances




Standard Branding Reference View 1

Branding scale and appearance at supplier discretion



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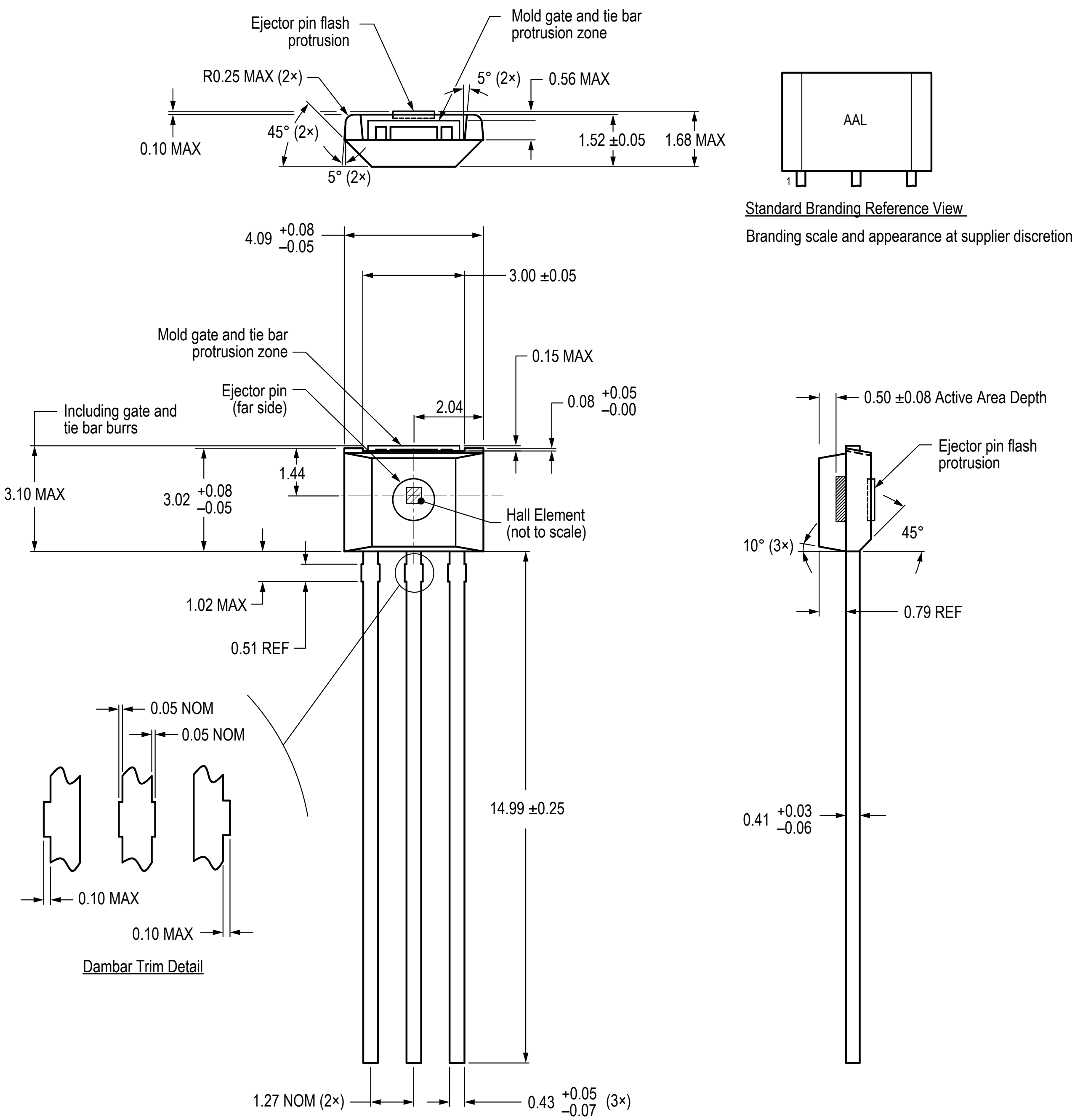
## Package UA, 3-Pin SIP

**For Reference Only – Not For Tooling Use**

(Reference DWG-0000404, Rev. 1)
NOT TO SCALE
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown



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### Revision History

| Number | Date | Description |
|---|---|---|
| – | February 24, 2021 | Initial release |
| 1 | February 21, 2022 | Updated package drawings (pages 13-14) |



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