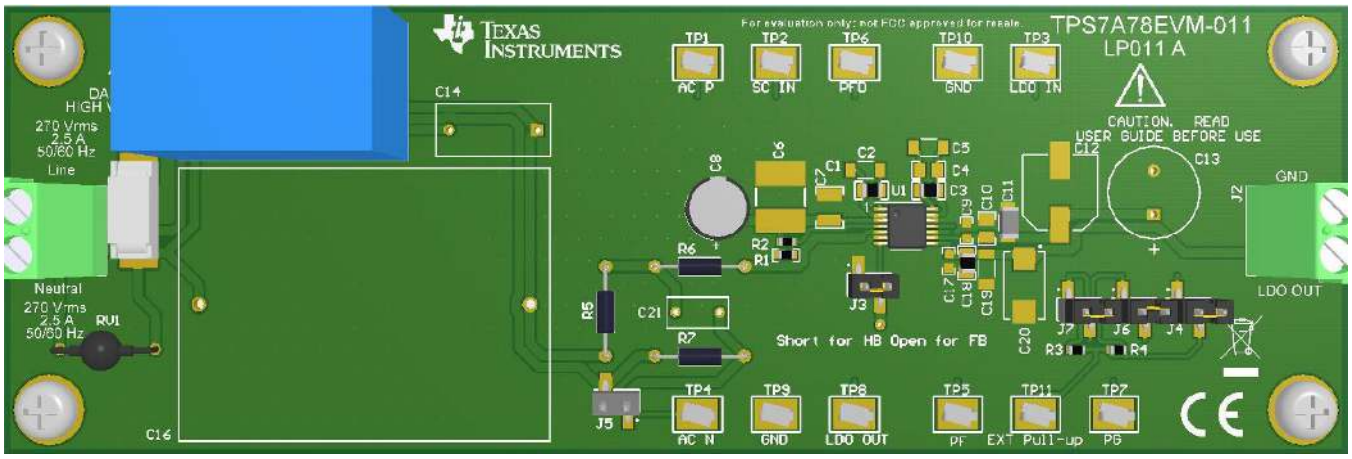
TPS7A78EVM-011 Evaluation module



This user's guide describes the operational use of the TPS7A78EVM-011 evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TPS7A78, non-isolated smart linear voltage regulator (LDO). Included in this user's guide are setup and operating instructions, thermal and layout guidelines, a printed circuit board (PCB) layout, a schematic diagram, and a bill of materials (BOM).

Throughout this document, the terms *demonstration kit*, *evaluation board*, and *evaluation module* are synonymous with the TPS7A78EVM-011.

The following related documents are available through the Texas Instruments web site at www.ti.com.

Table 1. Related Documentation

Device	Literature Number
TPS7A78	SBVS343

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Trademarks

1 General Texas Instruments High Voltage Evaluation (TI HV EVM) User Safety Guidelines

Always follow TI's setup and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center http://support/ti./com for further information.

Save all warnings and instructions for future reference.

WARNING

Failure to follow warnings and instructions may result in personal injury, property damage or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is *intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments.* If you are not suitable qualified, you should immediately stop from further use of the HV EVM.

1. Work Area Safety
   a. Keep work area clean and orderly.
   b. Qualified observer(s) must be present anytime circuits are energized.
   c. Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
   d. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
   e. Use stable and nonconductive work surface.
   f. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety
   As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
   a. De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
   b. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment connection, and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
   c. After EVM readiness is complete, energize the EVM as intended.

WARNING

While the EVM is energized, never touch the EVM or its electrical circuits, as they could be at high voltages capable of causing electrical shock hazard.

3. Personal Safety
   a. Wear personal protective equipment (for example, latex gloves or safety glasses with side shields) or protect EVM in an adequate lucent plastic box with interlocks to protect from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

2 Introduction

Texas Instruments' TPS7A78EVM-011 helps design engineers evaluate the operation and performance of the TPS7A78 smart linear voltage regulator for possible use in their own circuit application. This particular EVM is intended for evaluation purposes and is not intended to be an end product. The EVM configuration contains a single 3.3-V output regulator optimized for e-metering applications. The TPS7A78EVM-011 regulates V_{AC} supply to 3.3-V DC supply and can source up to 27 mA (max) current.

The EVM also features a power-fail detection signal and a power-good indication signal to warrant a V_{AC} supply failure and to indicate to a microcontroller (MCU) that the regulated DC voltage is greater than 90% of the targeted regulation DC voltage.

2.1 Before You Begin

This evaluation module is not encapsulated and has exposed terminals with voltages that are connected to the main AC supply; the following warnings are noted for the safety of anyone using or working close to the TPS7A78EVM-011. Observe all safety precautions.

WARNING

Failure to adhere to these steps or to not heed the safety requirements at each step may lead to shock, injury, and damage to the hardware. Texas Instruments is not responsible or liable in any way for shock, injury, or damage caused by negligence or failure to heed advice. If you are not trained in the proper safety of handling and testing power electronics please do not test this evaluation module.

	**Danger High Voltage**	**Electric shock possible when connecting board to live wire. Board should be handled with care by a professional.** **For safety, use of isolated test equipment with overvoltage/overcurrent protection is highly recommended.**

WARNING

Danger: HIGH VOLTAGE! This evaluation board is intended for professional use only. This board has exposed high voltages. Do not operate this board without proper high-voltage/high-current safety practices. Read this user guide carefully before testing with TPS7A78EVM-011. Use floating measurement equipment such as high-voltage differential scope probes and see Section 5 and Section 6 for proper EVM setup and test equipment connection.

3 Electrical Performance Specifications

Table 2 lists the electrical specifications for the TPS7A78EVM-011 evaluation board.

Table 2. TPS7A78EVM-011 Electrical Performance Specifications(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{AC}	AC input (RMS)		70	120		V
			70	230		
	Wall plug (RMS)			120		
				230		
f_{AC}	Line frequency		45	60/50		Hz
$P_{STANDBY}$	Standby power	V_{AC} = 120 V (60 Hz), I_{OUT} = 0 mA, R6 and R7 are shorted; see Section 4.			104	mW
OUTPUT CHARACTERISTICS						
V_{LDO_OUT}	Output voltage	V_{AC} = 120 V (60 Hz)	3.201	3.3	3.399	V
V_{LDO_OUT} ripple	Output ripple voltage	V_{AC} = 120 V (60 Hz)		10		mVpp
I_{OUT}	Output current	V_{AC} = 120 V (60 Hz)	16(2)	27	55(3)	mA
SYSTEMS CHARACTERISTICS						
	Standby power	V_{AC} = 120 V (60 Hz), I_{OUT} = 0 mA		104		mW

(1) All measurements are done with a half-bridge (HB) default EVM setting (unless otherwise noted).
(2) Output current level is determined by the size of the cap-drop (C_{15}), the size of the bulk capacitor (C_8), and the device configuration. When V_{AC} is 70 V (60 Hz), the EVM can source 16 mA (max); see Section 5 for EVM configuration and Section 6 for proper connection of test equipment.
(3) When V_{AC} is 120 V (60 Hz), the EVM can source 55 mA (max) with a full-bridge configuration.

4 Schematic

Figure 1 shows a schematic for the TPS7A78EVM-011.

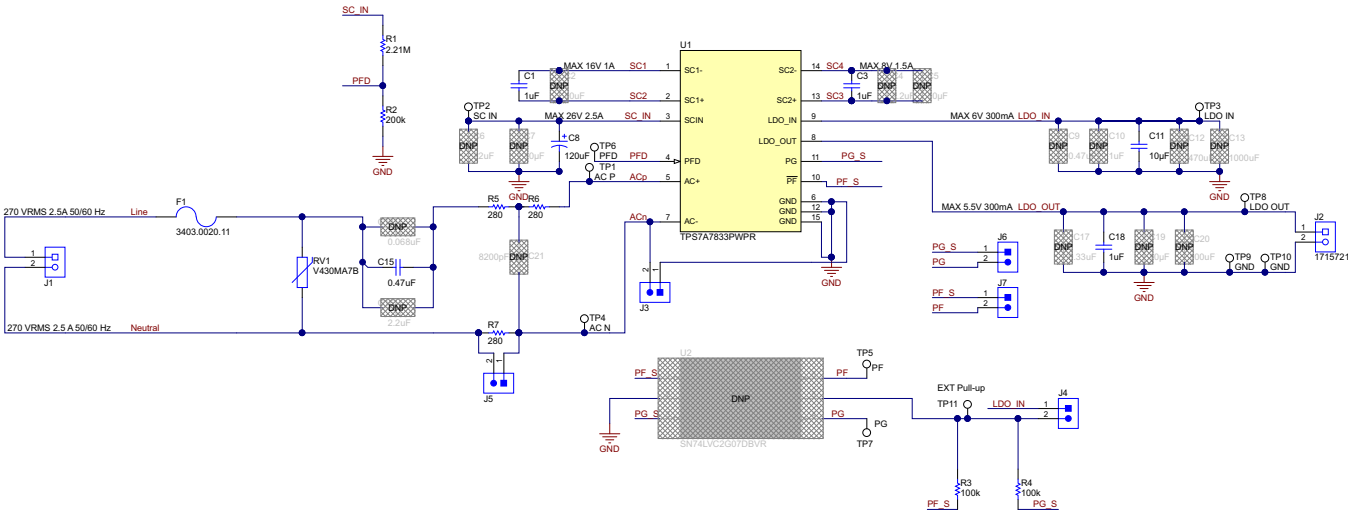

Figure 1. TPS7A78EVM-011 Schematic

5 EVM Setup

This section describes how to properly connect and setup the TPS7A78EVM-011, including the jumpers and connectors on the EVM board. See Section 6 for the proper connections of test equipment.

5.1 Input/Output Connectors and Jumpers Descriptions

5.1.1 J1: V_{AC}

Input AC power-supply connector. Ensure that the AC input power supply is turned off before making the connection to the EVM. The AC supply line lead must be connected to the line pin on the J1 connector, whereas the neutral lead must be connected to the neutral pin on the J1 connector to ensure proper operation of the TPS7A78 LDO.

NOTE: If the AC supply line and neutral leads are flipped when connected to the J1 connector, then the TPS7A78 device GND pin is referenced to the AC supply line and only floating measurement equipment must be used.

5.1.2 J3: Full-Bridge (FB) and Half-Bridge (HB) Configurations

This EVM comes configured for half-bridge (HB) configuration usage, when J3 jumper is connected. However, to use the full-bridge (FB) configuration, leave jumper J3 open and see Section 6 for the proper connections of test equipment.

HB configuration is achieved by tying V_{AC} neutral to the TPS7A78 device GND pin, whereas in FB configuration V_{AC} neutral is connected to the AC– pin and the device GND pin track V_{AC} neutral and therefore must be floating. See Section 6 for the proper connections of test equipment.

NOTE: When FB configuration is used, the device GND must float (that is, the device GND must not be tied to Earth-GND). Floating the device GND is required to limit the shunted AC current (the excess AC current charging the bulk capacitor C8) while the device active bridge shunts this current to circulate this current back to neutral. Jumper J5 is open by default to limit the circulating current though neutral when the device GND is intentionally or accidentally connected to Earth-GND, such as when using regular scope probes or a bench digital multimeter (DMM) where such equipment have their GNDs always tied to Earth-GND. Use floating measurement equipment when the FB EVM configuration is used.

5.1.3 J4: Power-Good Indication and Power-Fail Detection Pullup Voltage

Jumper J4 pulls up the open-drain power-good and power-fail detection indicators to V_{LDO_IN} by athe default EVM setting. An external DC pullup voltage can be used via test point TP11; however, jumper J4 must be open in order not to short the external pullup voltage to the LDO_IN pin.

NOTE: When an external DC voltage is used to pullup the PG and PF pins, this external supply must be a floating supply when FB configuration is used.

For HB configuration, the device GND can be tied to Earth-GND, and the external pullup supply can be referenced to the device GND.

5.1.4 J5: Second Surge Resistor (R7) Jumper

This EVM has three surge resistors, R5, R6, and R7. However, only one resistor R5 is required. R7 is needed when the device GND is tied to Earth-GND intentionally or accidentally when using regular scope probes.

R6 was populated for test purposes only. Capacitor C21 is a placeholder for conducting electromagnetic interference (EMI) filtering.

5.1.5 J6 and J7: Power-Good (PG) and Power-Fail (PF) Signals

The TPS7A78 device has two open-drain signals (power-good and power-fail) that are both pulled up to V_{LDO_IN} by default.

Becuase of the high-impedance open-drain logic, the AC supply frequency noise may be present on those signals when they are high. A low-impedance digital buffer isolation circuit is recommended, such as the U2 device in Section 4, to obtain noise-free PG ans PF signals. Jumpers J6 and J7 connect the device PG and PF signals directly to the TP7 and TP5 test points because the digital buffer circuit is not populated with the default EVM setting.

NOTE: When high-voltage differential scope probes are used when testing the TPS7A78EVM-011, the digital buffer circuit U2 in Section 4 is recommended to be populated and jumpers J6 and J7 must be open to obtain noise-free PG and PF signals.

5.1.6 J2: V_{LDO_OUT}

Regulated DC output voltage connector.

NOTE: This EVM is optimized for a 3.3-V output and a 27-mA to 55-mA (max) load current. If your application requires higher output current, see the TPS7A78 *Application and Implementation* section for the proper setting of your application requirement.

5.2 Test Points

Table 3 lists the test points for the TPS7A78EVM-011.

Table 3. Test Point Functions

TEST POINTS	NAME	DESCRIPTION
TP1	AC_P	AC supply line input to the device after the cap-drop capacitor and surge resistor.
TP2	SC_IN	Rectified DC voltage pin; see the TPS7A78 *Application and Implementation* section for the proper setting of your application requirement.
TP3	LDO_IN	Charge-pump output pin.
TP4	AC_N	AC supply neutral input to the device after the cap-drop capacitor and surge resistor.
TP5	PF	Power-fail pin.
TP6	PFD	Power-fail detect pin.
TP7	PG	Power-good pin.
TP8	LDO_OUT	Regulated DC output pin.
TP9	GND	Device GND connected to the thermal pad.
TP10	GND	

5.3 Performance Data for the TPS7A78EVM-011

As specified in Section 5.1.2, this EVM is configured for an HB 3.3-V output voltage and 27 mA of output current, and the EVM can also be configured for FB use.

5.3.1 Startup

Figure 2 to Figure 5 show various start-up plots for the TPS7A78EVM-011.

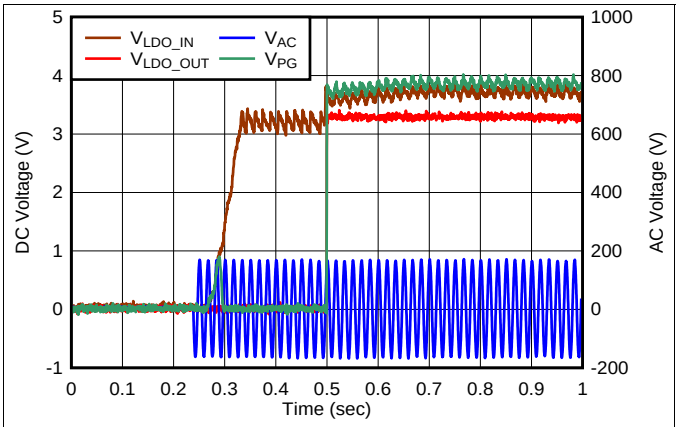

Figure 2. Startup: 120-V_{AC} Half-Bridge (HB) and 27-mA Load Current

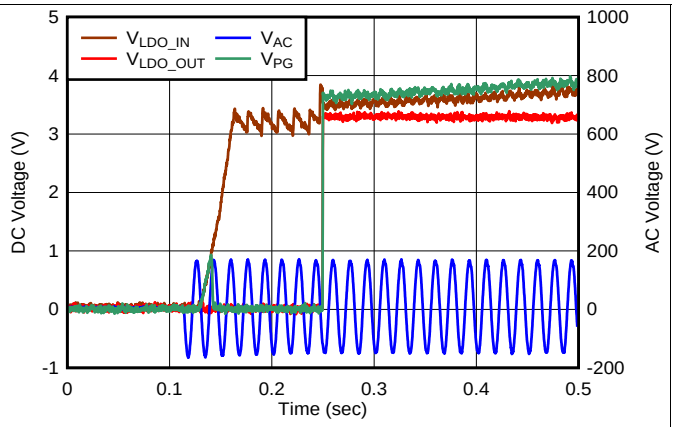

Figure 3. Startup: 120-V_{AC} Full-Bridge (FB) and 55-mA Load Current

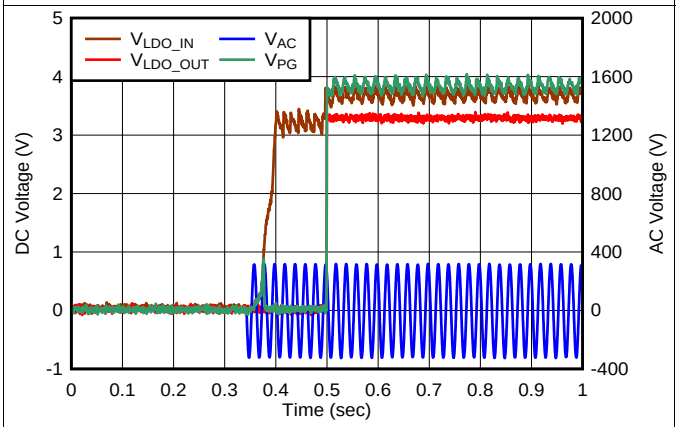

Figure 4. Startup: 230-V_{AC} Half-Bridge (HB) and 27-mA Load Current

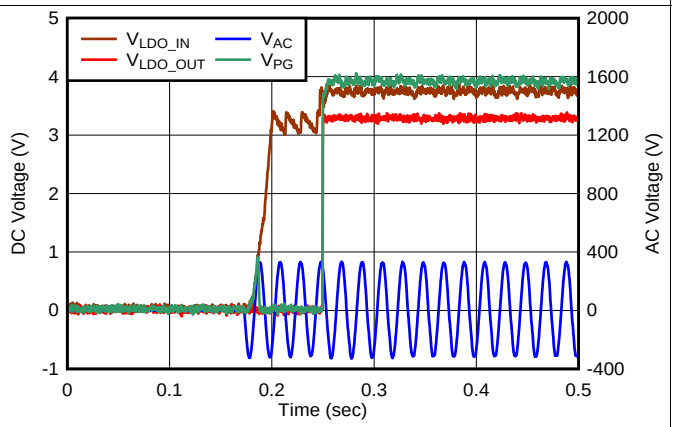

Figure 5. Startup: 230-V_{AC} Full-Bridge (FB) and 55-mA Load Current

In Figure 6, the power-fail detect (PFD) trace and resistor divider was placed close to the AC_P pin and as a result the power-fail (PF) signal glitches whenever there is a shunt event; see the TPS7A78 *Feature Description* section for details on the device active bridge control. Figure 6 shows the PF signal glitch.

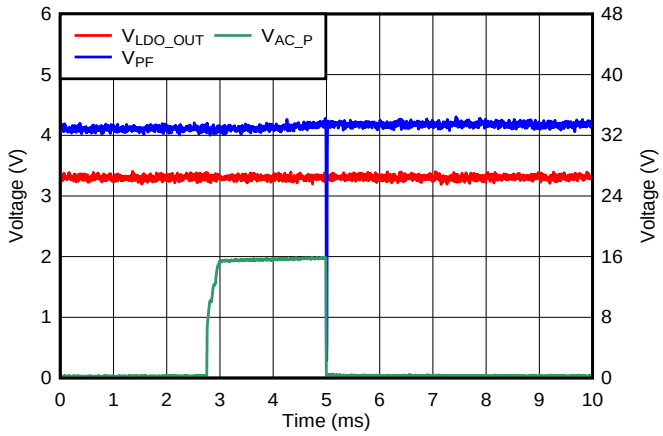

Figure 6. PF Signal Glitch

5.4 Soldering Guidelines

To avoid damaging the LDO, use a hot-air system for any solder rework to modify the EVM for the purpose of repair or other application reasons.

6 Equipment Connection and Operation

6.1 Equipment Connection

Connect test equipment as described in this section and follow the listed steps to properly take measurements:

NOTE: The FB configuration for the EVM requires a differential measurement. The TPS7A78 device GND must not be tied to Earth-GND.

6.1.1 Full-Bridge (FB) Test Equipment Connection

Figure 7 shows an FB connection diagram.

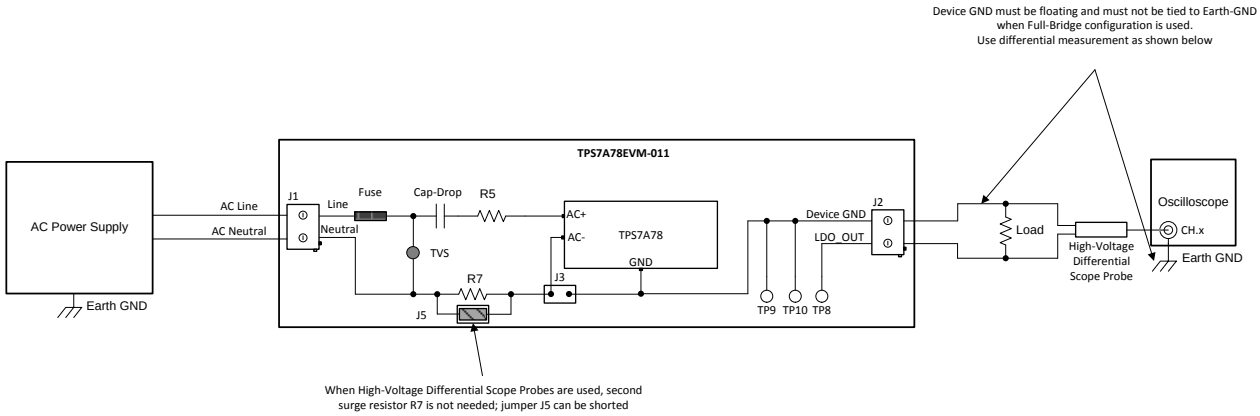

Figure 7. Proper Test Equipment Connections for the FB EVM Configuration

6.1.2 Half-Bridge (HB) Test Equipment Connection

Figure 8 shows an HB connection diagram.

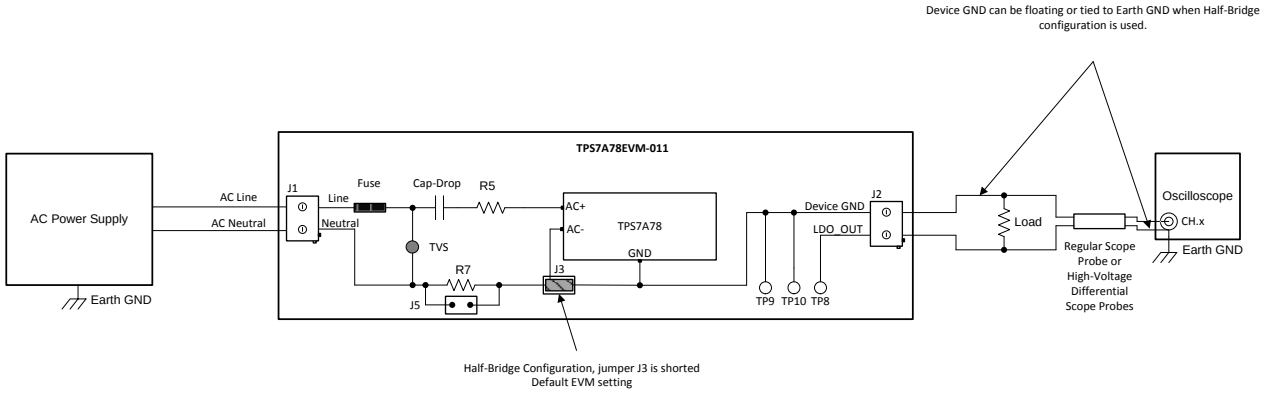

Figure 8. Proper Test Equipment Connections for the Half-Bridge (HB) EVM Configuration

To ensure proper connectivity:

1. Set the AC input power supply to 120 V_{AC} and 60 Hz, and turn the power supply off.
2. Connect the line lead from the AC power supply to the line pin on the J1 connector of the EVM.
3. Connect the neutral lead from the AC power supply to the neutral pin on the J1 connector of the EVM.
4. Connect a 0-mA to 27-mA load between J2 connecter terminals of the EVM.

6.2 Equipment Operation

Operate the test equipment using the following steps:

1. Turn on the AC power supply.
2. Vary the respective load and input voltage, as necessary, for test purposes.

7 PCB Layout

Figure 9 to Figure 11 illustrate the PCB layout for this EVM.

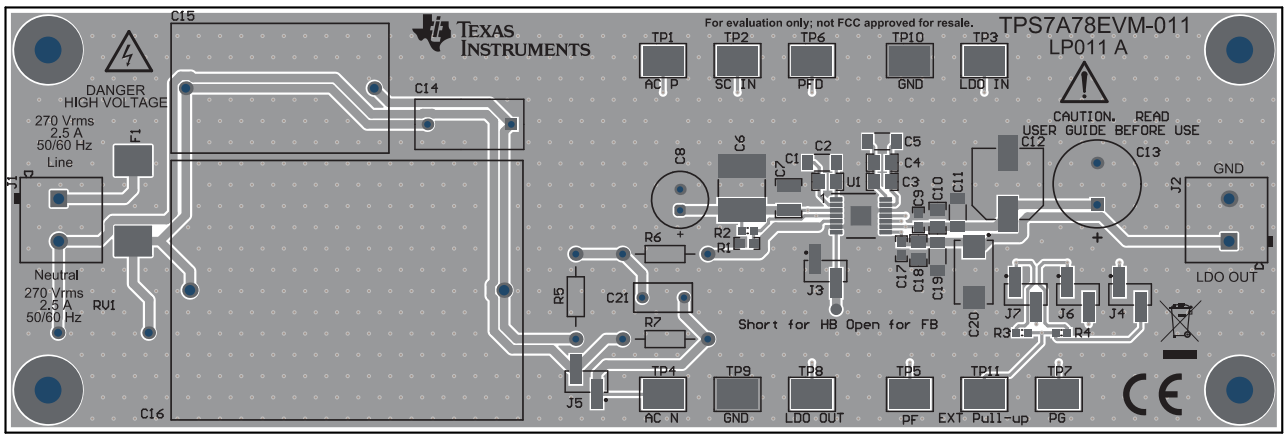

Figure 9. Assembly Layer

NOTE: The silk screens for resistors R1 and R2 are flipped in Figure 9.

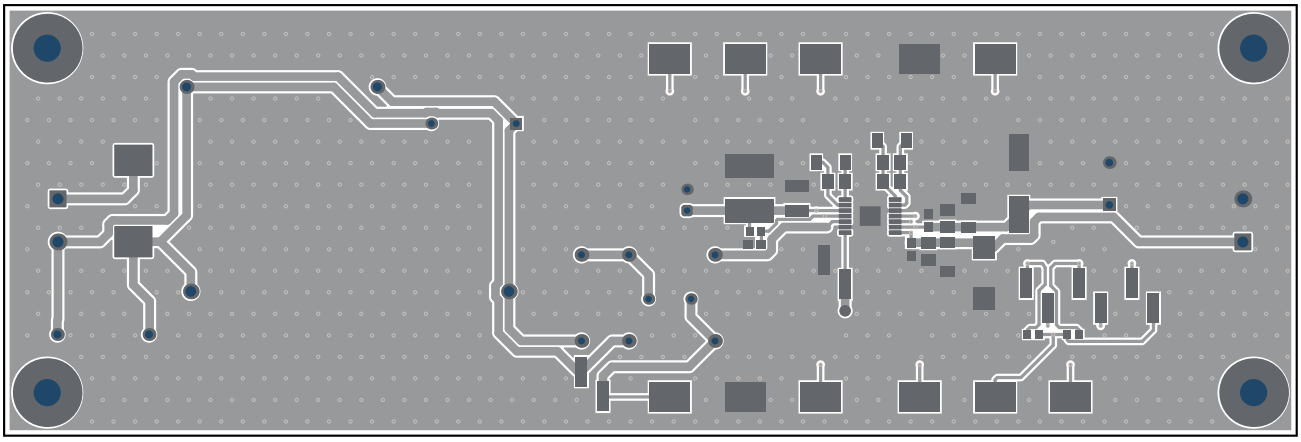

Figure 10. Top Layer Routing

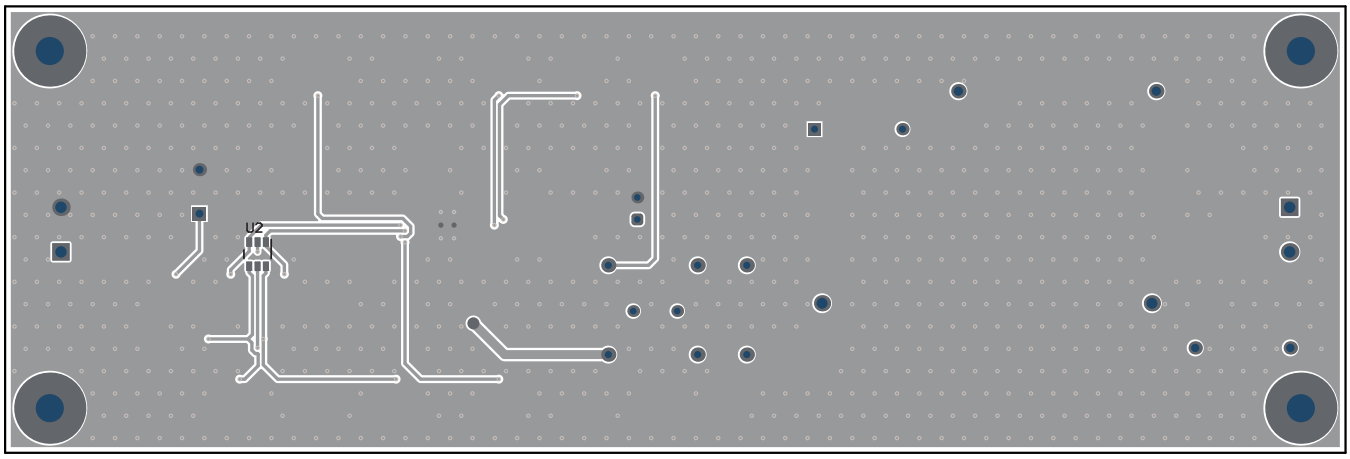

Figure 11. Bottom Layer Routing

8 Bill of Materials (BOM)

Table 4 shows the BOM for this EVM.

Table 4. TPS7A78EVM-011 BOM(1)(2)(3)(4)

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		LP011	Any		
C1	1	1 uF	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0805	0805	GRM21BR71H105KA12L	MuRata		
C3	1	1 uF	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0805	0805	GRM21BR71H105KA12L	MuRata		
C8	1	120 uF	CAP ALUM 120UF 20% 35V T/H	TH	35ZLQ120MEFC6.3X11	Rubycon		
C11	1	10 µF	CAP, CERM, 10 µF, 25 V,+/- 10%, X7R, 1206	1206	C3216X7R1E106K160AB	TDK		
C15	1	0.47 uF	CAP, Film, 0.47 uF, 1000 V, +/- 20%, TH	TH	PHE844RD6470MR30L2	Kemet		
C18	1	1 uF	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0805	0805	GRM21BR71H105KA12	MuRata		
F1	1	2.5 A	Fuse, 2.5 A, 250VAC/VDC, SMD	SMD	3403.0020.11	Schurter		
J1, J2	2		Terminal Block, 5.08 mm, 2x1, TH	TH	1715721	Phoenix Contact		
J3, J4, J5, J6, J7	4		Header, 100mil, 2x1, Tin, SMD	SMD	TSM-102-01-T-SV-P-TR	Samtec		
R1	1	2.21 M	RES, 2.21 M, 1%, 0.1 W, 0603	0603	RC0603FR-072M21L	Yageo		
R2	1	200 k	RES SMD 200K OHM 1% 1/10W 0603	0603	RC0603FR-07200KL	Yageo		
R3, R4	2	100 k	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100KFKEA	Vishay-Dale		
R5, R6, R7	3	280	RES 280 OHM 1/4W 1% AXIAL	TH	CMF50280R00FHEB	Vishay-Dale		
RV1	1		VARISTOR 430V 100A SOD83A AXIAL	TH	V430MA7B	Littelfuse Inc.		
SH-J3, SH-J4, SH-J6, SH-J7	4	1x2	Shunt, 100 mil, Gold plated, Black	Shunt	969102-0000-DA	3M	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11	11		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone		
U1	1		100-mA Non-Isolated Line Power Voltage Regulator, PWP0014C (HTSSOP-14)	HTSSOP-14	TPS7A7833PWPR	Texas Instruments		Texas Instruments

(1) These assemblies are ESD sensitive, observe ESD precautions.
(2) These assemblies must be clean and free from flux and all contaminants. Use of no-clean flux is not acceptable.
(3) These assemblies must comply with workmanship standards IPC-A-610 Class 2.
(4) Unless otherwise noted in the *Alternate Part Number* or *Alternate Manufacturer* columns, all parts may be substituted with equivalents.

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