CA3210, CA3223

TV Horizontal/Vertical Countdown Digital Sync System

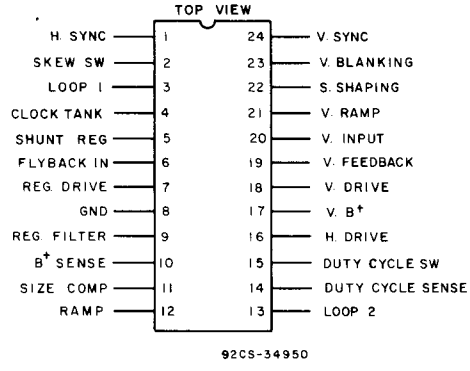
For 525-Line (CA3210E) or 625-Line (CA3223E) Operation

Features:
- *Horizontal Driver*
- *Two Phase-Lock Loops*
- *Horizontal Oscillator*
- *Vertical Countdown*
- *Vertical Blanking*
- *Vertical Ramp Generator*
- *Pulse-Width Voltage Regulator*
- *Tape-Recorder Skew Compensation*
- *Internal Shunt Regulator*

The RCA-CA3210E and CA3229E* are MSI integrated-circuit digital sync systems, designed for use in consumer TV applications which combine horizontal oscillator and vertical countdown sections, as well as a pulse-width voltage-regulator driver for color or monochrome receivers. They feature dual-mode operation and accept either standard signals or nonstandard signals. An automatic mode-recognition system forces the operation into the nonsynchronous mode for non-standard sync signals. The CA3210E is intended for use with 525-line systems and the CA3223E is intended primarily for use with 625-line systems. The CA3223E will also operate in the direct sync mode with 525-line signal sources.

The CA3210E and CA3223E are supplied in the 24-lead dual-in-line plastic package.

* Formerly RCA Dev. Type Nos. TA10955 and TA11324, respectively.



TERMINAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY:
- Terminal 17 ..... 10 V
- Terminal 22 ..... 15 V
- Terminal 5 — Shunt Regulator ..... 30 mA

DEVICE DISSIPATION:
- Up to +70°C ..... 695 mW
- Above +70°C ..... Derate linearly at 8.7 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating ..... 0 to +70°C
- Storage ..... −55 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

File Number **1361**

ELECTRICAL CHARACTERISTICS at T_A=+25 to +70° C

See Fig. 3, Test Points 4 and 18=27 V, Test Point 16=2.3 V, and Test Point 20=10 V.

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		Min.	Max.	
Supply Current	Note 1, Test pt. 5=9 V, Test pt. 4=adjusted	8	16	mA
Shunt Regulator Output	Test pt. 5	8.7	11	V
$4f_H$ Coincidence	Note 2, Test pin 21	24	45	μs
V. Count (÷262.5) *	Note 3, Test pin 21	16.6	16.7	ms
V. Count (÷312.5) **		19.9	20.1	
V. Count 7 Fields after Loss of Sync:	Note 4, S1=2, Test pin 21			
(÷262.5) *		16.6	16.7	
(÷312.5) **		19.9	20.1	
V. Count 8 Fields after Loss of Sync:	Note 5, S1=2, Test pin 21			
(÷296) *		18.7	18.9	
(÷232.5) **		22	22.2	
V. Count Low	Note 6, S1=2, Test pin 21			
(÷232) *		14.6	14.9	
(÷232.5) **		14.7	15	
V. Ramp Pulse Width at 7 V *	Note 7, Test pin 21	503	516	μs
**		506	518	
V. Blanking Pulse Width *	Note 8, Test pin 23	1.140	1.148	ms
**		1.148	1.156	
V. Blanking Sat. Voltage	Note 9, Test pin 21	1.2	1.8	V
V. Sync SVC SW.	Note 10, Test pt. 20=0.7 V, Test pin 21	12	14	
Vertical Loop Gain:	Note 11(a),(b)			
Low	Test pin 18=0.3 V	11	11.7	
Medium	Test pin 18=4.5 V	10.89	11.81	
High	Test pin 18=8 V	10.89	11.85	
Regulator Driver Out	Test pin 7	6.2	7.5	
Horizontal Pulse Width *	Note 12, Test pin 16	31.5	34.6	ns
**		31.7	34.9	
Horizontal Drive Shutdown	Note 13, Test pin 16, Clock disabled	4.9	5.1	V
Horizontal Drive Sat. Voltage	Note 14, Test pin 16 at 15 mA	—	0.42	
Nominal Loop Phase	Note 15, Test pin 16	11.25	13.6	ns
Ramp Voltage (p-p)	Test pin 12	3.8	7.5	V_{p-p}

*CA3210E—525-Line system.
**CA3223E—625-Line system.

NOTES:

1. Adjust 27-V supply for pin 5 voltage=9 V ± 0.1 V and measure current into pin 5.
2. Measure of the time delay between the output pulse at pin 21 and the input vertical sync at J1.
3. Measure the period of the waveform at pin 21. The frequency at pin 16 should be 262.5* or 312.5** times the frequency at pin 21. This corresponds to a frequency of 59.939* or 50.000** Hz at 21 when 16 is 15734* or 15625** Hz.
4. Remove vertical sync (SW1=2), and remeasure period of waveform at pin 21 6 fields later (100* or 120** ms). Period should remain the same as in previous test.
5. Keep vertical sync off and remeasure period of waveform at pin 21 after 2 additional fields. The frequency at pin 16 should be 296* or 346** times the frequency at pin 21.
6. With no vertical sync and pin 24 connected through 10 KΩ to +5 V, measure the period of the waveform at 21. The frequency at pin 16 should be 232* or 232.5** times that at pin 21.
7. Measure pulse width of waveform in pin 21 at +7-V trip points.
8. Measure pulse width at pin 23 at 4-V trip point.

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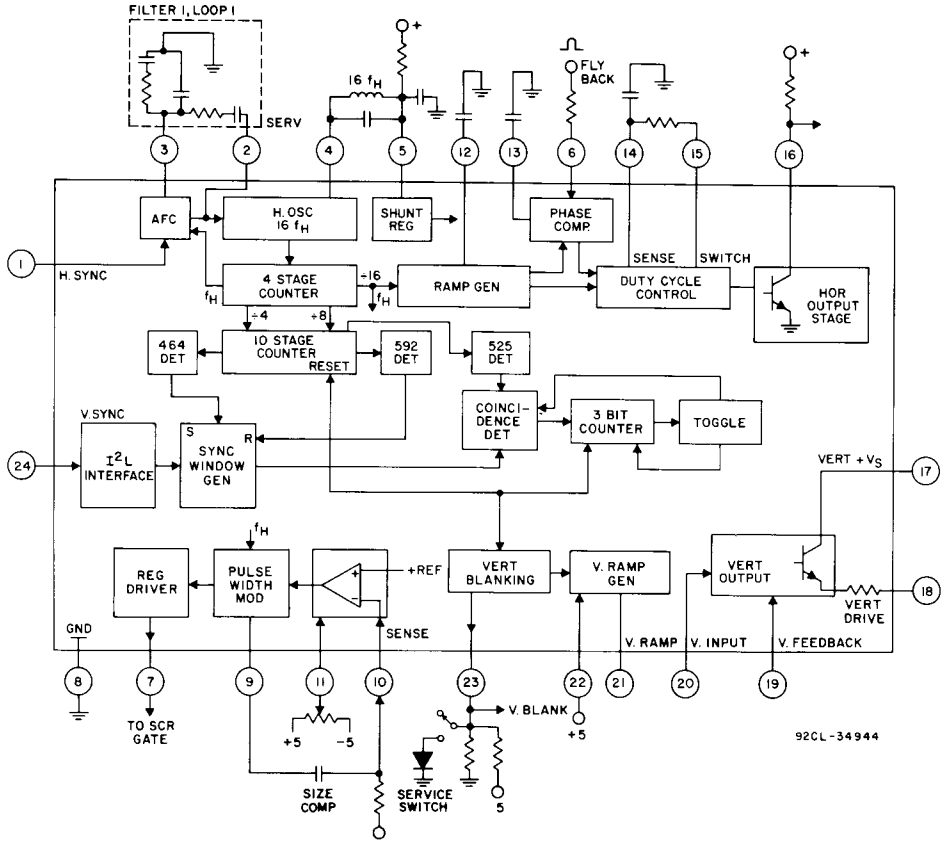

Fig. 1 - Functional block diagram of the CA3210E (525 line).

NOTES: (Cont'd)

9. Measure voltage at pin 21 when pin 23 is at low state. Clock may be stopped during measurement or measurement may be made on the "fly".
10. Set test point 20 to 0.7 V. Measure voltage at pin 21.
11. (a) Adjust test point 16 until pin 18 is 0.3 V. Measure voltage at pin 19.
    (b) Adjust so that the voltage on pin 18 is 4.5 and 8.0 V, respectively.
12. Measure width of negative-going pulse at pin 16 at the 2-V level.
13. When pin 16 goes low, disable clock by applying 18 V. The purpose of this test is to verify that pin 16 will then go from low to high with the clock (pin 14) disabled.
14. Measure amplitude of pulse at pin 16 at its low state.
15. Measure delay of horizontal sync pulse (positive leading edge) with respect to the positive leading edge of pin 16.

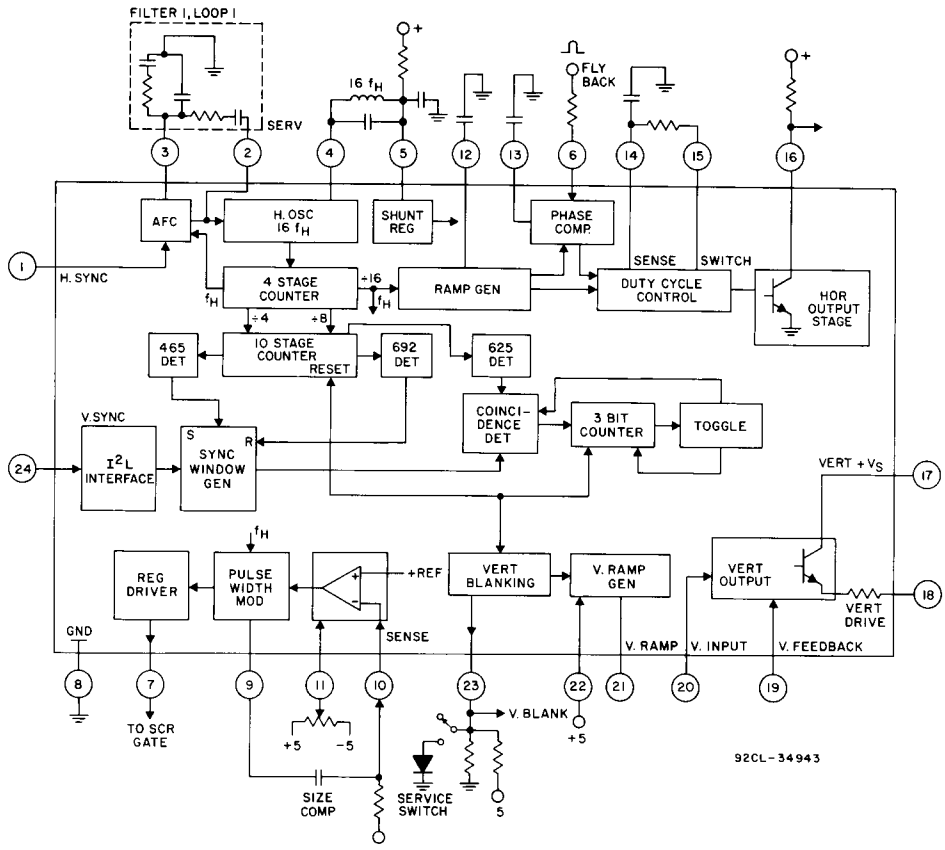

Fig. 2 - Functional block diagram of the CA3223E (625 line).

Horizontal/Vertical Processor

Circuit Operation

Figs. 1 and 2 of the block diagrams show the major functional elements of the RCA-CA3210E and CA3223E.

The master oscillator operates at 16 times the horizontal rate, f_H, as determined by an external LC tank connected between pins 4 and 5. The master oscillator is divided by 4, 8, and 16. The divide by 16 output is used to compare its phase with the incoming horizontal synchronization signal in the first APC loop which acts to synchronize the system. This output is also used to generate a horizontal ramp whose output is used to control the phase of the horizontal output pulse with respect to a flyback pulse input in the second APC loop. The deviation of the horizontal output pulse is adjusted and then connected to the horizontal driver stage. The divide by 4 and 8 outputs are used to drive a 10 section counter for the vertical circuits. The use of the countdown system and associated logic circuits assures good noise immunity and the absence of a vertical hold control in the TV receiver.

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As shown in Figs. 1 or 2 the 464th (CA3210E) or 465th (CA3223E) clock pulse is used to set a SYNC WINDOW generator. If the incoming SYNC signal occurs at the same time the 525th (CA3210E) or 625th (CA3223E) clock pulse occurs, the YES output of a coincidence gate is used to reset a 3-bit counter and to generate the start of vertical blanking and vertical sweep. If the incoming SYNC pulse is removed (by noise, for example), the 10-stage counter will continue to provide an output pulse at the 525th (CA3210E) or 625th (CA3223E) clock but the 3-bit counter will count the number of fields where no coincidence occurred. If incoming SYNC is regained before the 3-bit counter accumulates 8 fields, the 3-bit counter will reset and normal action will continue. If no coincidence is detected in 8 sequential fields, the 3-bit counter energizes the toggle which shifts the mode of operation from countdown to synchronization.

In the sync mode, vertical scan is initiated by the sync pulse. If no sync pulse is present, the system will free run at a frequency determined by the 592 (CA3210E) or 692 (CA3223E) count. A non-standard sync signal circuit operates if the incoming sync occurs regularly between 464 (CA3210E) or 465 (CA3223E) and 592 (CA3210E) or 692 (CA3223E) counts.

The divide by 16 output is also used in the pulse width modulator which generates a triggered constant pulse width signal which in turn drives the deflection circuit.

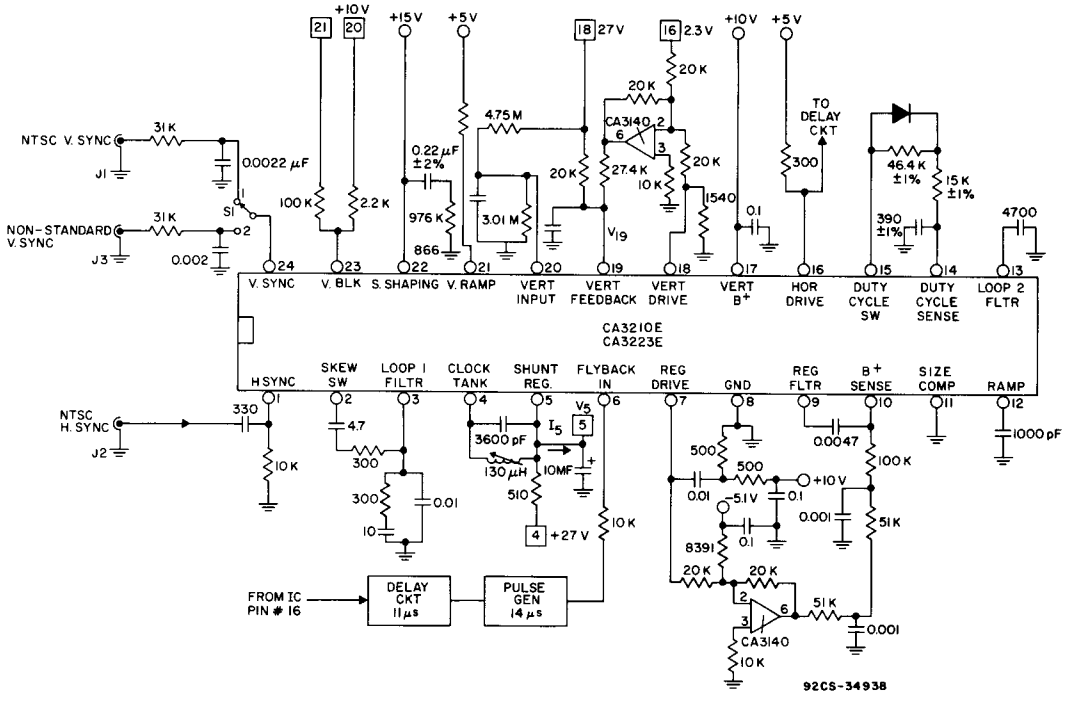

Fig. 3 - Testing circuit.

Circuit Description

Start-up Circuit

The start-up circuit provides power to the integrated circuit at turn-on until horizontally derived B+ is sufficient to power the chip. The start-up circuit protects the horizontal system of the TV receiver by insuring the IC is in the correct mode by delaying operation until the chip supply voltage has reached 8.0 V. After the circuit starts, should the chip supply decrease to 4.0 V, the start-up circuit will turn the IC off.

Skew Switch

A frequency selector circuit is used to route two frequency signals to the AFC (see Figs. 1 and 2). Vertical signals control both the selector circuit and the external Filter 1 time constants. During most of the vertical scan time, signal f_H is routed to AFC and the Filter 1 time constant is selected for a slow loop 1 response time. For the remaining part of the vertical scan, signal $2f_H$ is fed to the AFC and the Filter 1 time constant is selected to give the loop a fast response time. This dual time constant feature allows the system to phase synchronize rapidly with non-standard signals generated by equipment such as a VCR.

Internal Shunt Regulator

The shunt regulator maintains the IC's main supply rail at constant voltage. As the voltage V+ (Fig. 4) increases from zero, the zener voltage eventually becomes conductive, and current flows through R50, R51, and R52. As the voltage across R51 increases, transistor Q119 becomes conductive, maintaining a fixed voltage between the collector and emitter of Q119. Increasing voltage V+ still further increases the voltage across resistor R52, eventually turning on Q120. At this point, voltage V+ becomes regulated due to the varying conduction of shunt transistor Q120.

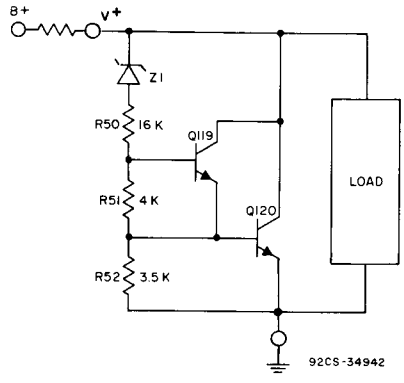

Fig. 4 - Shunt regulator.

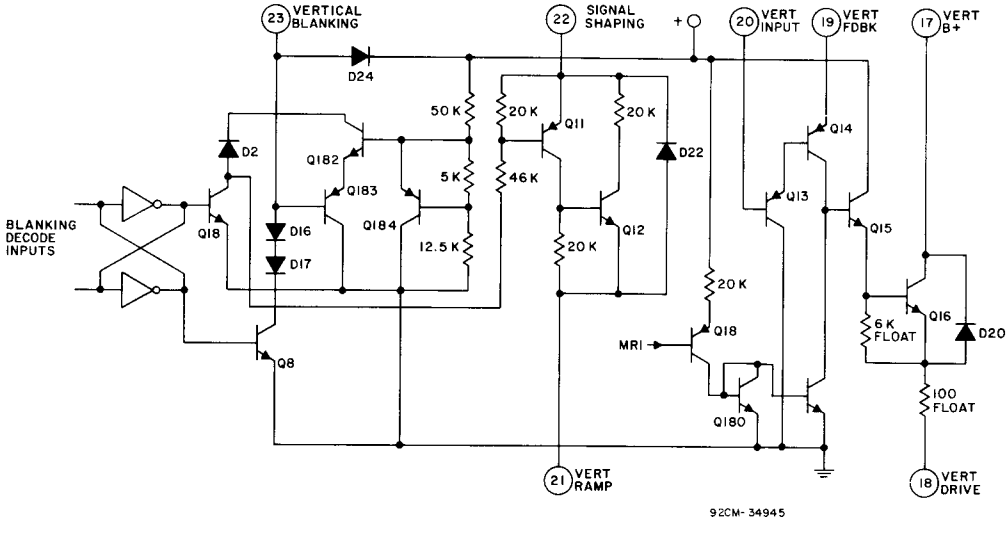

Fig. 5 - Vertical system signals.

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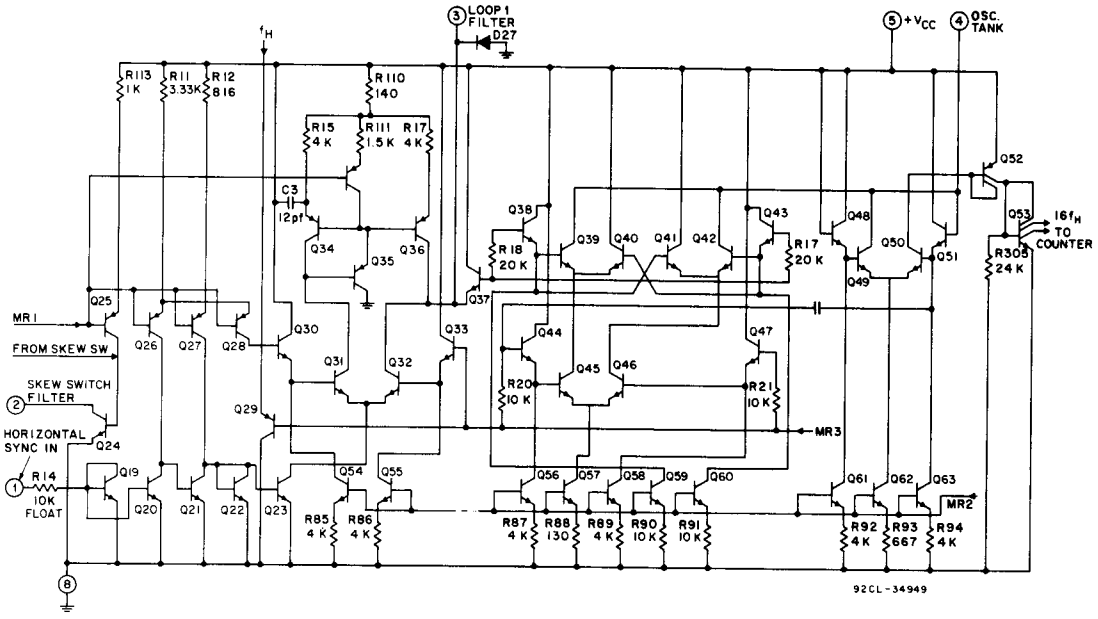

Fig. 6 - 1st loop phase detector of master oscillator.

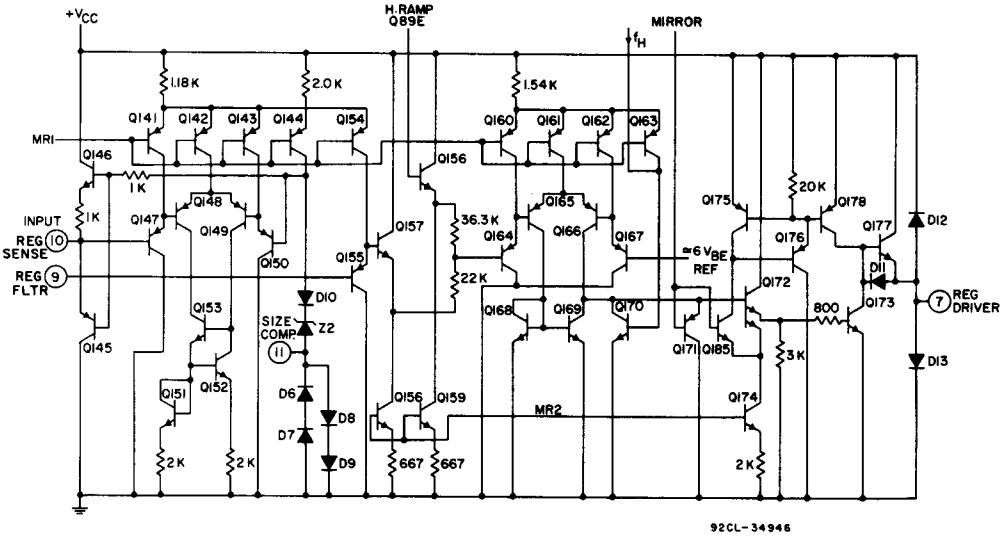

Fig. 7 - Regulator driver and pulse width modulator.

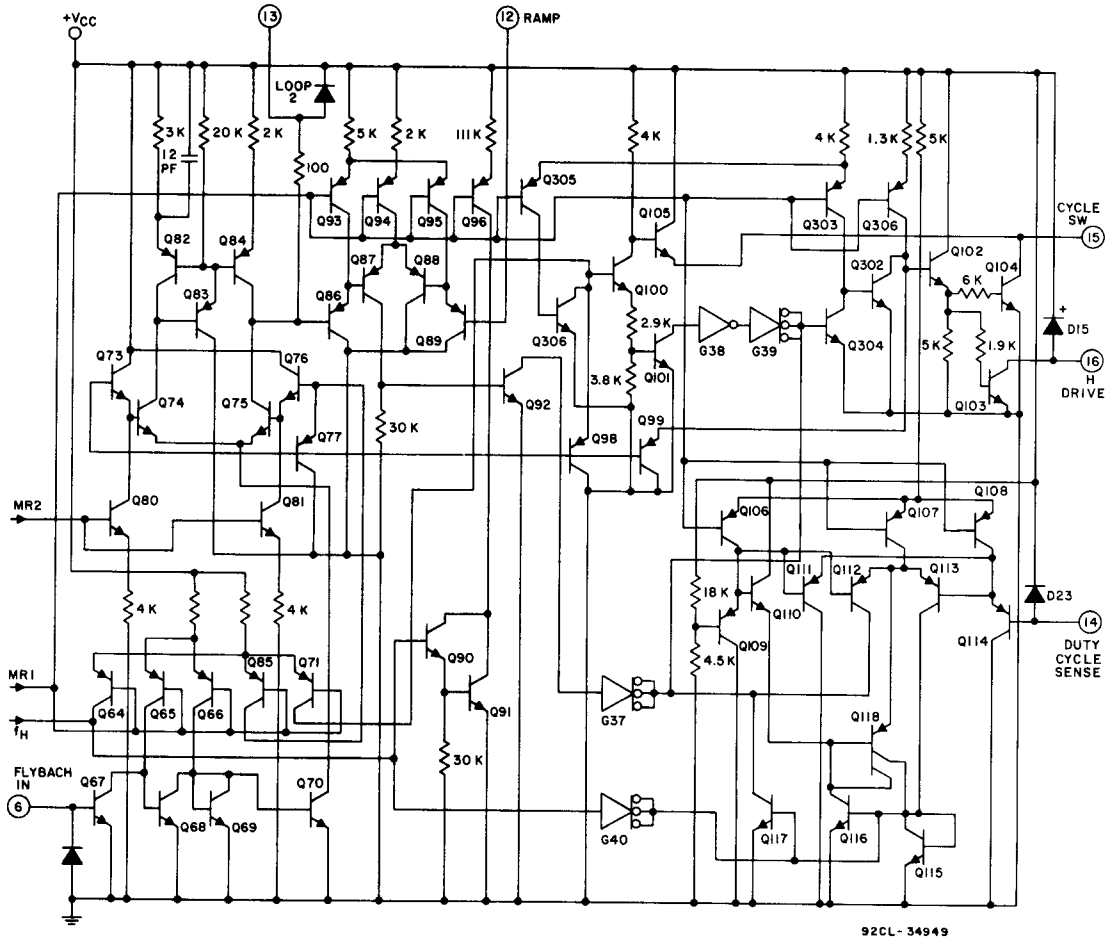

Fig. 8 - Horizontal ramp, control, and drive.

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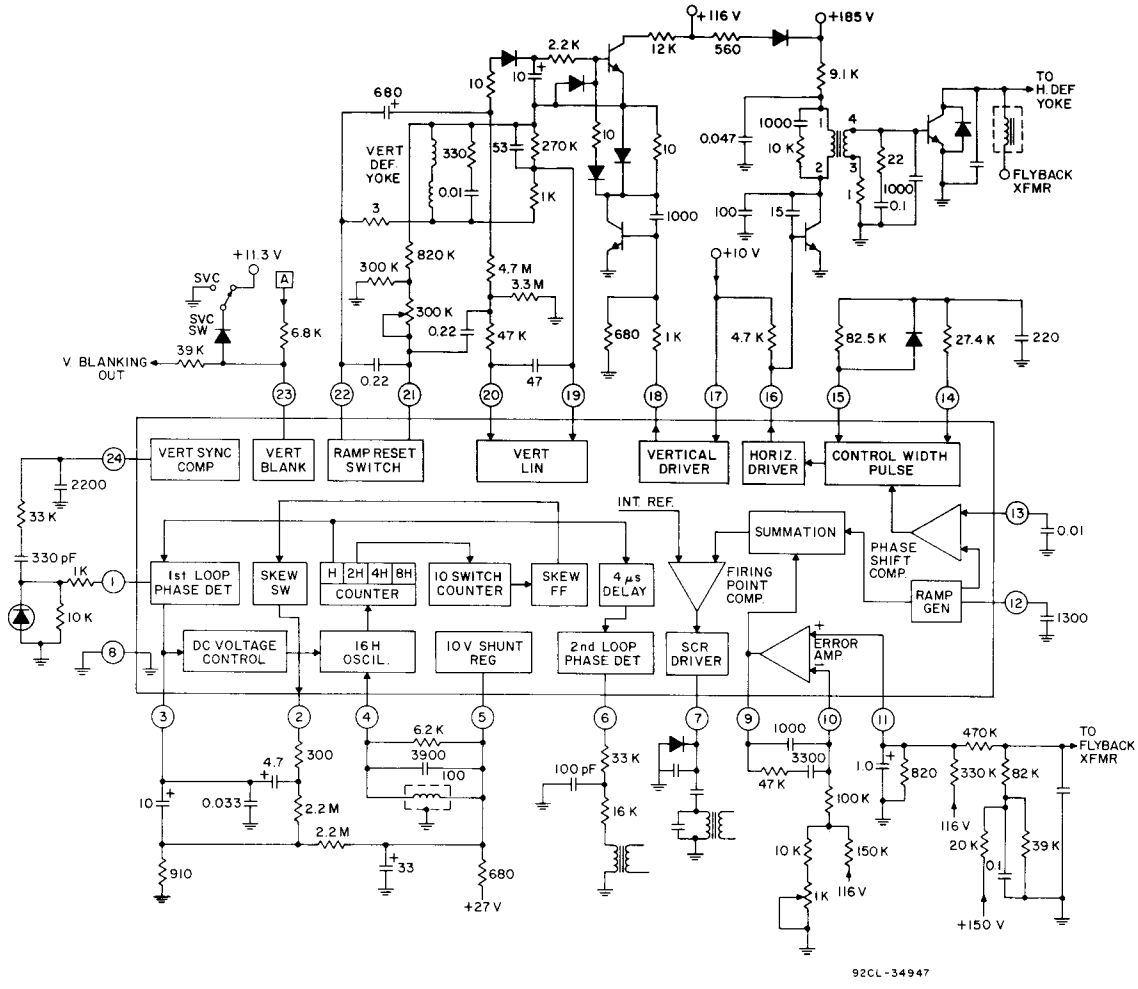

Fig. 9 – Application circuit.

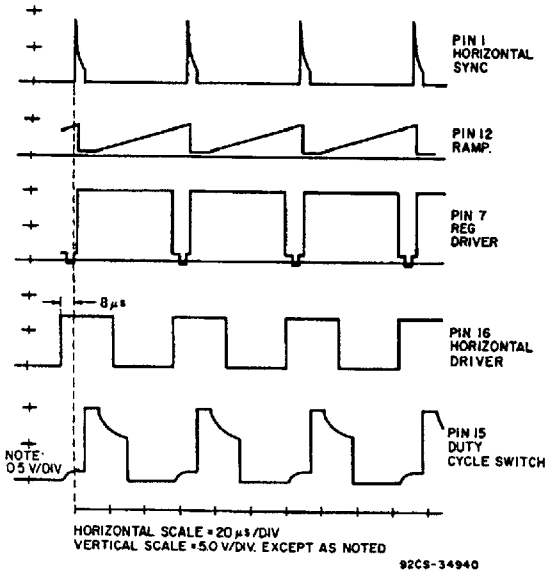

Fig. 10 – Timing relationship between various waveforms for typical circuit application.

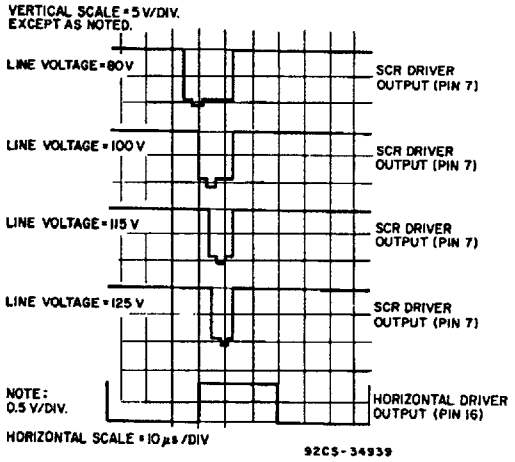

Fig. 11 – Relationship between SCR driver output and horizontal driver output vs. line voltage.

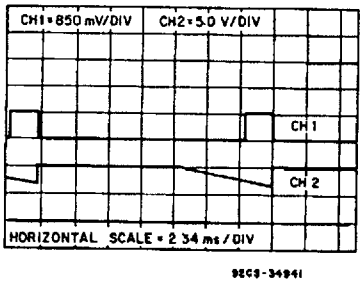

Fig. 12 – Relationship between the vertical sync pulse and the vertical ramp.