

Features

- ESD/EFT/Surge protection for one line with bi-direction
- Provide transient protection for one line to IEC 61000-4-2 (ESD) ±16kV(air) / ±13kV(contact) IEC 61000-4-4 (EFT) 50A (5/50ns) IEC 61000-4-5 (Lightning) 10A (8/20µs)
- Suitable for, **5V and below**, operating voltage applications
- 01005 small CSP package saves board space
- Protect one I/O line or one power line
- Fast turn-on and low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- Green part

Applications

- Mobile phones
- Handheld portable applications
- Computer interfaces protection
- Microprocessors protection
- Serial and parallel port protection
- Control signal lines protection
- Power lines on PCB protection
- Latchup protection

Description

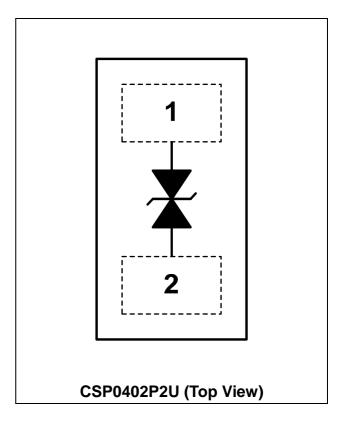
AZ5C25-01B is a design which includes one bi-directional ESD rated clamping cell to protect one power line, or one control line, or one low-speed data line in an electronic system. The AZ5C25-01B has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

AZ5C25-01B is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ5C25-01B is bi-direction and may be used on lines where the signal swings above and below ground.

AZ5C25-01B may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration



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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)					
PARAMETER	SYMBOL	RATING	UNIT		
Peak Pulse Current (tp =8/20µs)	I _{PP}	10	А		
Operating Voltage	V _{DC}	±5.5	V		
ESD per IEC 61000-4-2 (Air)	V _{ESD-1}	±16	kV		
ESD per IEC 61000-4-2 (Contact)	V_{ESD-2}	±13	κv		
Lead Soldering Temperature	T _{SOL}	260 (10 sec.)	°C		
Operating Temperature	T _{OP}	-55 to +125	°C		
Storage Temperature	T _{STO}	-55 to +150	°C		

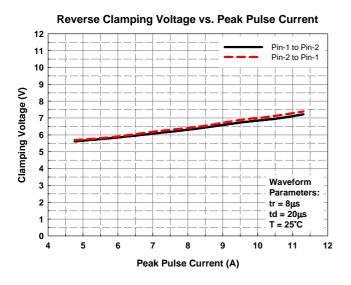
ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	BOL CONDITION		ΤΥΡ	MAX	UNIT
Reverse Stand-Off Voltage	V_{RWM}	T = 25°C.	-5		5	V
Reverse Leakage Current	I _{Leak}	$V_{RWM} = \pm 5.0V, T = 25^{\circ}C.$			100	nA
Reverse Breakdown Voltage	V_{BV}	$I_{BV} = 1mA, T = 25^{\circ}C.$	6		9	V
Surge Clamping Voltage	V _{CL-surge}	I _{PP} = 5A, tp = 8/20μs, T = 25°C.		5.6		V
ESD Clamping Voltage (Note 1)	V_{CL-ESD}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), contact mode, T = 25°C.		6.0		V
ESD Dynamic Turn-on Resistance	R _{dynamic}	IEC 61000-4-2 0~+8kV, contact mode, T = 25°C.		0.03		Ω
Channel Input Capacitance	C _{IN}	$V_{IN} = 0V$, f = 1MHz, T = 25°C.		14	18	pF

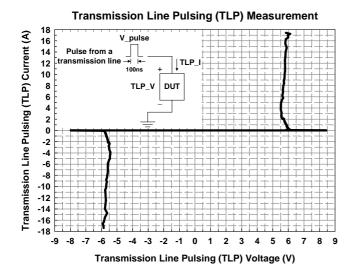
Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

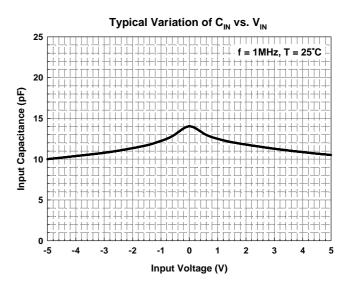
TLP conditions: Z_0 = 50 Ω , t_p = 100ns, t_r = 1ns.



Typical Characteristics







Revision 2019/09/25 © 2019-2020 Amazing Micro.



Application Information

The AZ5C25-01B is designed to protect one line against system ESD/EFT/Lightning pulses by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ5C25-01B is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ5C25-01B should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ5C25-01B.
- Place the AZ5C25-01B near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

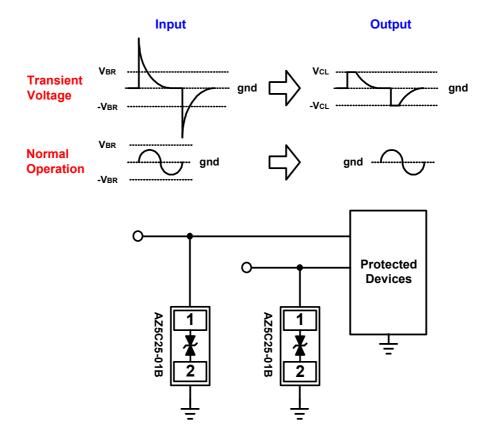
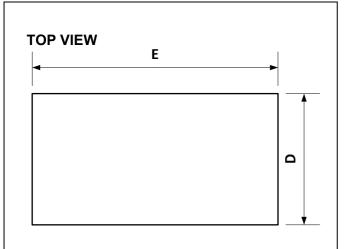


Fig. 1 ESD protection scheme by using AZ5C25-01B.



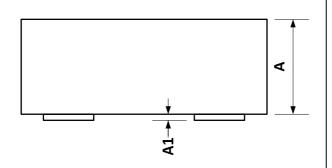
Mechanical Details CSP0402P2U PACKAGE DIAGRAMS



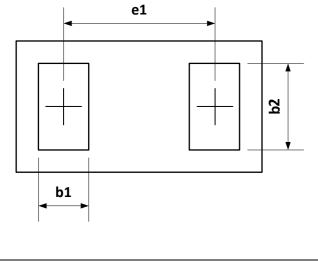
SYMBOL	MILLIMETERS				
STIVIBUL	MIN.	NOM.	MAX.		
E	0.415	0.440	0.465		
D	0.210	0.235	0.260		
Α	0.145	0.170	0.195		
A1	0.008	0.011	0.014		
b1	0.084	0.090	0.096		
b2	0.149	0.155	0.161		
e1		0.270BSC			

PACKAGE DIMENSIONS

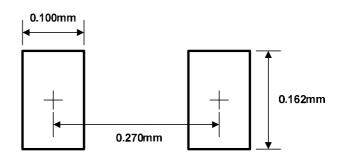
SIDE VIEW



BOTTOM VIEW



LAND LAYOUT

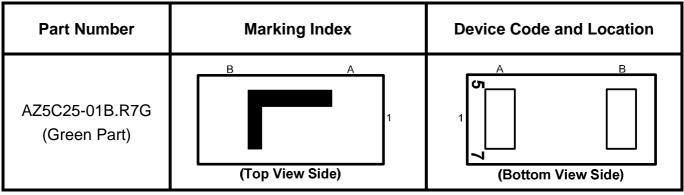


Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.



MARKING CODE



Notes

- 1. Green means Pb-free, RoHS, and Halogen free compliant.
- 2. The marking index is on the top view side of the device. The device code is on the pad side (bottom view side).

Ordering Information

PN#	Material	Туре	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ5C25-01B.R7G	Green	T/R	7 inch	15,000/reel	4 reels = 60,000/box	6 boxes = 360,000/carton

Revision History

Revision	Modification Description				Modification Description		
Revision 2019/09/25	Formal Release.						