Integrated Device Technology, Inc.

256K x 32 BiCMOS/CMOS STATIC RAM MODULE

IDT7MP4045

T-46-23-14

FEATURES:

- High density 8 megabit static RAM module
- Low profile 64 pin ZIP (Zig-zag In-line vertical Package) or 64 pin SIMM (Single In-line Memory Module)
- Ultra fast access time: 10ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

PIN CONFIGURATION[1]

		1	GND	
PD_0	2	3	PD_1	PD_0 – GND
I/O_0	4	5	I/O_8	PD_1 – GND
I/O_1	6	7	I/O_9	
I/O_2	8	9	I/O_{10}	
I/O_3	10	11	I/O_{11}	
V_{CC}	12	13	A_0	
A_7	14	15	A_1	
A_8	16	17	A_2	
A_9	18	19	I/O_{12}	
I/O_4	20	21	I/O_{13}	
I/O_5	22	23	I/O_{14}	
I/O_6	24	25	I/O_{15}	
I/O_7	26	27	GND	
$\overline{WE}$	28	29	A_{15}	
A_{14}	30	31	$\overline{CS_2}$	
$\overline{CS_1}$	32	ZIP, SIMM TOP VIEW		
		33	$\overline{CS_4}$	
$\overline{CS_3}$	34	35	A_{17}	
A_{16}	36	37	$\overline{OE}$	
GND	38	39	I/O_{24}	
I/O_{16}	40	41	I/O_{25}	
I/O_{17}	42	43	I/O_{26}	
I/O_{18}	44	45	I/O_{27}	
I/O_{19}	46	47	A_3	
A_{10}	48	49	A_4	
A_{11}	50	51	A_5	
A_{12}	52	53	V_{CC}	
A_{13}	54	55	A_6	
I/O_{20}	56	57	I/O_{28}	
I/O_{21}	58	59	I/O_{29}	
I/O_{22}	60	61	I/O_{30}	
I/O_{23}	62	63	I/O_{31}	
GND	64			

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NOTE:

1. Pins 2 and 3 (PD_0 and PD_1) are read by the user to determine the density of the module. If PD_0 reads GND and PD_1 reads GND, then the module had a 256K depth.

DESCRIPTION:

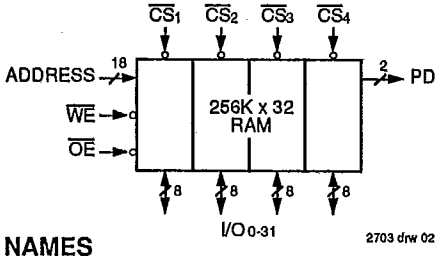
The IDT7MP4045 is a 256K x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 256K x 4 static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. Extremely fast speeds can be achieved due to the use of 1 megabit static RAMs fabricated in IDT's high performance, high reliability BiCEMOS™ technology. The IDT7MP4045 is available with access time as fast as 10ns with minimal power consumption.

The IDT7MP4045 is packaged in a 64 pin FR-4 ZIP (Zig-zag In-line vertical Package)or a 64 pin SIMM (Single In-line Memory Module). The ZIP configuration allows 64 pins to be placed on a package 3.65 inches long and 0.35 inches wide. At only 0.60 inches high, this low profile package is ideal for systems with minimum board spacing while the SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the IDT7MP4045 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Two identification pins (PD0 and PD1) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD0 and PD1 to determine a 256K depth.

FUNCTIONAL BLOCK DIAGRAM



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PIN NAMES

I/O_{0-31}	Data Inputs/Outputs
A_{0-17}	Addresses
$\overline{CS}_{1-4}$	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
PD_{0-1}	Depth Identification
V_{CC}	Power
GND	Ground
NC	No Connect

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COMMERCIAL TEMPERATURE RANGE

APRIL 1992

DSC-7061/3

T-46-23-14

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	$V_{(IN)}$ = 0V	12	pF
$C_{IN(A)}$	Input Capacitance (Address & Control)	$V_{(IN)}$ = 0V	70	pF
C_{OUT}	Output Capacitance	$V_{(OUT)}$ = 0V	12	pF

NOTE: 2703 tbl 02
1. This parameter is guaranteed by design but not tested.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	$DATA_{IN}$	Active
Read	L	H	H	High-Z	Active

2703 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2703 tbl 03
1. V_{IL} (min) = –1.5V for pulse width less than 10ns.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2703 tbl 06
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2703 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	80	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

2703 tbl 07

Symbol	Parameter	Test Conditions	10ns - 17ns[1] Max.	20ns - 45ns Max.	Unit
I_{CC}	Dynamic Operating Current	f = f_{MAX}; $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	1600	1200	mA
I_{SB}	Standby Supply Current	$\overline{CS} \geq V_{IH}$, V_{CC} = Max. Outputs Open, f = f_{MAX}	480	480	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \geq V_{CC}$ – 0.2V; f = 0 $V_{IN} > V_{CC}$ – 0.2V or < 0.2V	320	80	mA

NOTE: 2703 tbl 08
1. Preliminary specifications only.

AC TEST CONDITIONS

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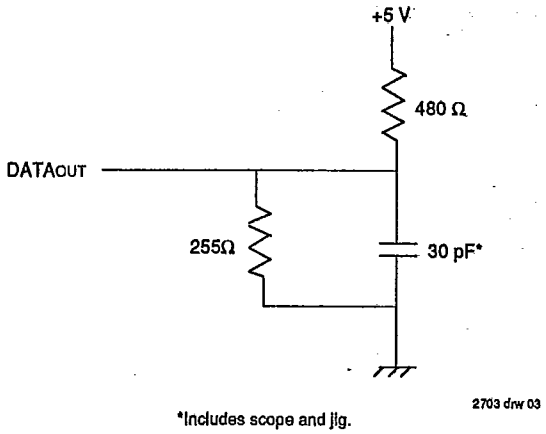
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

2703 tbl 09



*Includes scope and jig.

Figure 1. Output Load

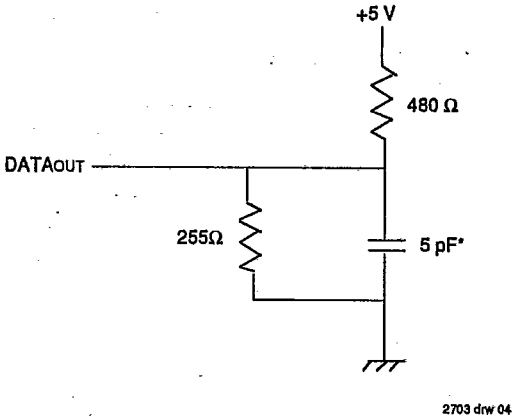


Figure 2. Output Load
(for t_{OLZ},t_{OHZ}, t_{CHZ}, t_{CLZ}, t_{WHZ}, t_{OW})

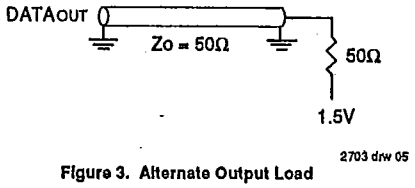


Figure 3. Alternate Output Load

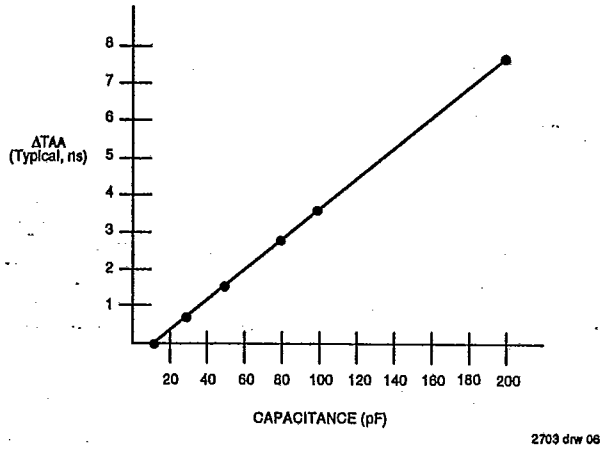


Figure 4. Alternate Lumped Capacitive Load, Typical Derating

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP4045SxxZ, 7MP4045SxxM								Unit
		-10[2]		-12[2]		-15[2]		-17[2]		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	10	—	12	—	15	—	17	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	17	ns
t_{ACS}	Chip Select Access Time	—	7	—	8	—	10	—	12	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	2	—	2	—	2	—	2	—	ns
t_{OE}	Output Enable to Output Valid	—	5	—	5	—	6	—	8	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	2	—	2	—	2	—	2	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	6	—	7	—	8	—	10	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	3	—	4	—	5	—	6	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	10	—	12	—	15	—	17	—	ns
t_{CW}	Chip Select to End of Write	8	—	8	—	9	—	10	—	ns
t_{AW}	Address Valid to End of Write	8	—	9	—	10	—	12	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	9	—	10	—	12	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	5	—	5	—	6	—	7	ns
t_{DW}	Data to Write Time Overlap	5	—	5	—	6	—	8	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	2	—	2	—	2	—	2	—	ns

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NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

AC ELECTRICAL CHARACTERISTICS

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(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP4045SxxZ, 7MP4045SxxM										Unit
		-20		-25		-30		-35		-45		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	30	—	35	—	45	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	10	—	12	—	15	—	18	—	23	ns
t_{CLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	10	—	12	—	15	—	18	—	20	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	10	—	10	—	10	—	10	—	10	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	20	—	25	—	30	—	35	—	45	ns
Write Cycle												
t_{WC}	Write Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
t_{CW}	Chip Select to End of Write	15	—	20	—	25	—	30	—	40	—	ns
t_{AW}	Address Valid to End of Write	15	—	20	—	25	—	30	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	13	—	15	—	18	—	20	—	23	ns
t_{DW}	Data to Write Time Overlap	12	—	15	—	17	—	20	—	25	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.

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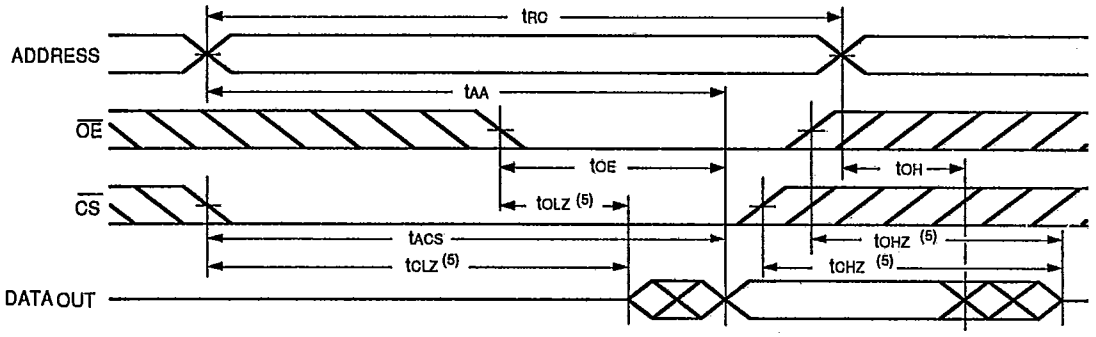
TIMING WAVEFORM OF READ CYCLE NO. 1(1)

T-46-23-14



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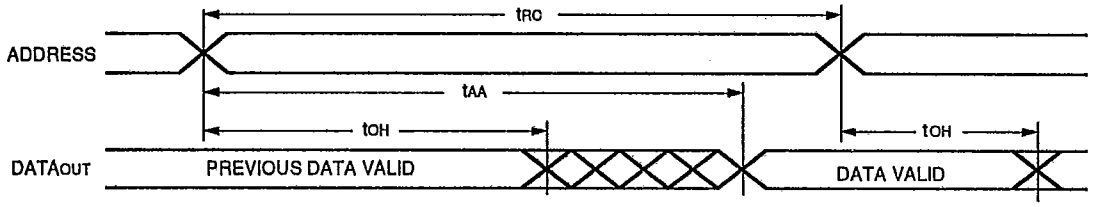
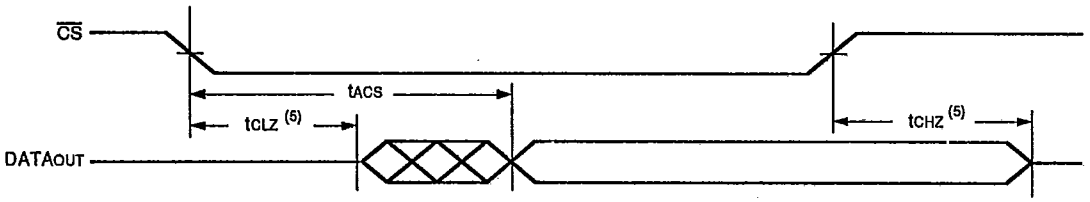
TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



2703 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)

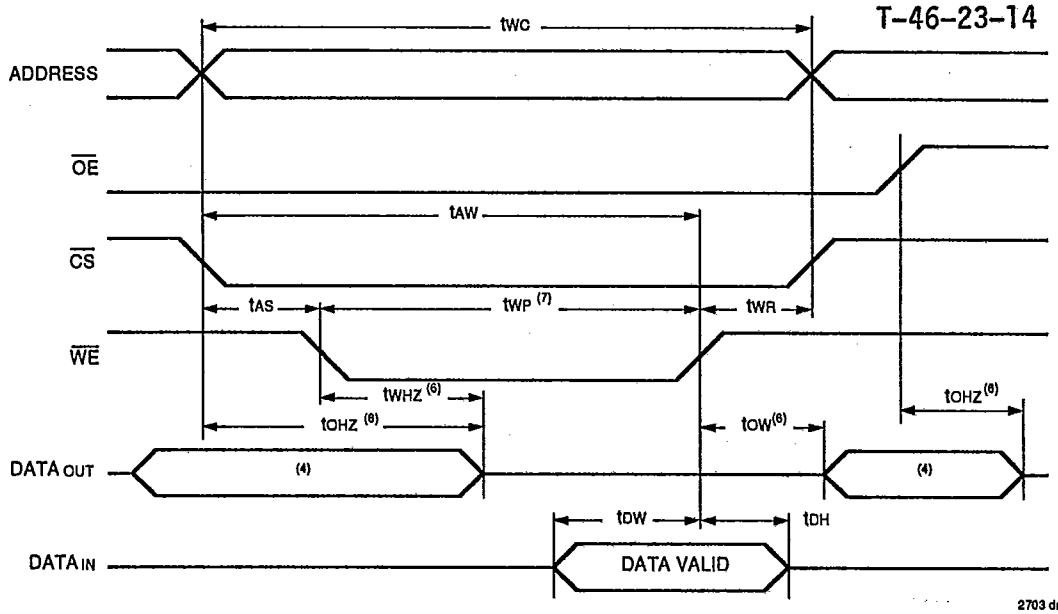


2703 drw 06

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

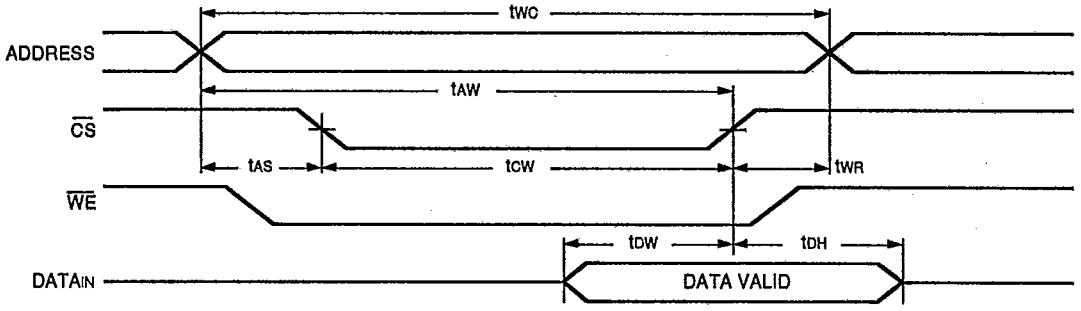
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (1, 2, 3, 7)

T-46-23-14



2703 drw 10

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) (1, 2, 3, 5)



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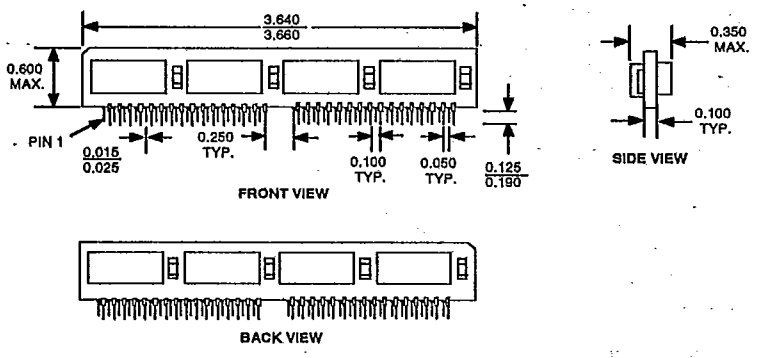
NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

PACKAGE DIMENSIONS

T-46-23-14

ZIP VERSION



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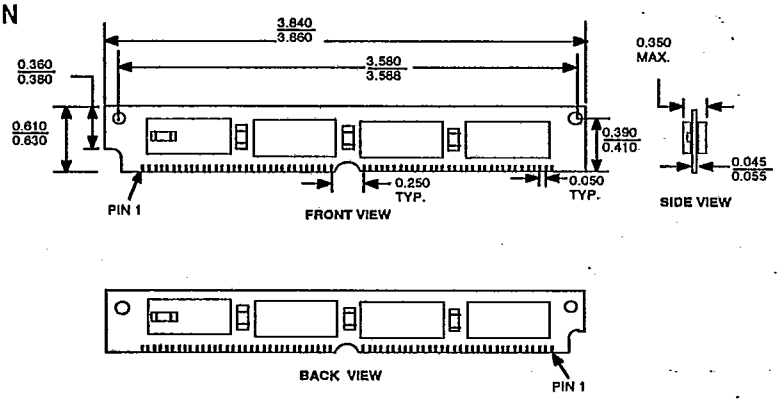
SIMM VERSION



2703 drw 13