5-V to 60-V WIDE-INPUT SYNCHRONOUS PWM BUCK CONTROLLER

Check for Samples: TPS40490

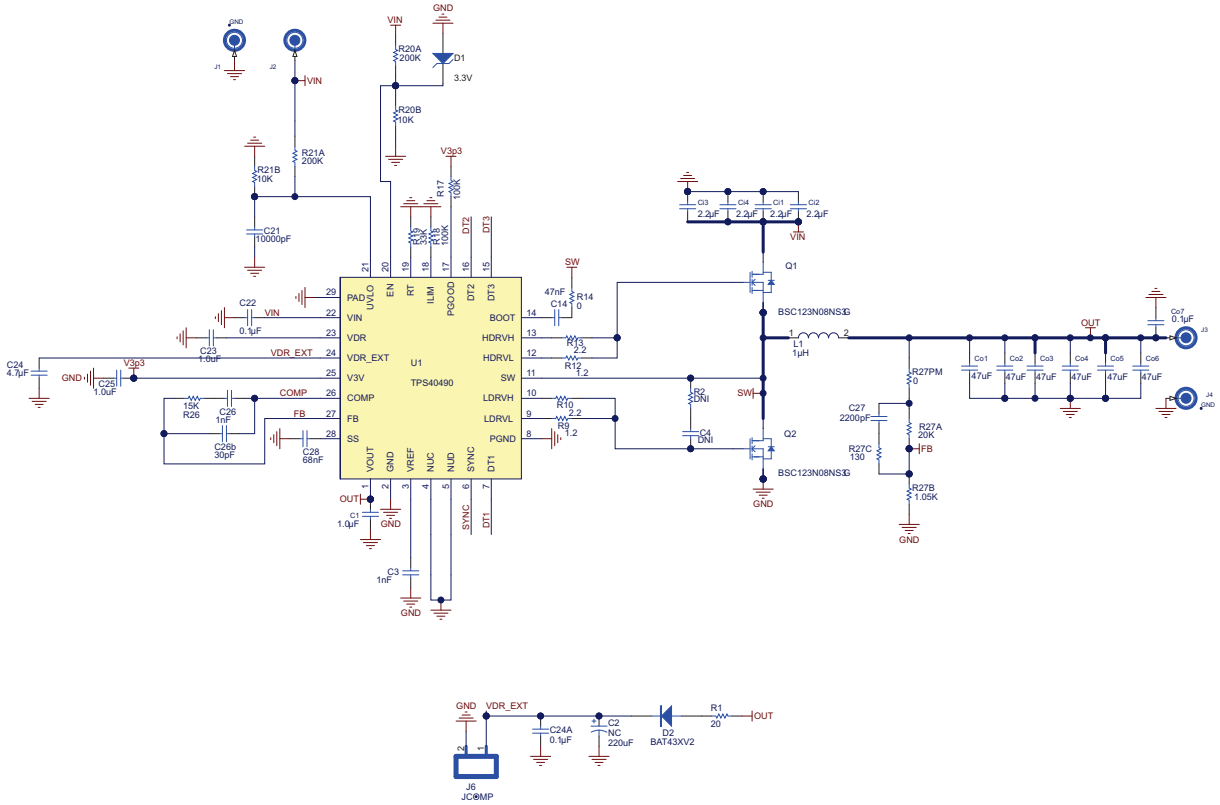
FEATURES

- Wide-Input Voltage Range from 5 V to 60 V
- 600-mV Reference Voltage With ±1% Accuracy and External Modulation Capabilities
- Programmable UVLO and Hysteresis
- Voltage Mode Control With Feed Forward and High Gain Bandwidth Error Amplifier
- 100-kHz to 5.4-MHz Programmable Frequency
- Smart Low and High Side Driver
  - Factory Selectable Gate Drive Voltage VDR With External Drive Capability and UVLO Protection
  - Matched Low and High Side Propagation Delay
  - Programmable Fixed Delay Dead-time
- Low-Side FET Sensing Overcurrent Protection and High-Side FET Sensing Short-Circuit Protection
- Programmable Closed Loop Soft-Start
- Supports Pre-Biased Outputs
- Thermal Shutdown at 160°C With Hysteresis
- Power Good Detector
- Integrated Diode for Bootstrap Supply With UVLO
- 28-Pin 5-mm × 5-mm QFN (RHD) Package

APPLICATIONS

- POL Modules
- Wide Input Voltage, High-Power Density DC/DC Converters for Industrial, Networking and Telecomm Equipment
- Notebook and Tablet Computers
- Envelope Tracking Systems

TYPICAL APPLICATION (Non-Isolated 24V-12V Supply)



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DESCRIPTION

TPS40490 is a full-featured, synchronous PWM buck controller that operates with an input voltage from 5 V to 60 V and is optimized for high-power-density, high-reliability DC/DC converter applications using the latest generation of MOSFET transistors.

TPS40490 can operate in multiple DC systems from 5 V to 60 V and provides accurate output voltage regulation with ±1% ensured accuracy. The reference voltage can be modulated in applications that require a tracking envelope supply.

The controller can be configured for voltage-mode control with input-voltage feed-forward compensation that enables instant response to input voltage change. The switching frequency is programmable from 100 kHz to 5.4 MHz.

The controller has an enable pin that allows for system shutdown in a low-current mode and a delayed start-up for sequencing purposes, and a soft-start pin that allows adjustable soft-start time by connecting a capacitor to the pin.

TPS40490 has a complete set of system protection and monitoring features such as programmable UVLO, programmable overcurrent protection (OCP) by sensing the low-side FET, selectable short-circuit protection (SCP) by sensing the high-side FET and thermal shutdown. The current limit trip point is set with a resistor fitted to the ILIM pin that enables the designer to adjust current limit by selecting an external resistor and optimize the choice of inductor. Once an over-current lasting more than 4 cycles is sensed, the converter will shut down for 100 ms and then the start-up sequencing will begin again. If the overload has been removed, the converter will ramp up and operate normally. If this is not the case, the converter will sense another over-current event and shut down again, repeating the cycle (hiccup) until the failure is cleared.

The controller supports pre-biased output and provides an open-drain PGOOD signal. The PGOOD pin is pulled low when the buck converter is pulled below 80% of the nominal output voltage. The PGOOD is pulled up through an external resistor when all converter outputs are more than 90% of its nominal output voltage. The default reset time is 100 ms. The polarity of the PGOOD is active high.

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the device to stop operating when the junction temperature exceeds thermal trip threshold. Once the die temperature decreases below 140°C, the device reinitiates the power up sequence. Thermal shutdown hysteresis is 20°C.

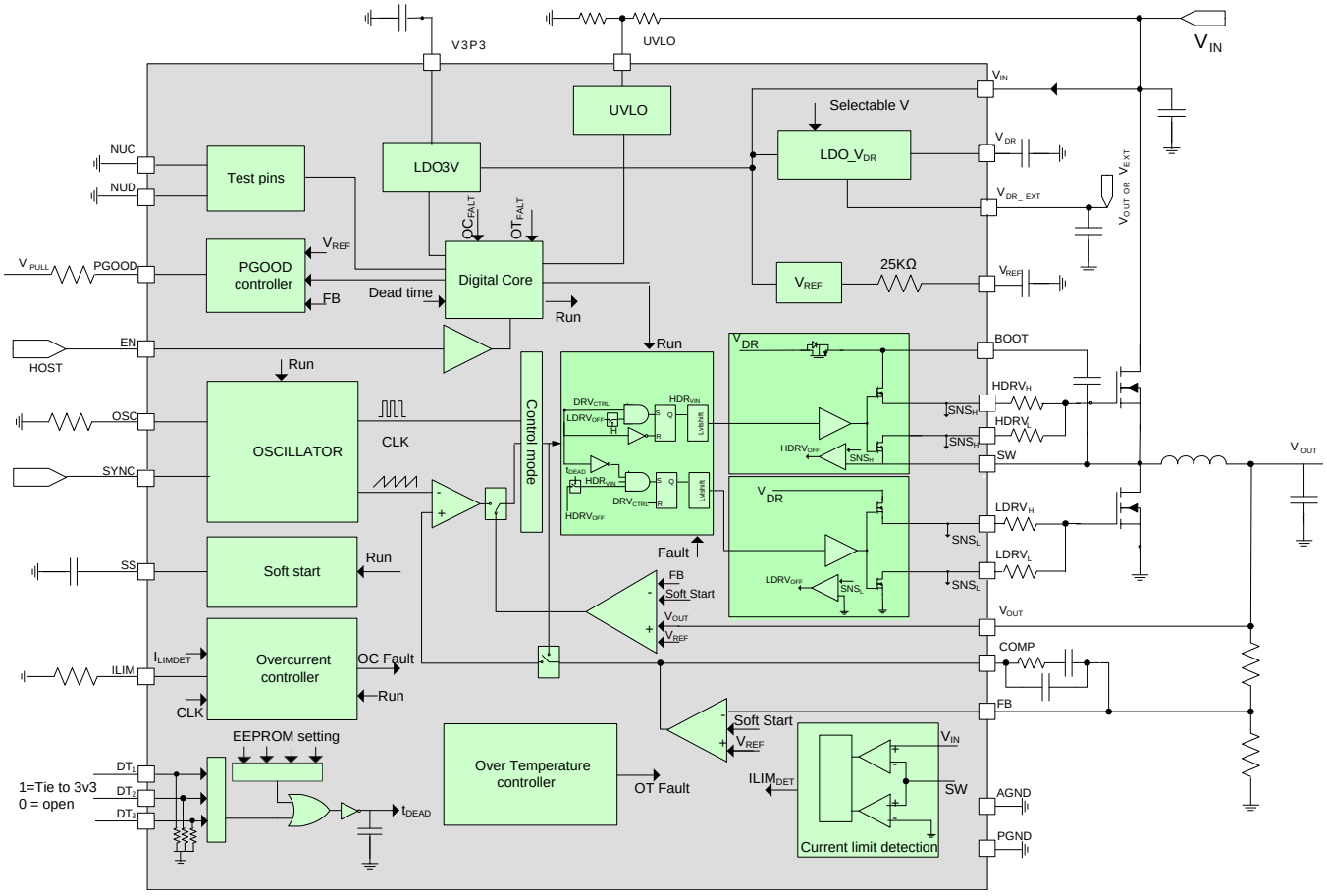
ORDERING INFORMATION(1)

T_A	DEVICE	V_{IN} RANGE (V)	V_{DR} (V)	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	TPS40490 MOSFET Low V_{IN}	5 to 30	4.8	RHD-28	TPS40490MLRHDR/T	TPS40490ML
	TPS40490 MOSFET High V_{IN}	5 to 60	6.8		TPS40490MHRHDR/T	TPS40490MH

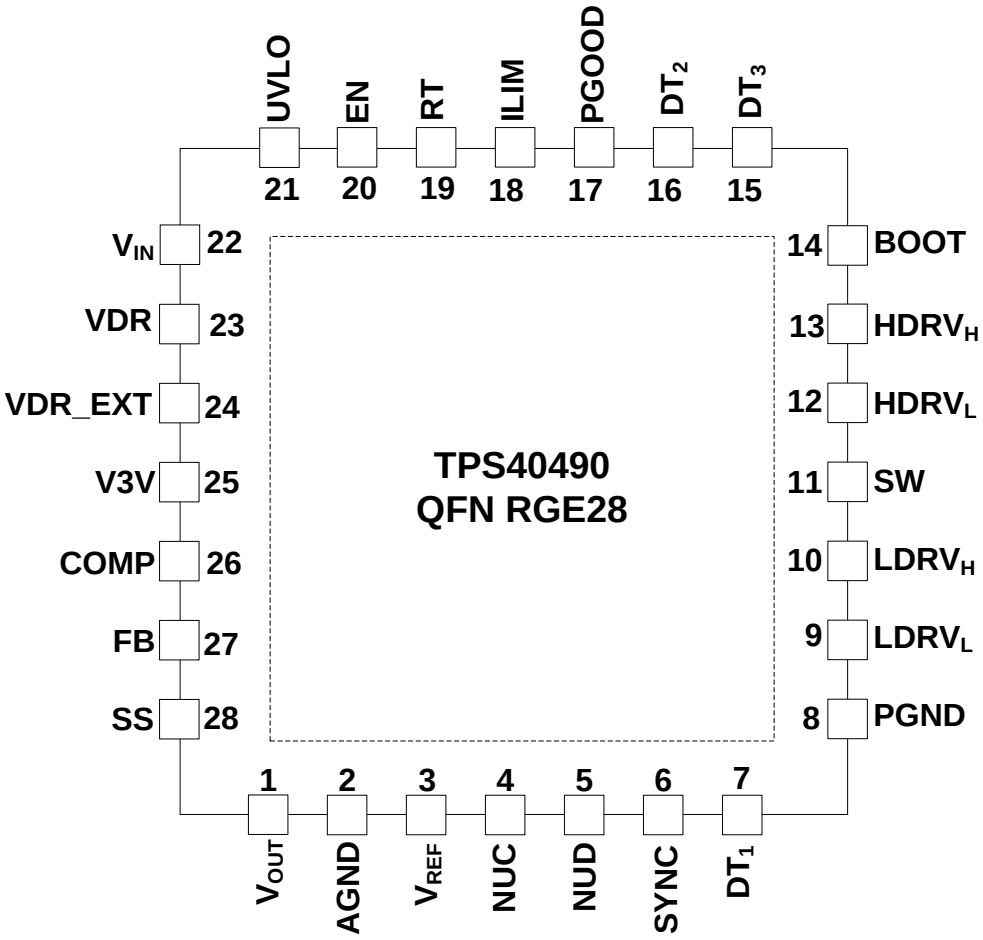
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

BLOCK DIAGRAM



PIN-OUT and TERMINAL FUNCTIONS



PIN FUNCTIONS

NAME	I/O	PIN	DESCRIPTION
VOUT	I	1	Output voltage for the controller
AGND	GND	2	Analog signal ground. This pin must be electrically connected to power ground PGND externally.
VREF	O	3	Reference pin. A ceramic capacitor with a value between 1 nF and 100 nF must be connected between this pin and the AGND pin and placed closely to this pin. This provides an RC filter with 25-kΩ resistor inside the die.
NUC	-	4	Pin not used. Connect to ground during normal operation.
NUD	-	5	Pin not used. Connect to ground during normal operation.
SYNC	I	6	External synchronization pin.
DT_1	I	7	Dead time set bit 1. Connect to 3V3 for 1, leave open for 0.
PGND		8	Power ground. This pin must externally connect to the AGND at a single point.
$LDRV_L$	O	9	Low side gate driver turn-off output. Connect the gate of the low side transistor with a short, low inductance path.
$LDRV_H$	O	10	Low side gate driver turn-on output. Connect the gate of the low side transistor with a short, low inductance path.
SW	O	11	This pin must connect to the switching node of the synchronous buck converter.
$HDRV_L$	O	12	High side gate driver turn-off output. Connect the gate of the high side transistor with a short, low inductance path.
$HDRV_H$	O	13	High side gate driver turn-on output. Connect the gate of the high side transistor with a short, low inductance path.
BOOT	O	14	Boot capacitor node for high-side FET gate driver supply. The boot capacitor is connected from this pin to SW.
DT_3	I	15	Dead time set bit 3. Connect to ground for 0, leave open for 1.
DT_2	I	16	Dead time set bit 2. Connect to ground for 0, leave open for 1.
PGOOD	O	17	Power good indicator. This pin is an open-drain output pin and a 10-kΩ pull-up resistor is recommended to be connected between this pin and V3V.
ILIM	I	18	A resistor from this pin to AGND sets the current limit. This pin provides source current used for over current protection threshold setting.
RT	I	19	A resistor from this pin to AGND sets the oscillator frequency. Even if operating with an external synchronization clock, it is required to have a resistor at this pin to set the free running switching frequency.
EN	I	20	This pin must be high for the device to be enabled. If this pin is pulled low, the device is put in a low-power consumption shutdown mode. Care must be taken to make sure the voltage at this pin does not exceed 3.6 V.
UVLO	I	21	Undervoltage lockout. A resistor divider on this pin from VIN to AGND can be used to set the UVLO threshold.
V_{IN}	I	22	Input voltage for the controller which is also the input voltage for the DC/DC converter. A 1-µF to 10-µF capacitor from this pin to AGND must be added and placed closed to VIN.
V_{DR}	O	23	Regulated output for gate driver. A ceramic capacitor with a value between 1 µF and 10 µF must be connected from this pin to PGND.
V_{DR_EXT}	I	24	Optional External supply to gate driver. A ceramic capacitor with a value between 1 µF and 10 µF must be connected from this pin to PGND. A supply of 5 V to 12 V can be connected to this input providing drive voltage for better efficiency.
V3V	O	25	3.3-V regulated output. A ceramic by-pass capacitor of 1 µF must be connected between this pin and the AGND pin and placed closely to this pin.
COMP	O	26	Output of the internal error amplifier. The feedback loop compensation network is connected from this pin to the FB pin.
FB	I	27	Negative input to the error amplifier. The output voltage is fed back to this pin through a resistor divider network.
SS	I	28	A capacitor must be connected at this pin to AGND. The capacitor value sets the soft-start time.
PAD			Power pad. Must be connected to PCB ground.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range, (unless otherwise noted) (1)(2)

			MIN	MAX	UNIT
Input	V_{IN}, V_{OUT}		–0.3	66	V
	V_{DR_EXT}		-0.3	13.2	V
	RT, SS, FB, V_{REF}, EN, PGOOD, V3V, ILIM, NUC, NUD, UVLO, SYNC, DT_1, DT_2, DT_3		–0.3	3.6	V
	V_{DR}, $LDRV_H$, LDR_{VL}, LDRV, COMP		–0.3	8.8	V
	$HDRV_H$, $HDRV_L$		V_{SW}	BOOT	V
	BOOT-SW, $HDRV_H$/$HDRV_L$-SW, differential from BOOT or $HDRV_H$/$HDRV_L$ to SW		–0.3	V_{DR}	V
Output	SW		–8	VIN	V
	BOOT		–0.3	80V(V_{SW} + V_{DR})	V
Ground	GND-PGND, PGND-GND		–0.3	0.3	V
	Power PAD to AGND (must be electrically connected externally to device)			0	
Electrostatic discharge (ESD)	Human body model (HBM)	All pins excluding LDRVH and LDRVL	2000		V
		LDRVH and LDRVL pins	1500		
	Charge device model (CDM)		500		
Lead Temperature				260	°C
Operating junction temperature range, T_J			–40	150	°C
Storage temperature T_{STG}			–55	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operatIon of the device at these or any other conditions beyond those indicted under recommended operating conditions is not implied. Exposure it absolute maximum rated condtions for extended periods may affect device reliability.
(2) Unless noted, all voltages are with respect to GND.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input operating voltage, TPS40490MHRHDR	6		60	V
	Input operating voltage, TPS40490MLRHDR	5(1)		25	V
T_A	Ambient temperature	–40		125	°C

(1) Operation with 5-V input is possible by connecting V_{IN} pin to V_{DR}. Consult with the factory.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS40490 RHD 28 pins	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(1)	36.6	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance(2)	26.2	
θ_{JB}	Junction-to-board thermal resistance(3)	8.8	
ψ_{JT}	Junction-to-top characterization parameter(4)	0.3	
ψ_{JB}	Junction-to-board characterization parameter(5)	8.7	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance(6)	1.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7.
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 150°C, V_{IN} = 48 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY							
V_{IN}	Input Voltage range			5		60	V
IDD_{SDN}	Shutdown	V_{EN} < 100 mV			2		µA
IDD_Q	Quiescent, drivers not switching	V_{EN} > 2 V, f_{SW} = 1 MHz			2		mA
ENABLE							
V_{DIS}	Enable pin voltage to disable the device					300	mV
V_{EN}	Enable pin voltage to enable the device			1200			mV
I_{EN}	Enable pin source current			50	150	300	nA
V_{DR} AND 3.3-V REGULATORS							
V_{DR_MOSFET}	Driver voltage regulator output voltage	TPS40490MLRHD: V_{EN} ≥ 2 V, 5.6 V < V_{IN} ≤ 60 V			4.8		V
		TPS40490MHRHD: V_{EN} ≥ 2 V, 6.8 V < V_{IN} ≤ 60 V			6.8		
$V_{DR\_MOSFET\_UVLO}$	Driver voltage UVLO MOSFET rising edge	TPS40490MHRHD			6.25		V
		TPS40490MLRHD			4.4		
$V_{DR\_ACCURACY}$	Drive voltage accuracy			-4.5		4.5	%
$V_{DR\_EXT\_UVLO}$	External drive UVLO	TPS40490MHRHD			11		V
		TPS40490MLRHD			5		V
V3p3	Internal biasing supply	I_{LOAD} = 0 to 10 mA			3.2		V
FIXED AND PROGRAMMABLE UVLO							
V_{UVLO}	Programmable UVLO ON voltage			870	900	930	mV
I_{UVLO}	Hysteresis current out of UVLO pin				5		µA
REFERENCE							
V_{REF}	Reference voltage (+ input of the error amplifier)	T_J = 25°C, 6 V < V_{VIN} < 60 V		594	600	606	mV
		–40°C ≤ T_J 125°C, 6 V < V_{VIN} ≤ 60 V		588	600	612	
		–40°C ≤ T_J 125°C, 5 V < V_{VIN} ≤ 60 V		576	600	624	
OSCILLATOR							
f_{sw}	Switching frequency range	Set by external resistor	TPS40490MHRHD: V_{VIN} = 48 V	100		5400	kHz
			TPS40490MLRHD: V_{VIN} = 12 V	100		5400	

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 150°C, V_{IN} = 48 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
f_{sw_acc}	Switching frequency set accuracy	TPS40490MHRHD: V_{IN} = 48 V, Rset = 31.6 kΩ, f_{SW} = 1.15 MHz	–12.5		12.5	%
		TPS40490MLRHD: V_{IN} = 12 V, Rset = 100 kΩ, f_{SW} = 1.75 MHz	–12.5		12.5	
V_{VALLEY}	Valley voltage		0.7	1	1.31	V
K_{PWM}	PWM gain (V_{IN}/V_{RAMP})	TPS40490MLRHD: 5 V < V_{VIN} ≤ 25 V		7.5		V/V
		TPS40490MHRHD: 5 V < V_{VIN} ≤ 60 V		20		V/V
PWM AND DUTY CYCLE (PWM control)						
$t_{off(MIN)}$	Minimum off-time	5 V < V_{IN} < 60 V		70		ns
ERROR AMPLIFIER						
GBWP	Gain bandwidth product	5 V < V_{IN} < 60 V		40		MHz
A_{OL}	Open loop gain	VREF = 0.6 V		75		dB
I_{IB}	Input bias current				100	nA
I_{EAOP}	Output source current	V_{VFB} = 0 V, V_{REF} = 0.6 V, output grounded		4.2		mA
I_{EAOM}	Output sink current	V_{VFB} = 1 V, V_{REF} = 0.6 V, output connected to 3-V supply		2.5		mA
PROGRAMMABLE SOFT-START						
I_{SS}	Soft-start source current at V_{SS} < 0.5 V	V_{SS} = 0.5 V	8.5	10.5	12.5	µA
GATE DRIVERS						
V_G	Gate voltage	High side		V_{DR}-0.6		V
		Low side		V_{DR}		
R_{HDHI}	High-side driver pull-up resistance	C_L = 1 nF, V_{DR} = 5 V		0.7		Ω
R_{HDLO}	High-side driver pull-down resistance			0.35		Ω
R_{LDHI}	Low-side driver pull-up resistance			0.7		Ω
R_{LDLO}	Low-side driver pull-down resistance			0.35		Ω
t_{RC}	Drive rise time			5		ns
t_{FC}	Drive fall time			5		ns
DEAD TIME CONTROLLER (DTC) AND PROPAGATION DELAY						
$t_{DT\_H2L\_EXT}$	Dead time range HDRV fall and LDRV rise					ns

DT_3	DT_2	DT_1	T(ns)
0	0	1	7.5
0	1	1	18
1	0	1	32
1	1	1	45

$t_{DT\_L2H\_EXT}$	HDRV rise and LDRV fall					ns

D_{T3}	D_{T2}	D_{T1}	T(ns)
0	0	1	5
0	1	1	18
1	0	1	32
1	1	1	44

$t_{DT\_H2L\_INT}$	Dead time internal HDRV fall and LDRV rise **(Internal value fixed 001)**	Measured dead time will be the highest of $t_{DEAD\_TIME\_INT}$, $t_{DEAD\_TIME\_EXT}$		7.5		ns
$t_{DT\_L2H\_INT}$	Dead time internal HDRV rise and LDRV fall **(Internal value fixed 001)**	Measured dead time will be the highest of $t_{DEAD\_TIME\_INT}$, $t_{DEAD\_TIME\_EXT}$		5		ns
$t_{DEAD\_TIME\_ACC}$	Accuracy dead time setting	Percentage of set time 001 setting	–10%		10%	
t_{HPHL}	high turn-off propagation delay	Falling gate voltage, 0 ns DTC time		25		ns
t_{HPLH}	High turn-off propagation delay	Rising gate voltage, 0 ns DTC time		25		ns
t_{LPHL}	Low turn-off propagation delay	Falling gate voltage, 0 ns DTC time		25		ns
t_{LPLH}	Low turn-off propagation delay	Rising gate voltage, 0 ns DTC time		25		ns
	Delay matching	HS gate off to LS gate ON, 0 ns DTC time	–4	0	4	ns

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 150°C, V_{IN} = 48 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
OVERCURRENT PROTECTION (LOW-SIDE MOSFET SENSING)						
ILIM_PIN	ILIM pin voltage	5 V < V_{IN} < 60 V, T_J = 25°C		1.23		V
ILIM_Tc	Temperature coefficient of ILIM current	5 V < V_{IN} < 60 V		25		ppm
THERMAL SHUTDOWN						
T_{TRIP}	Thermal S/D trip point	Rising temperature		160		°C
T_{HYST}	Thermal S/D hysteresis	Device re-starts		140		°C
$T_{TRIP\_DEGLITCH}$	Thermal S/D deglitch			110		µS
POWER GOOD						
VUV_{BUCKX}	Under voltage threshold	Output falling		80		%
		Output rising (PGOOD asserted)		90		%
$t_{BUCKUV\_deglitch}$	Deglitch time	Both edges		110		us
$t_{VINUV\_deglitch}$	Deglitch time	Both edges		110		us
t_{ON_HICCUP}	Hiccup mode ON time	VUV_{BUCKX} asserted		10		ms
t_{OFF_HICCUP}	Hiccup mode OFF time	Converter disabled. Once t_{OFF_HICCUP} elapses, converter will go through start-up again		100		ms
VOV_{BUCKX}	Threshold voltage for buck OVP % of Vset	Output rising (high side FET will be forced off)		114		%

TYPICAL CHARACTERISTICS

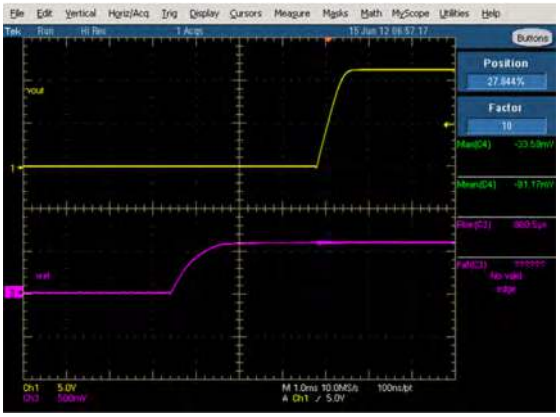


Figure 1. Vref and Vout start-Up Vin=48V Vo=12V

Figure 2. SS Vin=24V, Cref=1nF, CVdr=1µF, Cv3V=1µF, css=68nF, Io=5.5A

Figure 3. Start-up 15Vin Vo=5.8V, 6A, 5MHz

Figure 4. Start-up 22Vin Vo=5.8V, 6A, 5MHz

Figure 5. Soft-Start with Vout connected to Vdr_ext with diode +20 Ω 200µF Yellow=Vout, Purple=Vdr_ext Blue=Vdr, Green=IC current

Figure 6. Detailed start-up operation, 24Vin, Vo=12V, 6A Ch1 (yellow): FB pin (negative input to the error amplifier), Ch2 (blue): Vout,

TYPICAL CHARACTERISTICS (continued)

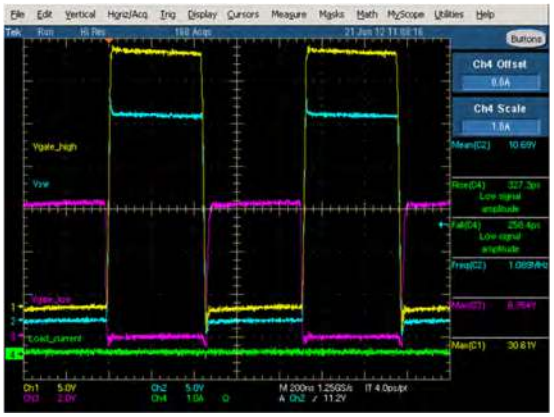


Figure 7. Switching node signals 24Vin, Vo=12V, 0A
Ch1 (yellow): Vgate_high (measured on FET),
Ch2 (blue): switching node, Ch3 (purple): Vgate_low
(measured on FET), Ch4 (green): Load current

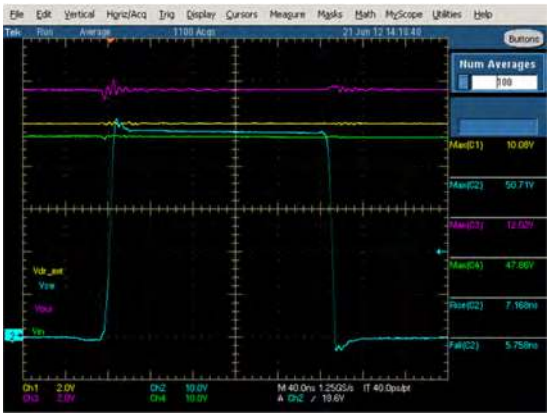


Figure 8. Switching node signals 24Vin, Vo=12V, 6A
Ch1 (yellow): Vdrive_external), Ch2 (blue): switching node
Ch3 (purple): Vout, Ch4 (green): Vin

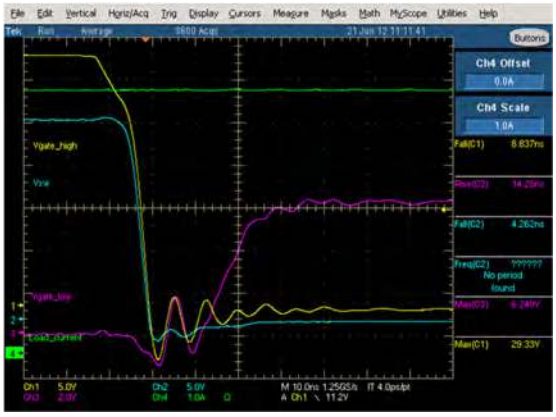


Figure 9. Detailed fall time plots, 24Vin, Vo=12V 6A out
Ch1 (yellow): Vgate_high (measured on FET),
Ch2 (blue): switching node Ch3 (purple): Vgate_low
(measured on FET), Ch4 (green): Load current.

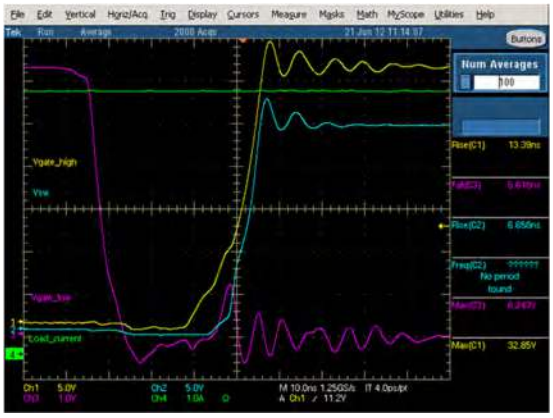


Figure 10. Detailed rise time plots, 24Vin, Vo=12V 6A out
Ch1 (yellow): Vgate_high (measured on FET),
Ch2 (blue): switching node Ch3 (purple): Vgate_low
(measured on FET), Ch4 (green): Load current.

Figure 11. Sw node 1.8MHz

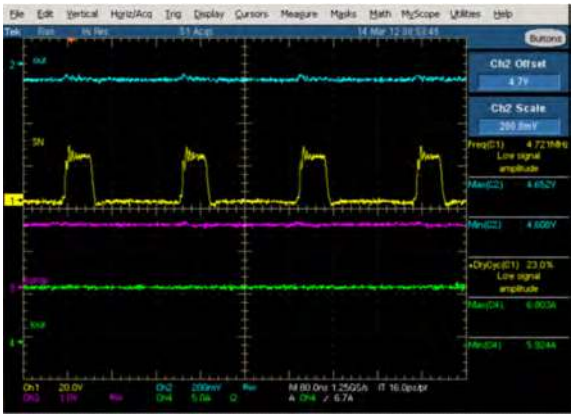


Figure 12. Sw node 4.7MHz operation 22Vin Vo=4.7V, Io=6A
Ch1 (yellow): Switching node, Ch2 (blue): Vout
Ch3 (purple): COMP, Ch4 (green): Load current.

TYPICAL CHARACTERISTICS (continued)

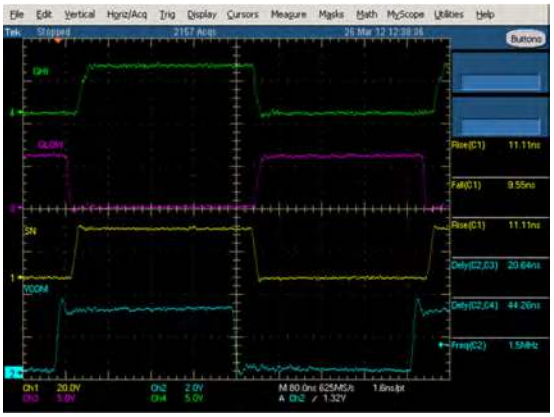


Figure 13. Gate drive and switching node fsw=1.5MHz, no load

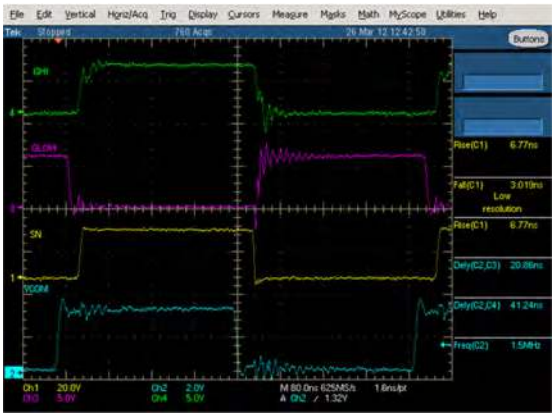


Figure 14. Gate drive and switching node fsw=1.5MHz, Io=7A

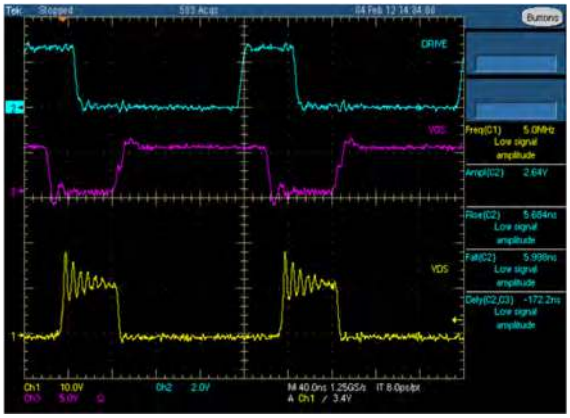


Figure 15. High Gate drive and switching node, fsw= 5MHz

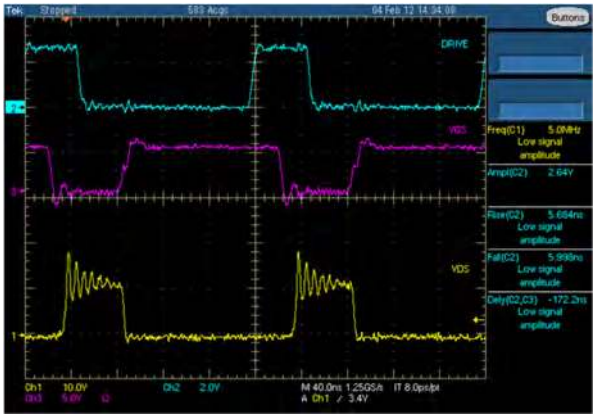


Figure 16. Low Gate drive and switching node, fsw=5MHz

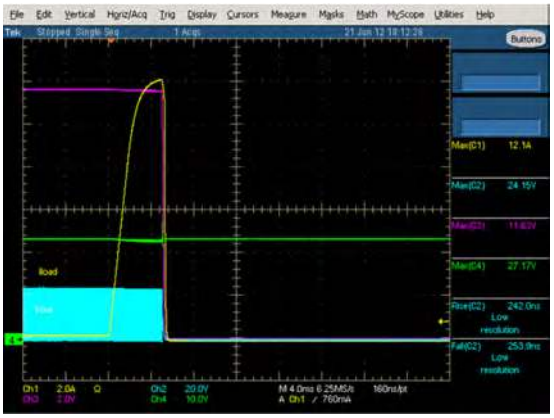


Figure 17. Current limit operation Rds_on= 13mΩ, Rlim=128kΩ Ch1 (yellow): output current, Ch2 (blue): switching node Ch3 (purple): output voltage, Ch4 (green): input voltage

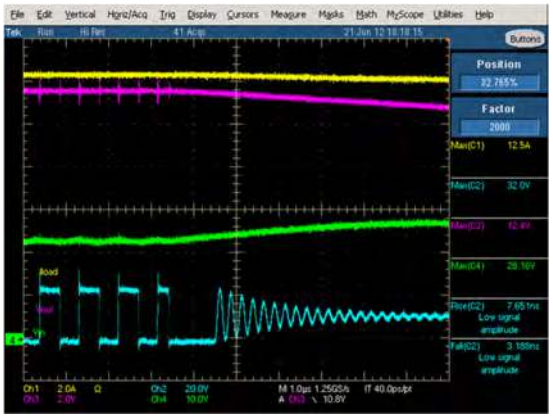


Figure 18. Expanded Current limit operation Rds_on= 13mΩ, Rlim=128kΩ Ch1 (yellow): output current, Ch2 (blue): switching node Ch3 (purple): output voltage, Ch4 (green): input voltage.

TYPICAL CHARACTERISTICS (continued)

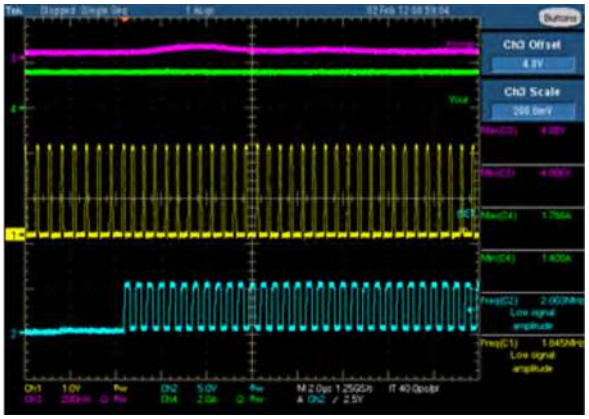


Figure 19. Sync at 2MHz, Vin=24V, Vo=5V From top to bottom COMP, Iout, Vsw, vsync

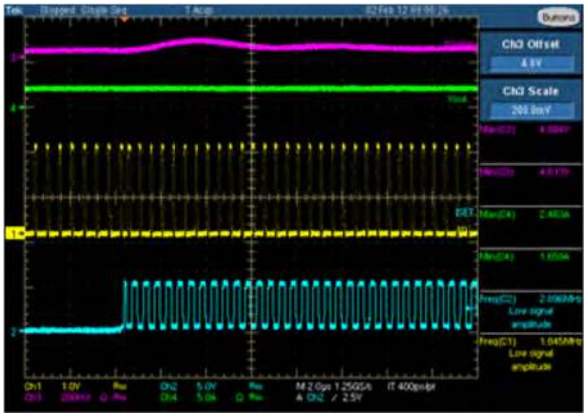


Figure 20. Sync at 3MHz, Vin=24V, Vo=5V COMP, Iout, Vsw, vsync

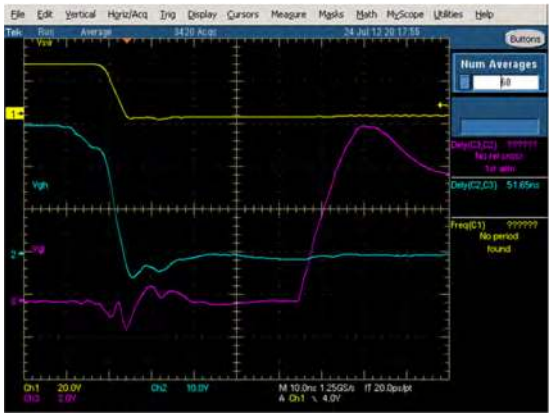


Figure 21. Dead time setting to 111 (42ns typ)
Ch1 (yellow): Switching node, Ch2 (blue): Vg high side
Ch3 (purple): Vg low side

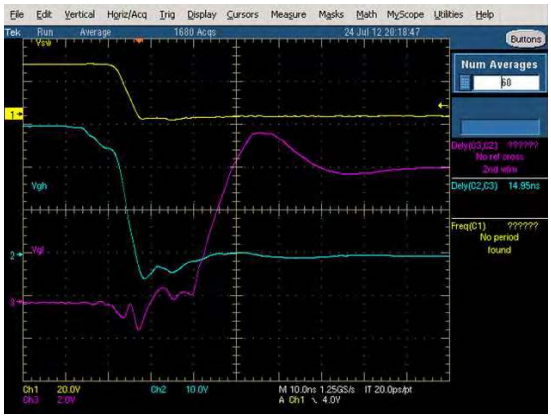


Figure 22. Dead time setting to 011 (18ns typ)
Ch1 (yellow): Switching node, Ch2 (blue): Vg high side
Ch3 (purple): Vg low side

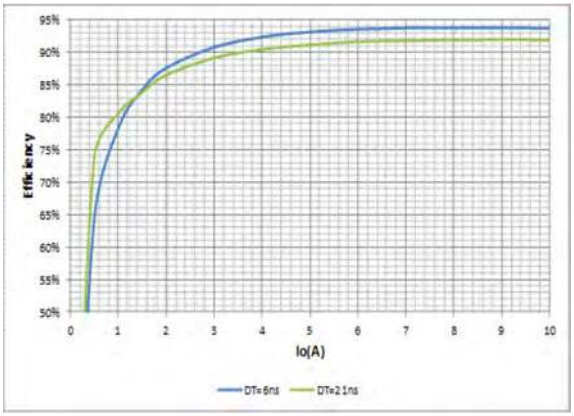


Figure 23. System efficiency improvement with different dead times Vin=12 Vo= 3.3V 1.25MHz

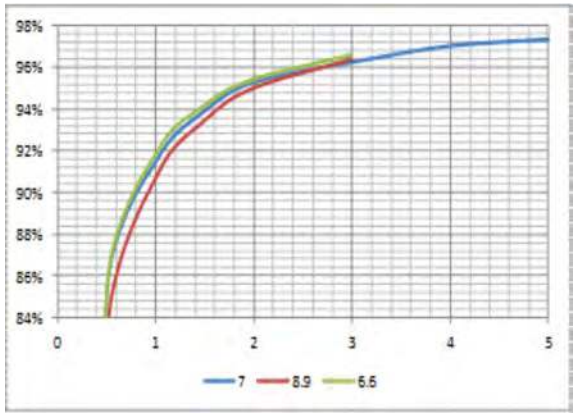


Figure 24. System efficiency variation with gate drive voltage Vin=48V, Vo=30V, f=1.25MHz 80V MOSFETs (for information only)

TYPICAL CHARACTERISTICS (continued)

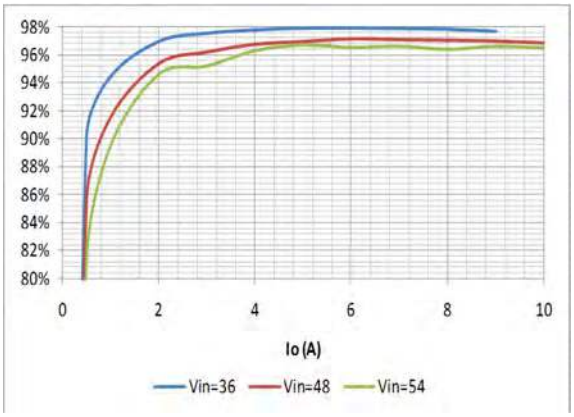


Figure 25. Efficiency at Vo=30V

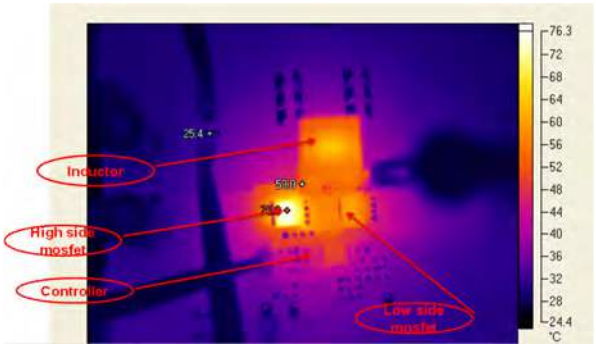


Figure 26. Thermal plot (forced air) Vin=36V Vo=30V, Io=6A fsw=1MHz, TA=25°C

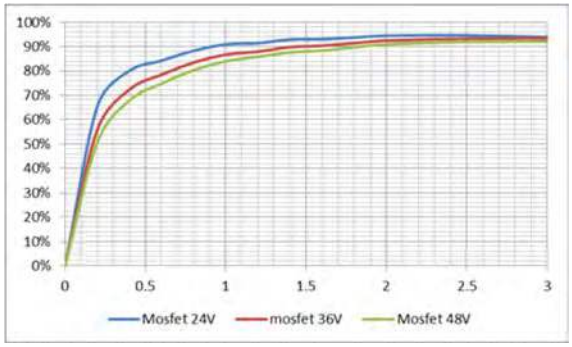


Figure 27. 1.1MHz Vo=12V efficiency with MOSFET BSC123N08NS3G

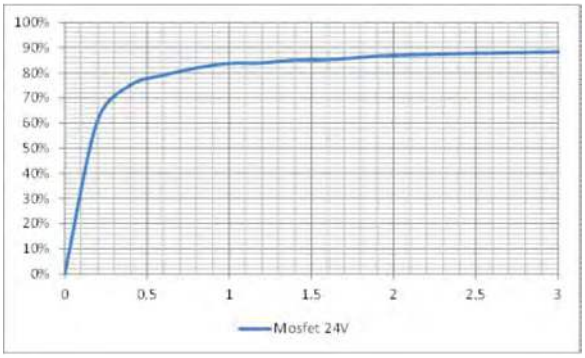


Figure 28. 2.5MHz Vo=12V efficiency with MOSFET BSC123N08NS3G

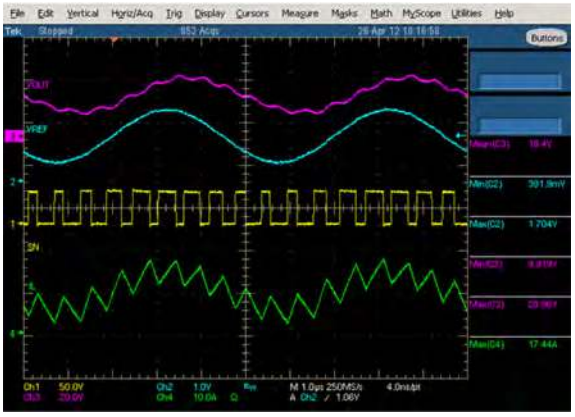


Figure 29. 200kHz Modulated output 10-30V, 3Ω load, fsw=1.5MHz

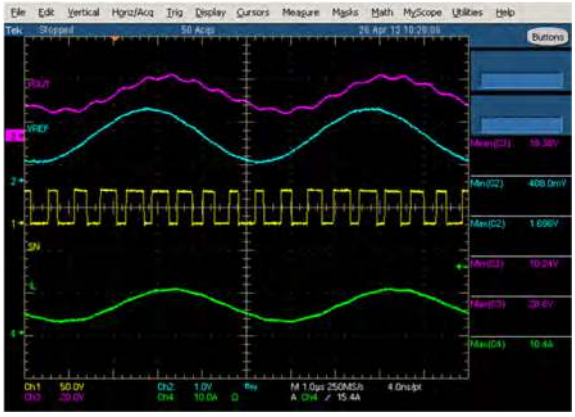


Figure 30. 200kHz modulated output 5-15V, 1.5Ω load, fsw= 1.5MHz

TYPICAL CHARACTERISTICS (continued)

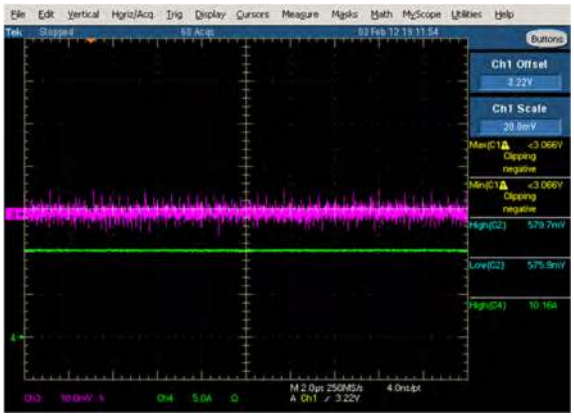


Figure 31. Ripple 18Vin Vo=3.3V, 10A 2.25MHz

Figure 32. Ripple 8Vin Vo=6V, 6A 5MHz

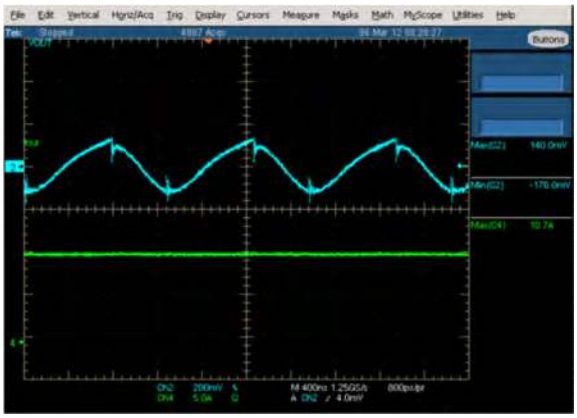


Figure 33. Ripple at 1MHz Vin=48V, Vo=30V, Io=10A Lo=1µH, Co=12µF ceramic

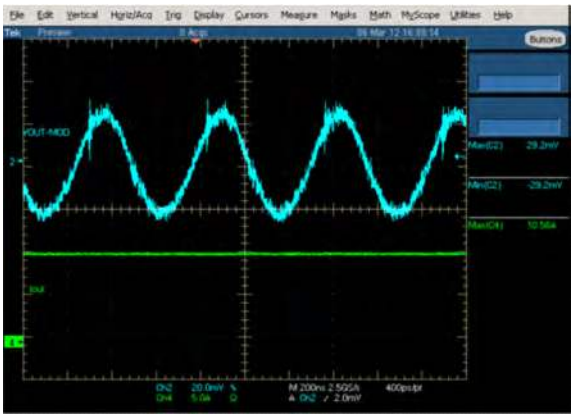


Figure 34. Ripple at 1MHz Vin=48V, Vo=30V, Io=10A Lo=1µH, Co=12µF ceramic +470µF electrolytic

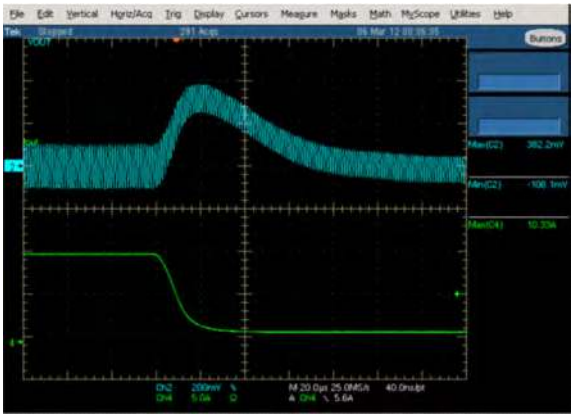


Figure 35. Transient response, 10A step down load1MHz Vin=48V, Vo=30V, Io=10A Lo=1µH, Co=12µF ceramic

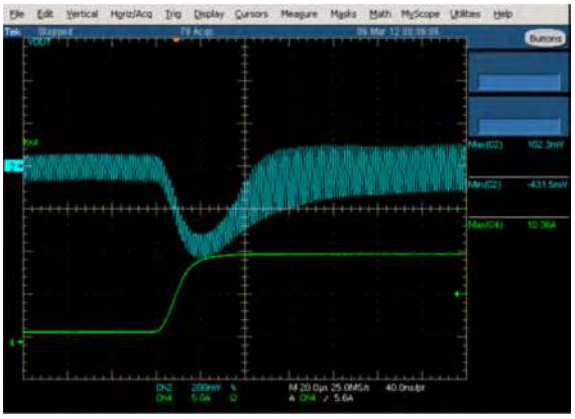


Figure 36. Transient response, 10A step down load1MHz Vin=48V, Vo=30V, Io=10A Lo=1µH, Co=12µF ceramic

TYPICAL CHARACTERISTICS (continued)

Figure 37. Transient step response
Vin=15V, Vo=3.3V 2.2MHz 1-8A

Figure 38. Transient step response
Vin=24V, Vo=5V 5MHz 1-10A Fc=140kHz

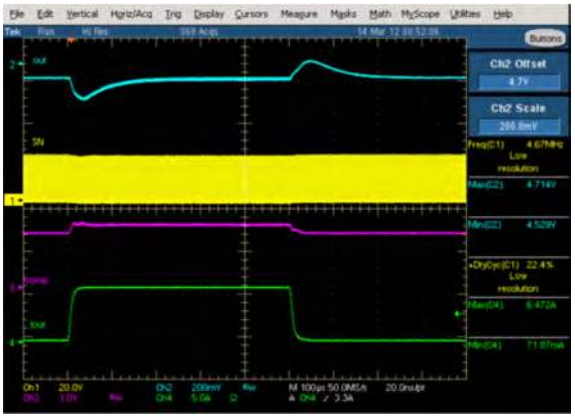


Figure 39. Transient step response
Vin=24V, Vo=5V 5MHz 1-7A,Fc=140kHz
Ch1 (yellow):Switching node, Ch2 (blue):Vo,
Ch3 (purple): COMP, CH4(green): Io

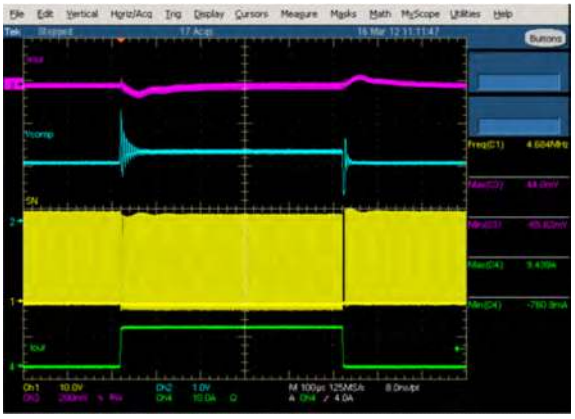


Figure 40. Transient step response
Vin=24V, Vo=5V 5MHz 1-7A,Fc=600kHz
Ch1 (yellow): Switching node, Ch2 (blue):COMP,
Ch3 (purple): Vo, CH4(green): Io

Figure 41. Steady state operation
Vin=12, Vo=3.3V 5MHz No load Ch1 (yellow):
Switching node, Ch3 (purple): Vout, CH4(green): Io

Figure 42. Steady state operation
Vin=12, Vo=3.3V 5MHz 5A Ch1 (yellow):
Switching node, Ch3 (purple): Vout, CH4(green): Io

TYPICAL CHARACTERISTICS (continued)

Figure 43. 0-5A step load Vin=12 Vo=3.3V fsw=5MHz, Ch3 (purple): Vout, CH4(green): Io

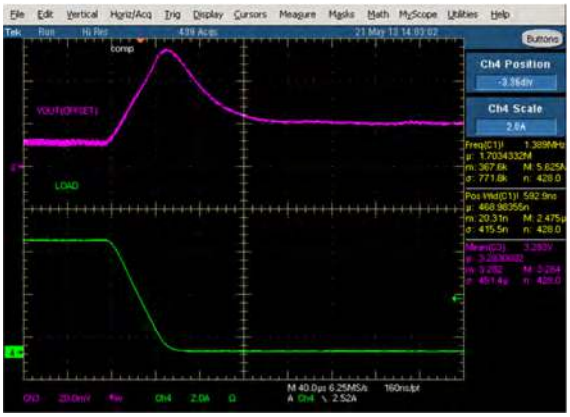
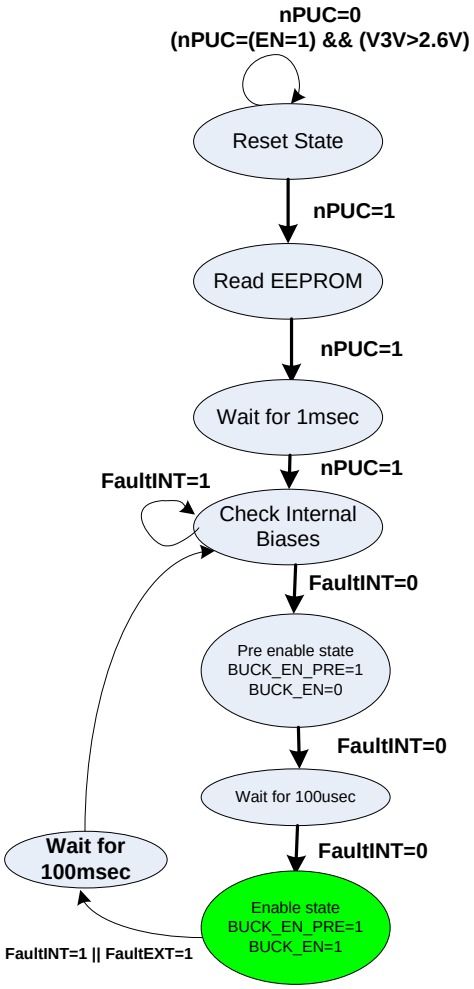


Figure 44. 5-0A load dump Vin=12 Vo=3.3V fsw=5MHz, Ch3 (purple): Vout, CH4(green): Io

TPS40490 STATE MACHINE



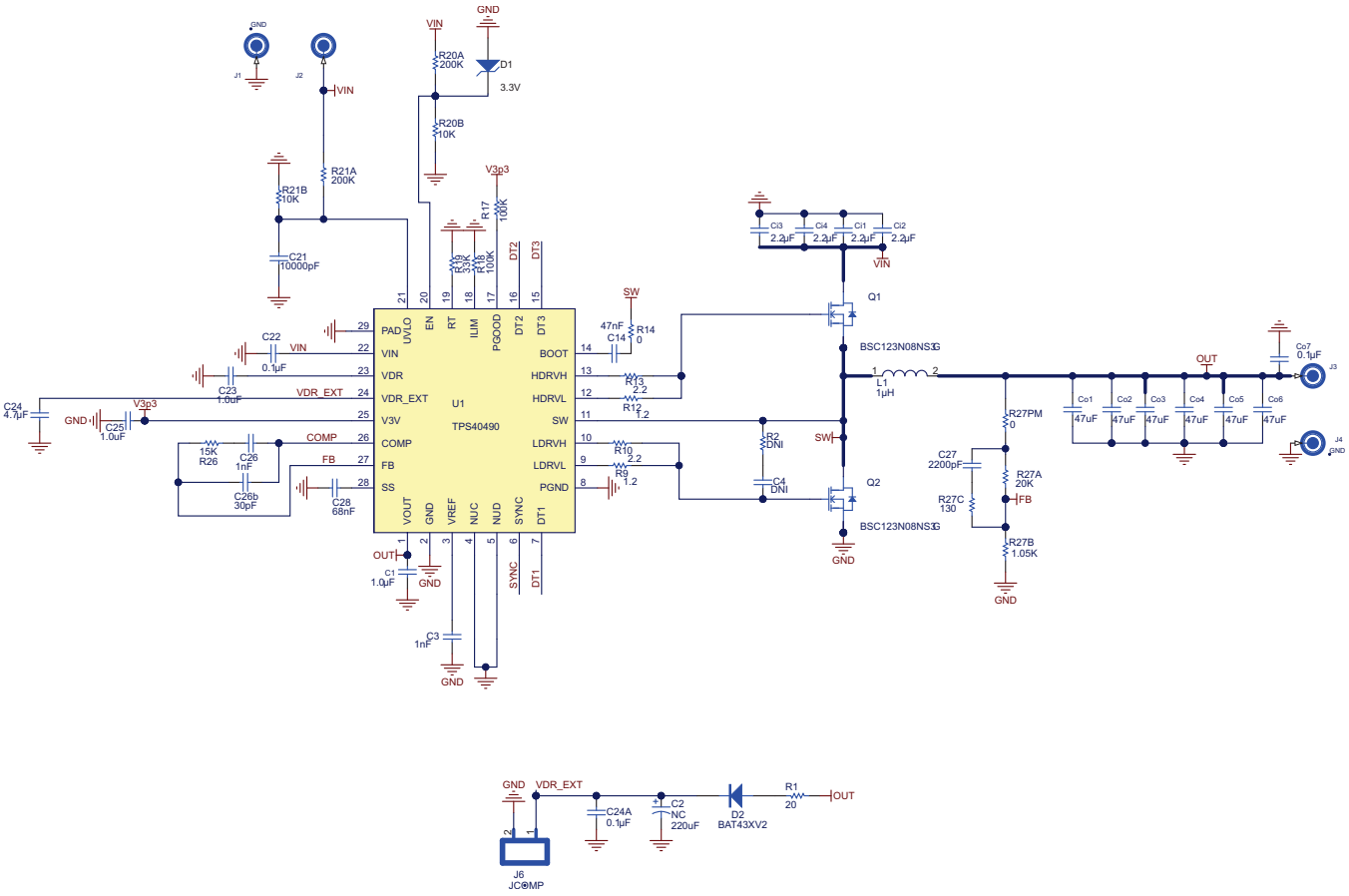
FaultINT=(VDRV_UVdeg=1) || (VINUVdeg=1) || (OTSdeg=1)

FaultEXT=(VBUCK_UVdeg=1) || (ILIM_LATCH=1)

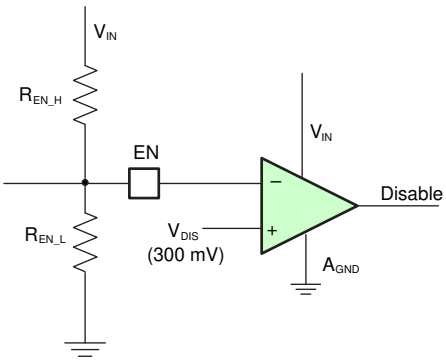
APPLICATION INFORMATION

TYPICAL APPLICATION CIRCUIT

The following page contains the TPS40490 application circuit.

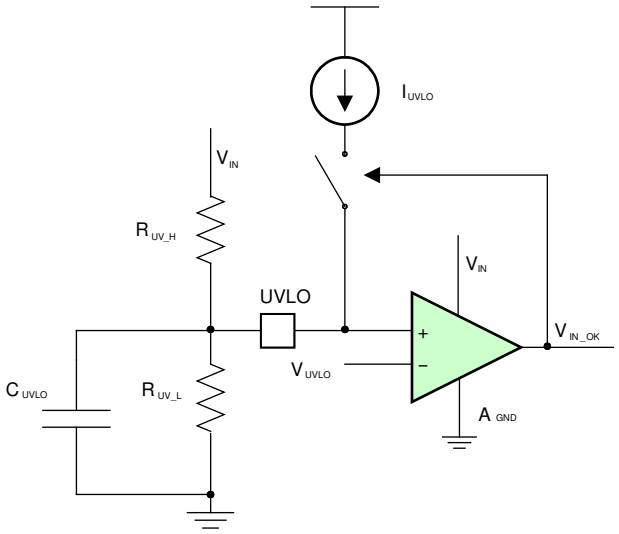


ENABLE CIRCUIT



The internal LDOs are enabled if the enable pin is higher than V_{EN}. When V_{EN} is less than 300 mV, the device is fully disabled and the current consumption is less than 2 µA. The internal LDOs are actively discharged. The enable pin must not be allowed to float. If the function is not needed for the design, EN should be pulled up to V_{IN} by a high value resistor ensuring that the current into the enable pin does not exceed 10 µA. If it is not possible to meet this clamp current requirement, a resistor divider from V_{IN} to GND be used to connect to EN. The resistor divider should be such that the enable pin should be higher than V_{EN} and lower than 3.3 V. A capacitor can be used to provide additional start-up delay. To avoid potential erroneous behavior of the enable function, the enable signal applied must have a minimum slew rate of 20 V/s.

UVLO CIRCUIT



TPS40490 has both fixed and programmable input UVLO. For the device to turn-on, the enable pin must be greater than V_{EN} and the UVLO voltage higher than 900 mV (typ). Once the input voltage reaches UVLO, a small 5-µA hysteresis current source is switched on.

To calculate the UVLO divider use the following formula:

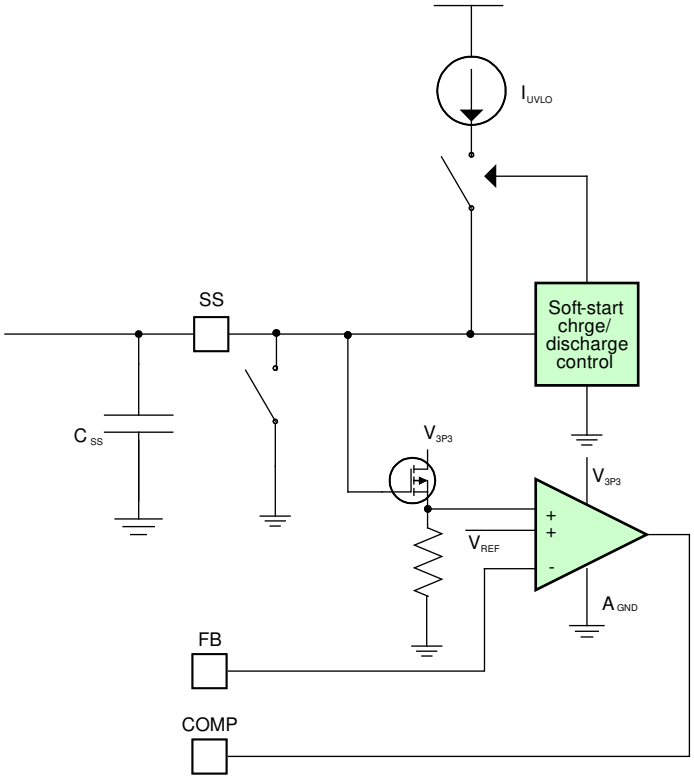
$R_{UV\_H} = (V_{ON} – V_{OFF})/I_{UVLO}$

$R_{UV\_L} = R_{UV\_H} \times V_{UVLO}/(V_{ON}–V_{UVLO})$

Where:

V_{ON} = Desired turn-on voltage
V_{OFF} = Desired turn-off voltage
I_{UVLO} = Hysteresis current (5 µA)
V_{UVLO} = UVLO threshold voltage

SOFT-START



As the SS pin voltage approaches 0.65 V, the positive input to the error amplifier begins to rise and the output of the error amplifier (COMP pin) starts rising. The rate of rise of the COMP voltage is mainly limited by the feedback loop compensation network. Switching begins once VCOMP reaches the valley of the PWM ramp. The output is regulated to the error amplifier input through the FB pin in the feedback loop. When the FB pin reaches the 600-mV reference voltage, the feedback node is regulated to the reference voltage, VREF. The SS pin continues to rise and is clamped to VDD.

The formula to calculate the soft-start capacitor is

$C_{SS} = t_{ss}/0.09$
C_{SS} = Soft-Start capacitance (nF)
t_{SS} = Soft-Start time (ms)

OSCILLATOR AND V_{IN} FEED-FORWARD

The resistor at the RT pin sets the current. The proportional current charges an internal 20-pF oscillator capacitor. The ramp voltage on this capacitor is compared with the RT pin voltage, VRT. Once the ramp voltage reaches VRT, the oscillator capacitor is discharged. The ramp that is generated by the oscillator (which is proportional to the input voltage) acts as a voltage feed-forward ramp to be used in the PWM comparator.

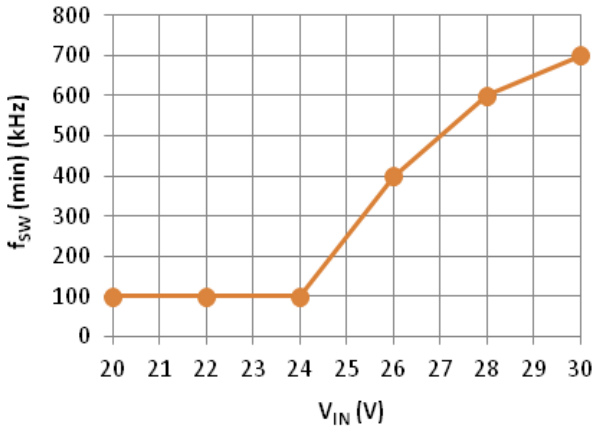
The frequency of operation of the device can be set according to the following formulae:

TPS40490MHRHDR: R_T (kΩ) = 37.5/f_{SW} (MHz) (1)

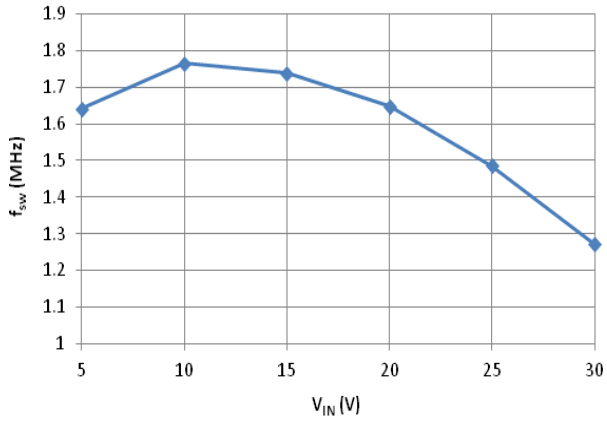
TPS40490MLRHDR: R_T (kΩ) = 176.5/f_{SW} (MHz) (2)

It is important to keep in mind the following two requirements when using TPS40490MLRHDR with operating voltage in the 24 V to 30 V range:

1. There is a restriction on the minimum set frequency for voltages as the following graph shows.



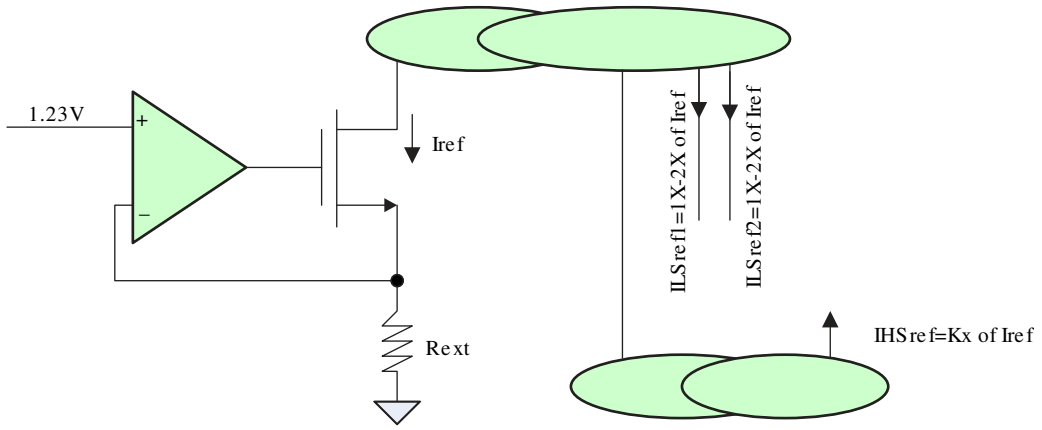
2. There is a shift in the switching frequency as the following graph shows for a setting of 1.7 MHz at 12 V.



External Clock

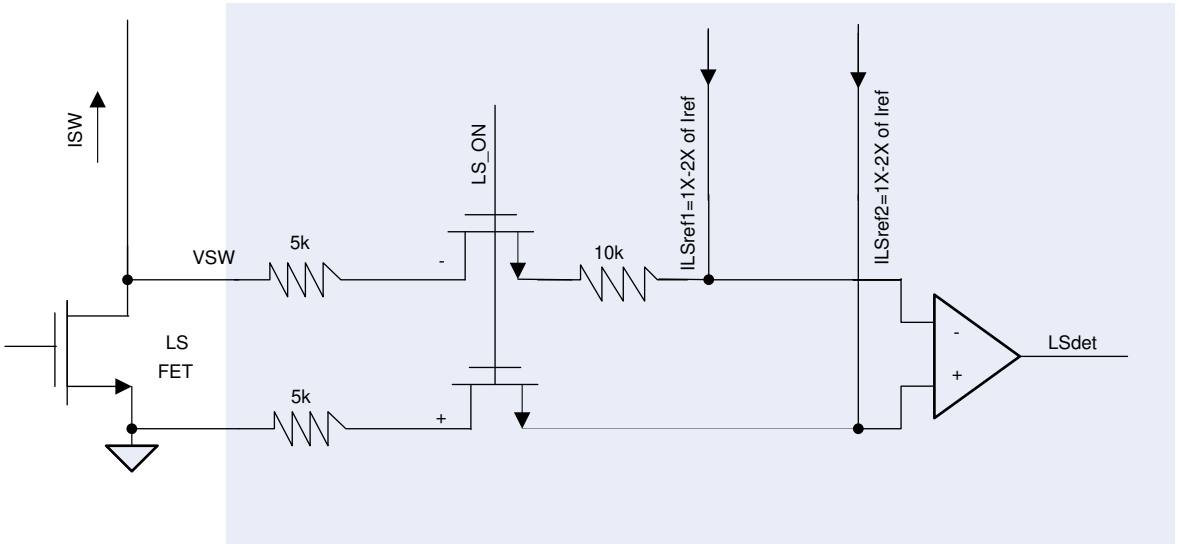
When synchronization is applied, the PWM oscillator frequency must be lower (70-80%) than the sync pulse frequency. The SYNC pin will be ignored during start-up and when PGOOD is not asserted. The SYNC pin must be tied to GND when the feature is not used.

Current Limit Operation



There are two different current limit mechanisms in TPS40490, high-side (HS) and low-side (LS). HS and LS values are adjustable through an external resistor Rext. A reference current of 1.23 V/RESext is generated first. This current is going to be mirrored for HS and LS. The current limit circuit does not have temperature adjustment.

Low Side Current Limit

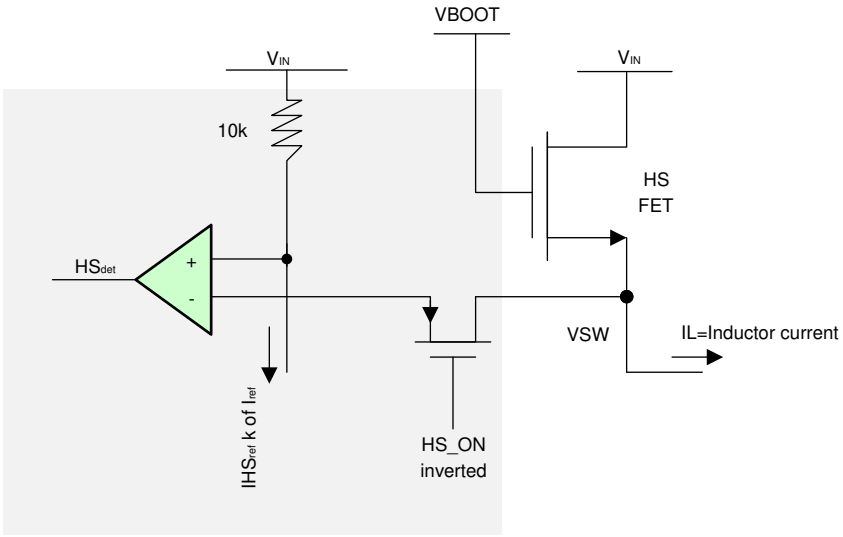


The formula to calculate the low side current limit is,

$$I_{LS-lim} = 1.75 \frac{10k}{R_{LS\_ON}} \frac{1.23}{R_{ext}} \quad (3)$$

where R_{LS_ON} is LS switch on resistance.

High Side Current Limit

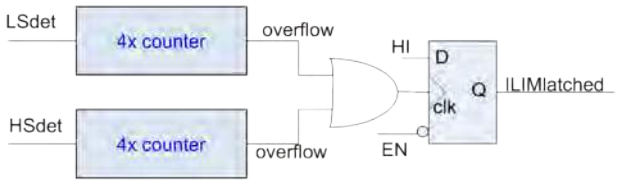


The formula to calculate the high side current limit is,

$$I_{HS-lim} = K \frac{10k}{R_{HS\_ON}} \frac{1.23}{R_{ext}} \quad (4)$$

where R_{HS_ON} is high-side switch on resistance and K is the current limit multiple (5).

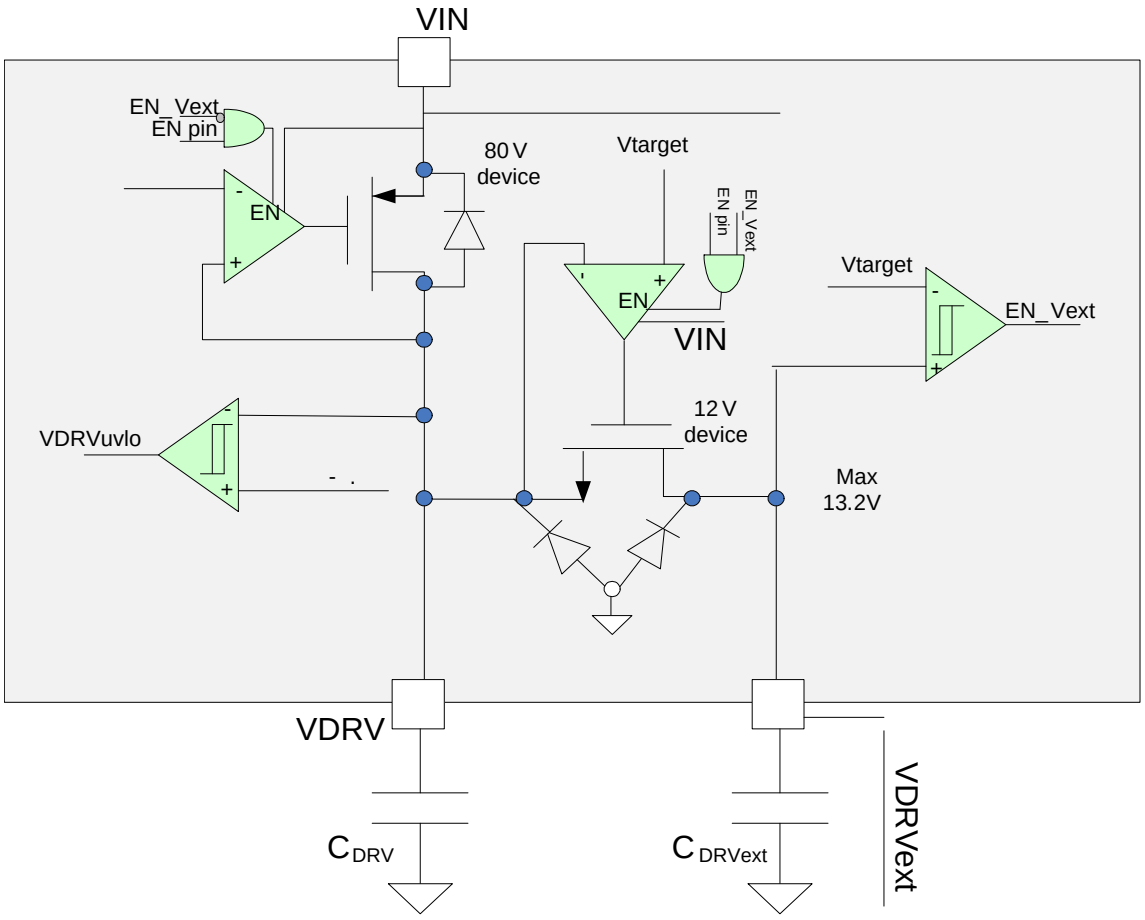
Shut-Down Counter



HS and LS current detect signals will go to the input of a 4x up/down counter. If there is a current limit detect, the counter will count up. In the next cycle, if there is another current limit detect, the counter counts up again, but if there is no current limit detected, the counter counts down and when at zero count, it stays there.

If there are consecutive current faults, the counter overflows, and ILIMlatched will be set to 1. This will inform the digital core of a current limit fault, the driver and oscillator will be disabled and a new soft-start will be initiated after 100 ms.

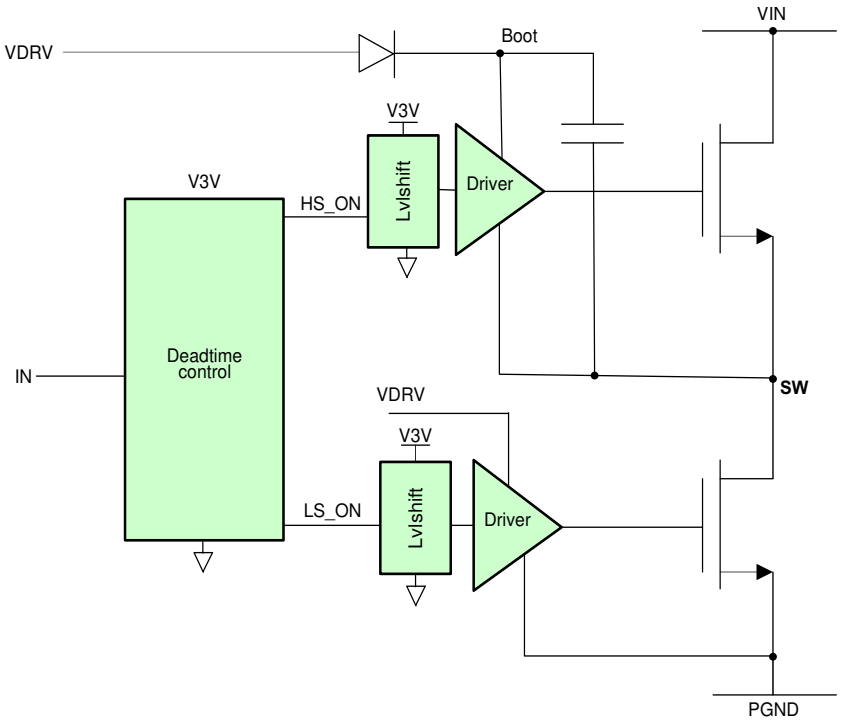
V_{DR} and V_{DR_EXT}



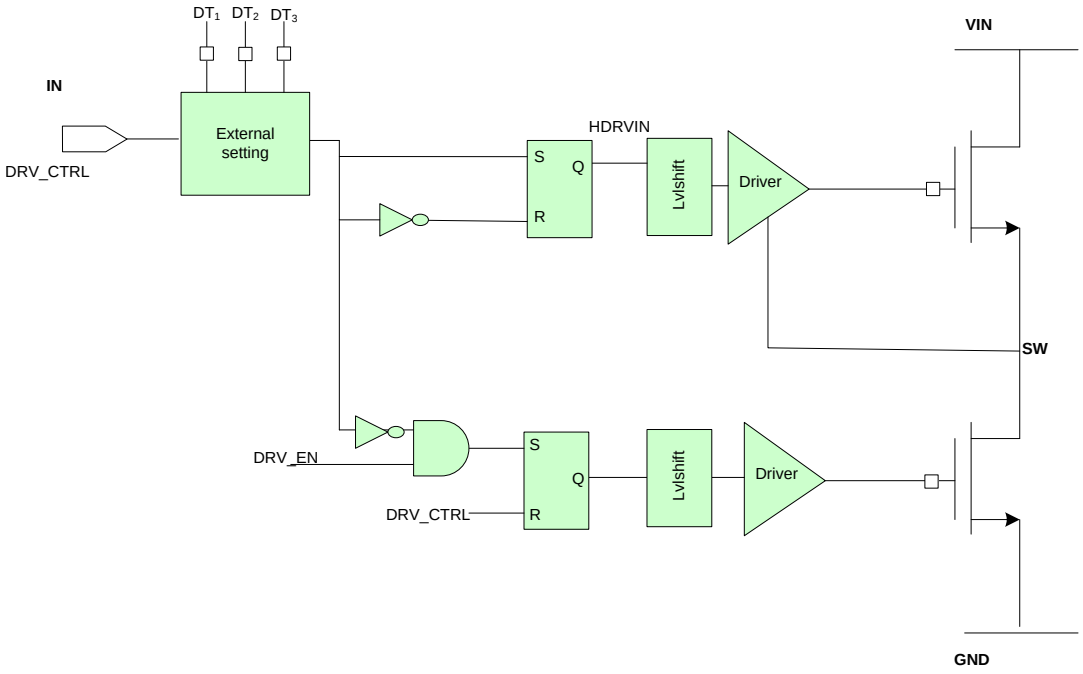
The driver voltage is set to 4.8 V or 6.8 V according to the device version. If an external drive voltage is applied, the internal driver voltage will be regulated internally to pre-set factory voltage. The decoupling capacitor should be fitted very close to the VDR and VDR_EXT.

Driver Circuits

The high side driver is designed as a floating driver that can be connected either as a high side in a system operating up to 60 V or connected to ground with a programmable dead time controller.



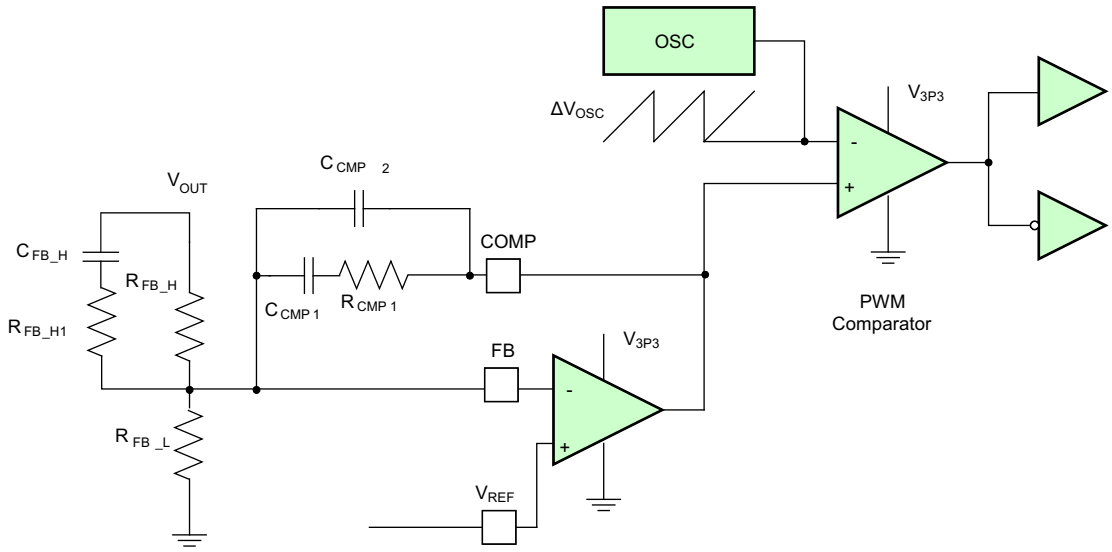
Fixed Dead Time Control



The device is provided with a programmed dead time of 6 ns and can be increased by setting the DT_1 to DT_3 pins.

Feed-Forward PWM Mode

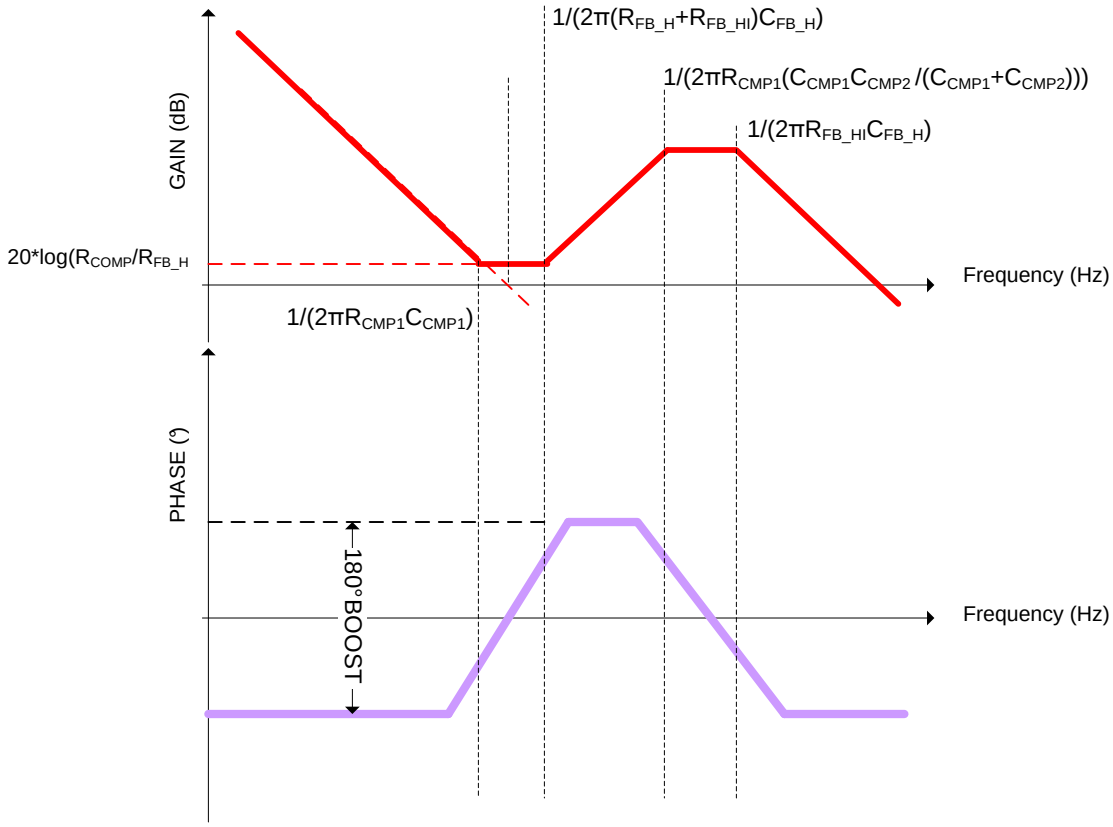
The configuration for PWM operation is shown in the following figure.



A type 3 compensation circuit is recommended for this type of operation. It's transfer function is:

$$GAIN_{T3} = \frac{R_{FB\_H1} + R_{FB\_H}}{R_{FB\_H1} * R_{FB\_H} * C_{CMP2}} * \frac{\left(s + \frac{1}{R_{CMP1} * C_{CMP1}}\right) * \left(s + \frac{1}{\left(R_{FB\_H1} + R_{FB\_H}\right) * C_{FB\_H}}\right)}{s * \left(s + \frac{C_{CMP1} + C_{CMP}}{R_{CMP1} * C_{CMP1} * C_{CMP1}}\right) * \left(s + \frac{1}{\left(R_{FB\_H1}\right) * C_{FB\_H}}\right)} \quad (5)$$

A typical transfer function plot is:



The system gain is:

$$SYS_{GAIN} = \frac{R_{FB\_H1} + R_{FB\_H}}{R_{FB\_H1} * R_{FB\_H} * C_{CMP2}} * \frac{\left(s + \frac{1}{R_{CMP1} * C_{CMP1}}\right) * \left(s + \frac{1}{\left(R_{FB\_H1} + R_{FB\_H}\right) * C_{FB\_H}}\right)}{s * \left(s + \frac{C_{CMP1} + C_{CMP}}{R_{CMP1} * C_{CMP1} * C_{CMP1}}\right) * \left(s + \frac{1}{\left(R_{FB\_H1}\right) * C_{FB\_H}}\right)} * \frac{V_{IN}}{\Delta V_{OSC}} * \frac{1 + s * ESR * C_{OUT}}{1 + s * (ESR + DCR) * C_{OUT} + s^2 * L_{OUT} * C_{OUT}} \quad (6)$$

To calculate the external compensation components follow the following steps:

ACTION	FORMULA	COMMENT
Define switching frequency (f_{SW}), output filter parameters, L and C, output filter resonant frequency and output capacitor ESR zero frequency.	$f_{LC} = \frac{1}{2\pi\sqrt{I_{OUT} \cdot C_{OUT}}}$ (7) $f_{ESR} = \frac{1}{2\pi \cdot ESR \cdot C_{OUT}}$ (8)	
Pick R_{FB_H}		Suggested to use a value lower than 10 kΩ.
Calculate R_{FB_L}	$R_{FB\_L} = \frac{R_{FB\_H}}{\frac{V_{OUT}}{V_{REF}} - 1}$ (9)	Set the value according to required output voltage.
Determine loop desired bandwidth	BW = 1/5th to 1/10th of f_{SW} (10)	Suggested range
Calculate R_{CMP1}	$R_{CMP1} = \frac{BW}{f_{LC} \cdot K_{PWM}} \cdot R_{FB\_H}$ (11)	Used to achieve the desired bandwidth
Calculate C_{CMP1}	$C_{CMP1} = \frac{1}{\pi \cdot f_{LC} \cdot K_{PWM}}$ (12)	Places a zero at ~50% of the output filter double pole frequency
Calculate C_{CMP2}	$C_{CMP2} = \frac{1}{2\pi \cdot R_{CMP1} \cdot C_{PCMP1} \cdot f_{ESR} - 1}$ (13)	Places first pole at the output capacitor ESR frequency
Calculate R_{FB_H1}	$R_{FB\_H1} = \frac{R_{FB\_H}}{\frac{f_{SW}}{2 \cdot f_{LC}} - 1}$ (14)	Places second pole at half the switching frequency
Calculate C_{FB_H}	$C_{FB\_H} = \frac{1}{\pi \cdot R_{FB\_H1} \cdot f_{SW}}$ (15)	Places second zero at the output filter double pole

Minimum Controllable On-Time

When operating in voltage mode control TPS40490 does not have any restrictions associated with a minimum on-time (as it occurs with current mode control circuits due to the blanking of the leading edge inductor current).

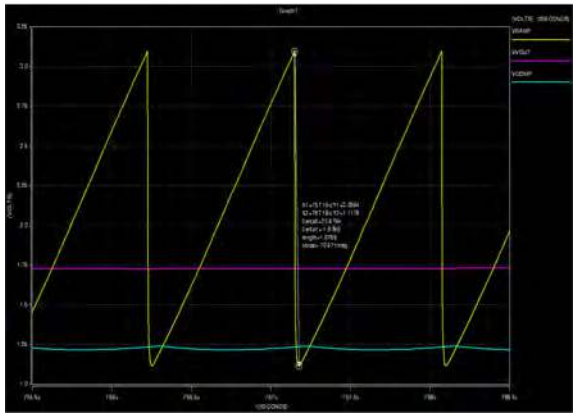


Figure 45. Simulation Plot Showing Error (COMP) VoltageRequired to Provide a Narrow Switching Pulse

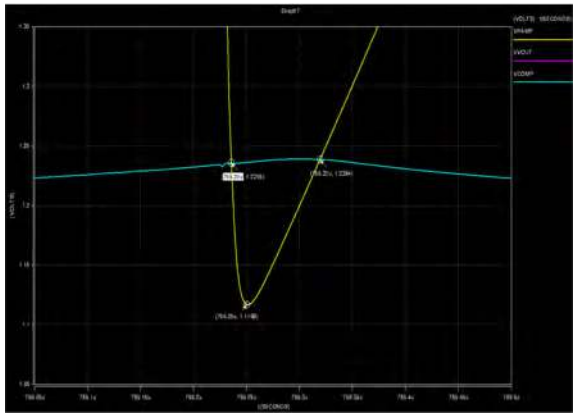
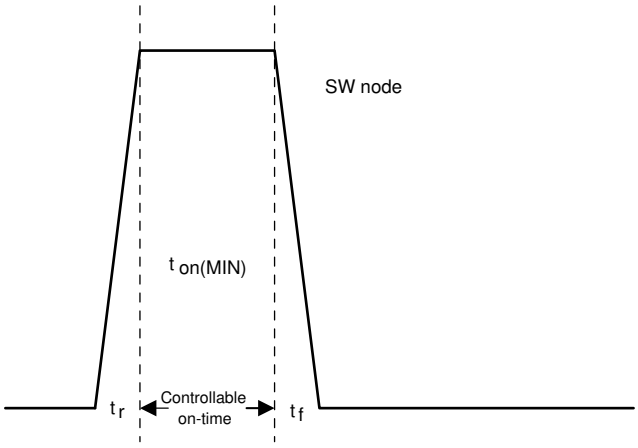


Figure 46. Detail of Error (COMP) Voltage and PWM Ramp

As the simulation plots show the difference between the start of the PWM ramp and the error voltage is around 100 mV or less, therefore generating specific challenges on applications requiring a narrow pulse operation:

1. Attention must be paid to layout to avoid noise imposed on the COMP and internal ramp to avoid spurious trips of the PWM comparator.
2. It is important to pick the right transistor for the application. If rise and fall times are comparable to the minimum on time, it is possible to have a jitter effect on the switching node.



The combined rise and fall time (t_r and t_f shown above) should meet the following:

$$t_r + t_f < 0.1 \times t_{on(MIN)}$$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS40490MHRHDR	ACTIVE	VQFN	RHD	28	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 150	TPS 40490MH	Samples
TPS40490MHRHDT	ACTIVE	VQFN	RHD	28	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 150	TPS 40490MH	Samples
TPS40490MLRHDR	PREVIEW	VQFN	RHD	28	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 150	TPS 40490ML	
TPS40490MLRHDT	PREVIEW	VQFN	RHD	28	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 150	TPS 40490ML	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

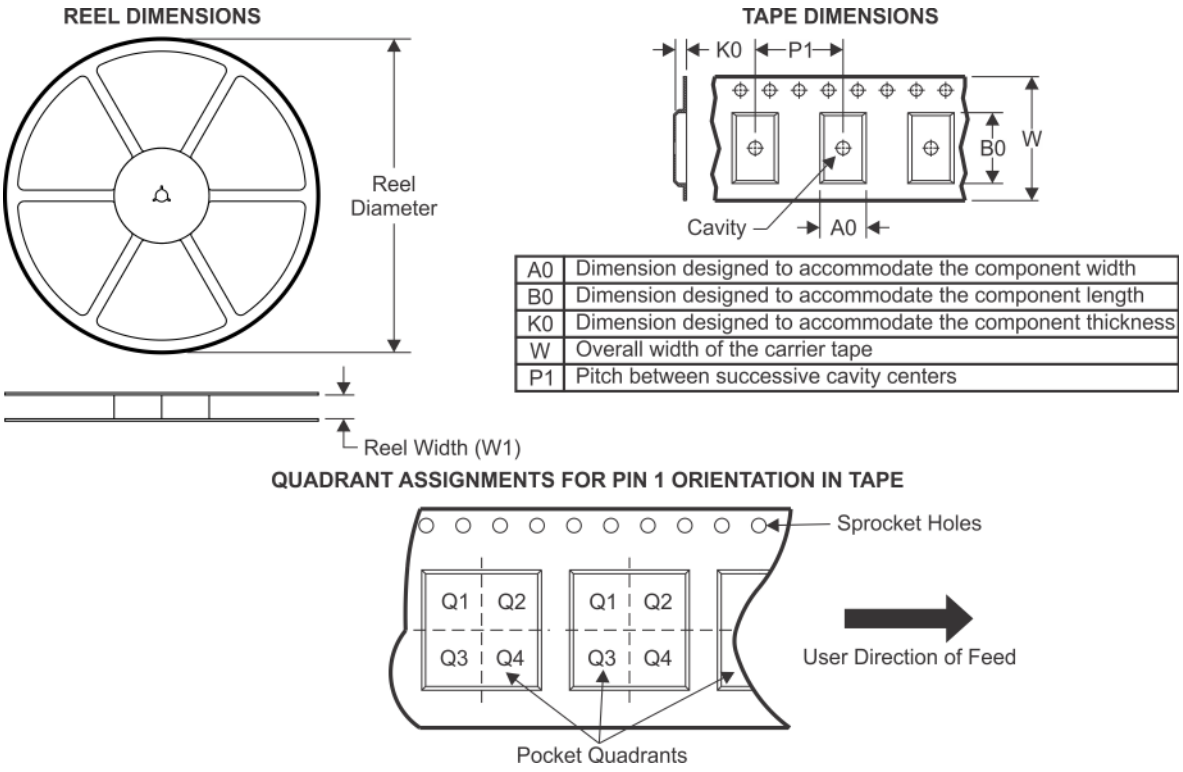
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

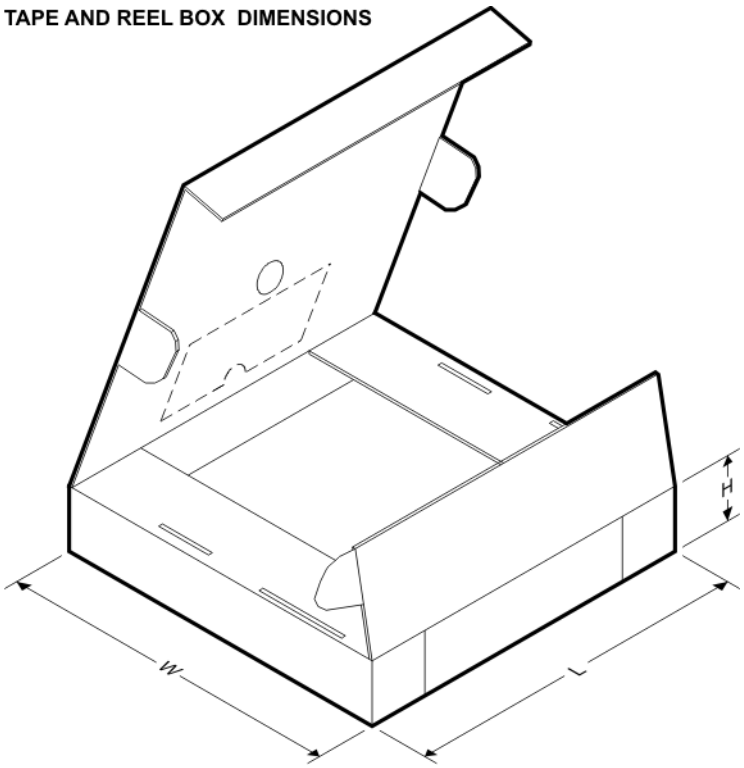


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40490MHRHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS40490MHRHDT	VQFN	RHD	28	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

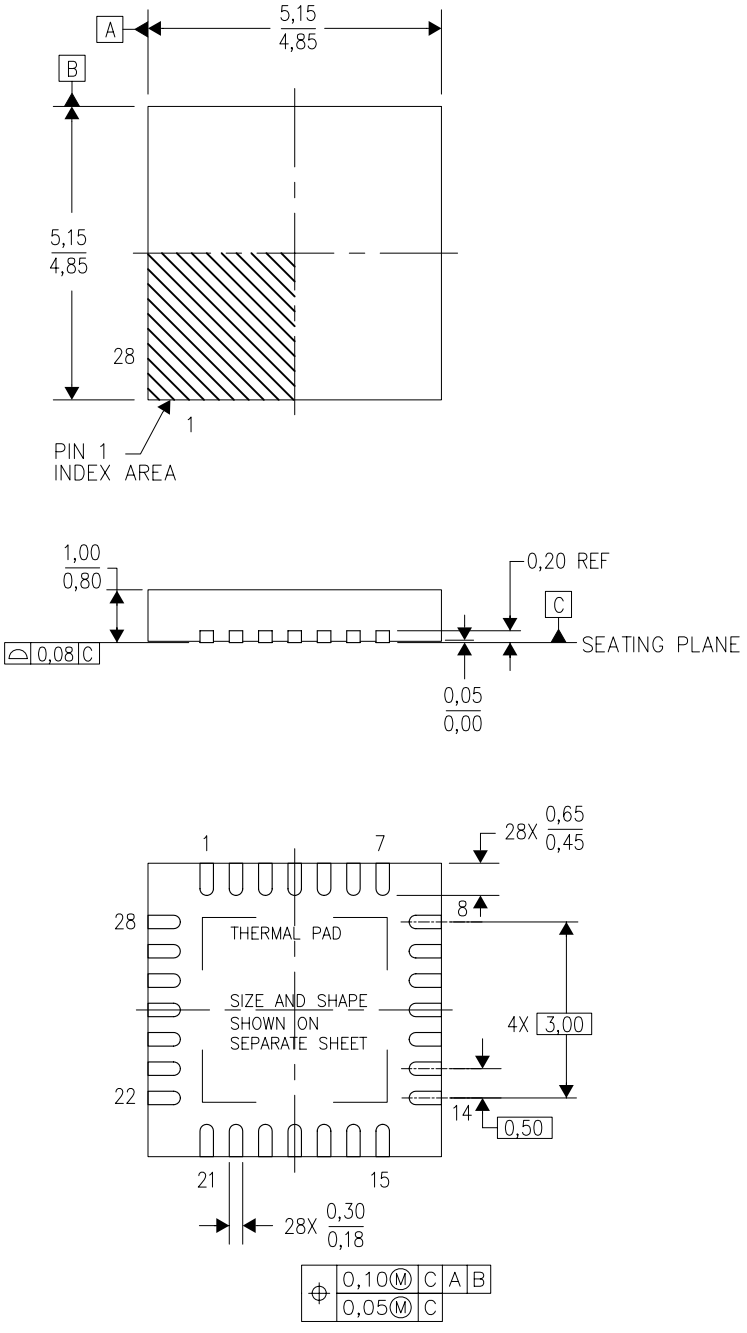
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40490MHRHDR	VQFN	RHD	28	3000	367.0	367.0	35.0
TPS40490MHRHDT	VQFN	RHD	28	250	210.0	185.0	35.0

RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



4204400/F 09/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

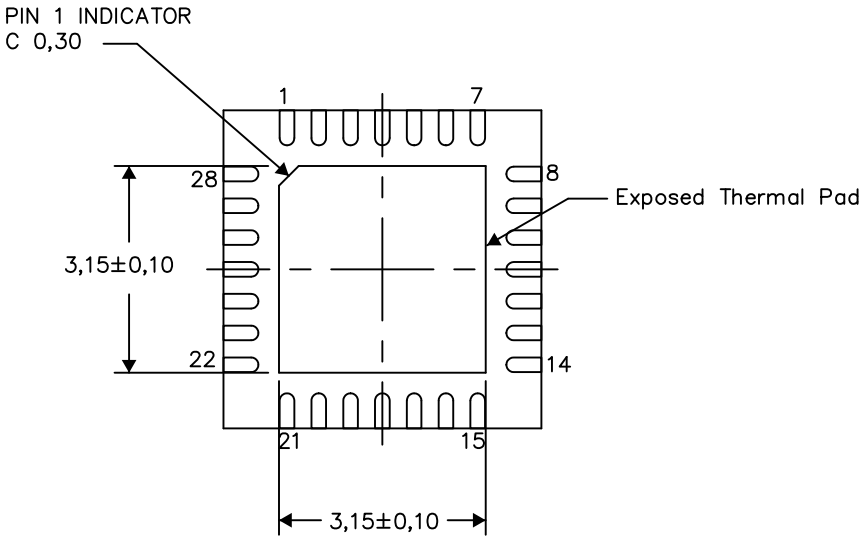
RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



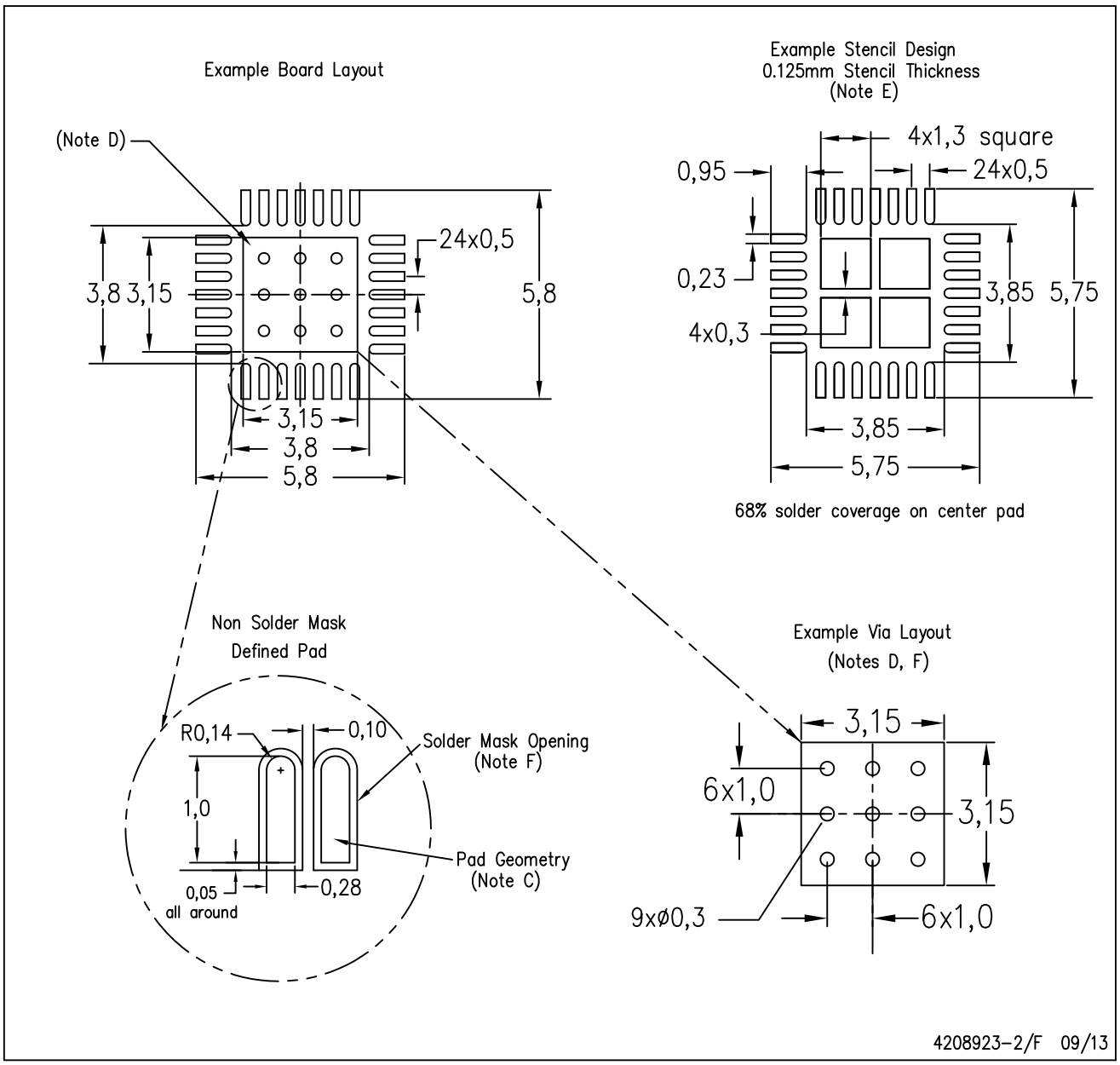
Bottom View

Exposed Thermal Pad Dimensions

4206358–2/J 09/13

NOTE: All linear dimensions are in millimeters

RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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