DS26521DK
Single T1/E1/J1 Transceiver Design Kit

www.maxim-ic.com

GENERAL DESCRIPTION

The DS26521DK is an easy-to-use evaluation kit for the DS26521 T1/E1/J1 single-chip transceiver (SCT). The DS26521DK is intended to be used as a stand-alone system. The board comes complete with a transceiver, transformer, termination resistors, configuration switches, network connectors, microprocessor, and RS-232 connector. The on-board processor and Dallas' ChipView software give point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal and interrupt status, as well as multiple clock and signal routing configurations.

Windows is a registered trademark of Microsoft Corp.

DESIGN KIT CONTENTS

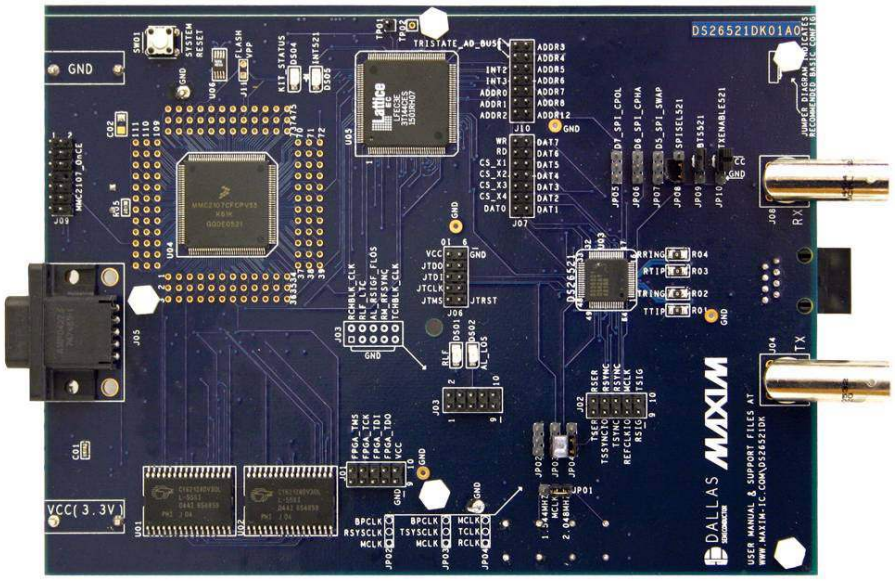
DS26521DK PC Board
CD_ROM Including:
- ChipView Software
- DS26521 Definition Files
- DS26521 Initialization Files
- DS26521DK Data Sheet
- DS26521 Data Sheet
- DS26521 Errata Sheet (if applicable)

FEATURES

- **Demonstrates Key Functions of DS26521 T1/E1/J1 SCT**
- **Includes Transceiver, Transformers, and Termination Passives**
- **BNC Connections for 75Ω E1**
- **RJ48 Connector for 120Ω E1 and 100Ω T1**
- **On-Board Processor and ChipView Software Provide Point-and-Click Access to the DS26521 Register Set**
- **Accessible Address/Data Bus with Tri-State Control to Allow Interface for External Processor**
- **All Equipment-Side Framer Pins are Easily Accessible for External Data Source/Sink**
- **LEDs for Loss-of-Signal and Interrupt Status**
- **Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs**

ORDERING INFORMATION

PART	DESCRIPTION
DS26521DK	Design Kit for DS26521



REV: 021406

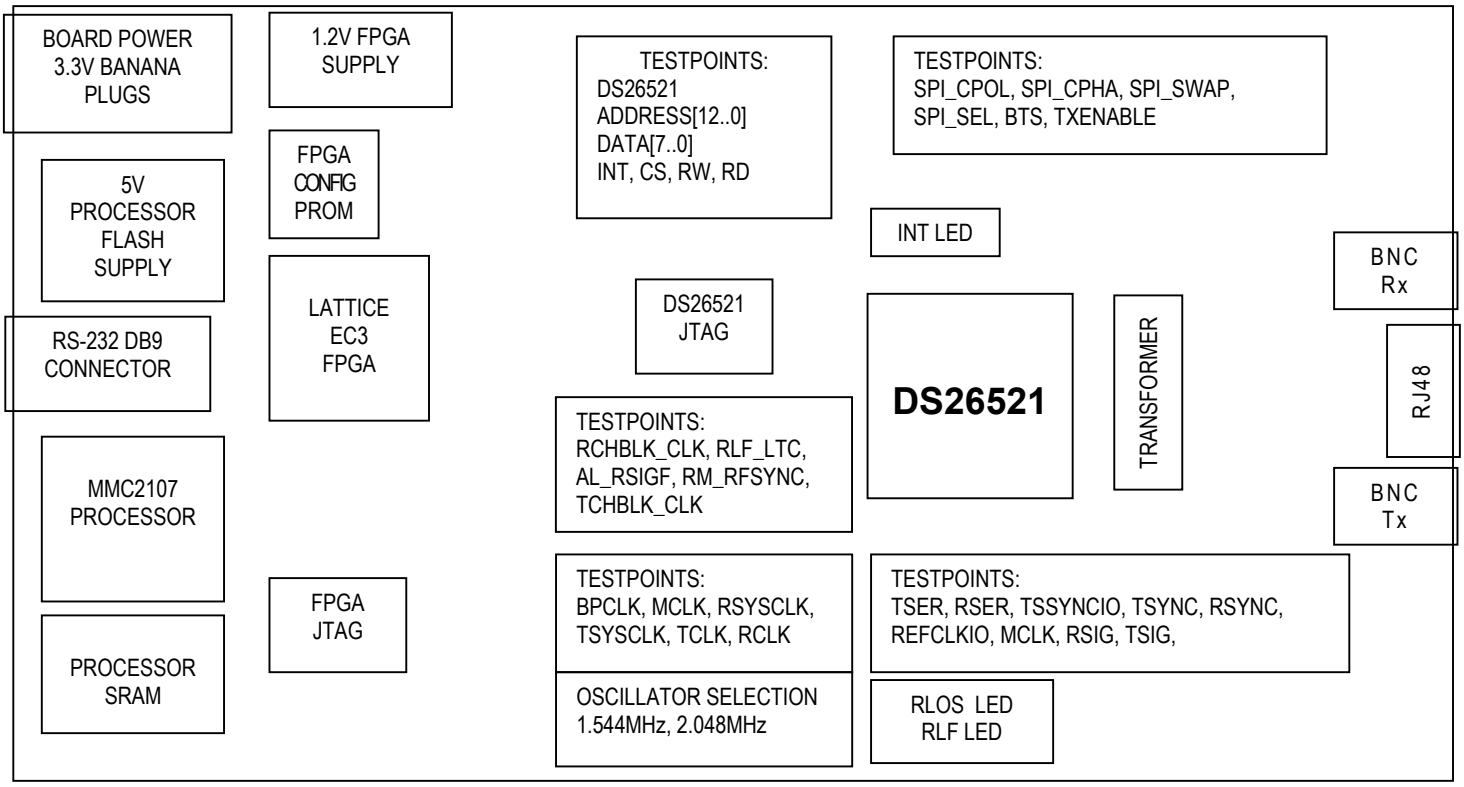
COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER/PART
C01, CB07, CB08, CB10, CB12, CB16, CB18, CB19, CB21, CB23, CB26, CB32, CB39–CB41	15	0.1µF ±10%, 16V ceramic capacitors (0603)	Phycomp 06032R104K7B20D
C02	1	1µF ±10%, 16V ceramic capacitor (1206)	Panasonic ECJ-3YB1C105K
CB01, CB02, CB05, CB06, CB11, CB14, CB20, CB28, CB31, CB34, CB36, CB37	12	10µF ±20%, 10V ceramic capacitors (1206)	Panasonic ECJ-3YB1A106M
CB03, CB04, CB13, CB17, CB24, CB25, CB29, CB38	8	4.7µF, 6.3V multilayer ceramic capacitors (0603)	Digi-Key ECJ-1VB0J475M
CB09	1	560pF ±5%, 50V ceramic capacitor (1206)	Digi-Key 478-1489-2-ND
CB15, CB22, CB27, CB33, CB35	5	0.1µF ±20%, 16V X7R ceramic capacitors (0603)	Arrow 0603YC104MAT2
CB30	1	470µF ±20%, 6.3V tantalum capacitor (D case)	Digi-Key 399-3002-1-ND
DB01	1	1A 40V Schottky diode	International Rectifier 10BQ040
DS01, DS02, DS05	3	Red LEDs, SMD	Panasonic LN1251C
DS04	1	Green LED, SMD	Panasonic LN1351C
GND_TP01–GND_TP06	6	Standard ground clips	Keystone 4954
H1–H5, H10	6	Kit, 4-40 hardware, 0.50 nylon standoff and nylon hex-nut	Lab Stock 4-40KIT4
J01–J03, J06	4	10-pin, dual-row, vertical terminal strips	Samtec TSW-105-07-T-D
J04, J08	2	5-pin right-angle BNC connectors	Trompetor UCBJR220
J05	1	DB9 right-angle connector (long case)	AMP 747459-1
J07, J10	2	Nonpopulated 14-pin, dual-row, vertical headers	Samtec NOPOP-HDR-TSW-107-14-T-D
J09	1	100-mil, 2 x 7-position jumper	Lab Stock
J11	1	100-mil, 2-position jumper	Lab Stock
JB01	1	Red banana plug socket, horizontal	Mouser Electronics 164-6219
JB02	1	8-pin single-port RJ48 connector	Molex 15-43-8588
JB03	1	Black banana plug socket, horizontal	Mouser Electronics 164-6218
JP01–JP09, JP10	10	100-mil, 3-position jumpers	Lab Stock
R01–R04, RB47	5	0Ω ±5%, 1/8W resistors (1206)	Panasonic ERJ-8GEYJ0R00V
R05, RB35–RB40, RB45, RB46	9	1.0kΩ ±5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ102V

DESIGNATION	QTY	DESCRIPTION	SUPPLIER/PART
R06, R07, RB06, RB07, RB44, RB54, RB55	7	10kΩ ±5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ103V
RB01–RB05, RB11, RB23–RB26, RB28, RB29	12	30Ω ±5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ300V
RB08, RB09, RB10, RB14–RB22, RB27, RB32, RB33, RB43, RB48	17	10kΩ ±5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ103V
RB12, RB13, RB50	3	330Ω ±5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ331V
RB30, RB31	2	61.9Ω ±1%, 1/10W resistors (0805)	Panasonic ERJ-6ENF61R9V
RB34	1	1.0MΩ ±5%, 1/16W resistor (0603)	Panasonic ERJ-3GEYJ105V
RB41	1	51.1Ω ±1%, 1/10W resistor (0805)	Panasonic ERJ-6ENF51R1V
RB42	1	10kΩ ±1%, 1/10W resistor (0805)	Panasonic ERJ-6ENF1002V
RB51	1	0Ω ±5%, 1/16W resistor (0603)	Panasonic ERJ-3GEY0R00V
RB52	1	330Ω ±5%, 1/16W resistor (0603)	Panasonic ERJ-3GEYJ331V
RB53	1	1.0kΩ ±5%, 1/16W resistor (0603)	Panasonic ERJ-3GEYJ102V
SW01	1	4-pin single-pole switch	Panasonic EVQPAE04M
TB01	1	16-pin SMT transformer	Pulse Engineering TX1099
TP01, TP02	2	Testpoints, one plated hole **DO NOT STUFF**	Lab Stock
U01, U02	2	Cypress SRAM	Lab Stock
U03	1	Single T1/E1/J1 transceiver, 64-pin, 10mm x 10mm LQFP	Dallas Semiconductor DS26521
U04	1	MMC2107 processor	Motorola MMC2107
U05	1	1.2V FPGA 144-pin, 20mm x 20mm TQFP	Lattice LFEC3E-3T144C
U06	1	3V to 5V regulating charge pump	Maxim MAX1686HEUA
UB01	1	Dual RS-232 transceivers with 3.3V/5V internal capacitors	MAXIM NA
UB02	1	Microprocessor voltage monitor, 2.93V reset, 4-pin SOT143	Maxim MAX811SEUS-T
UB04	1	SPI serial EEPROM, 2M, 2.7V to 3.6V, 8-pin SO	Atmel AT25F2048N-10SU-2.7
UB05	1	LDO regulator with reset, 1.20V output, 300mA, 6-pin SOT23	Maxim MAX1963EZT120-T
YB01	1	Oscillator, crystal clock 3.3V, 1.544MHz	SaRonix NTH039A3-1.5440

DESIGNATION	QTY	DESCRIPTION	SUPPLIER/PART
YB02	1	Oscillator, crystal clock 3.3V, 2.048MHz	SaRonix NTH039A3-2.0480
XB01	1	8.0MHz low-profile crystal	PEI Sales Inc. EC1-8.000M

BOARD FLOORPLAN



PC BOARD ERRATA

DS26521DK01A0 10/10/2005:
There is no errata for the DS26521DK01A0 design.

DS26521DK02A0 11/22/2005:
There is no errata for the DS26521DK02A0 design.

BASIC OPERATION

This design kit relies upon several supporting files, which are available for downloading on our website at www.maxim-ic.com/DS26521DK QuickView page.

Hardware Configuration

- Supply 3.3V to the banana-plug receptacles marked GND and VCC_3.3V.
- Install the following jumpers (detailed in Table 2):
  - JP01—Connect MCLK to 2.048MHz (for both T1 and E1).
  - Connect JP02 MCLK to RSYSCLK, JP03 MCLK to TSYSCLK, JP04 TCLK to RCLK.
  - JP08 SPI_SEL to GND, JP09 BTS to VCC, TXENABLE to VCC.
- From the **Programs** menu, launch the host application named *ChipView.exe*. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select **Programs** → **ChipView** → **ChipView**.

General:

- Upon power-up, the RLF and AL_LOS LEDs (red) will be lit, and the INT LED (red) will not be lit. The board will draw approximately 200mA at power-up.

Quick Setup (Register View)

- The PC will load ChipView, offering a choice among DEMO MODE, REGISTER VIEW, and TERMINAL MODE. Select REGISTER VIEW.
- The program will request a definition file. Navigate to the .def files in the T1 or E1 folder, then select the file named *DS26521_GLOBAL_T1.def* (T1 mode) or *DS26521_GLOBAL_E1.def* (E1 mode). Note: Through the "links" section this will also load the LIU def file and framer def file.
- The *Register View Screen* will appear, showing the register names, acronyms, and values for the DS26521.
- Predefined register settings for several functions are available as initialization files.
  - .ini files are loaded by selecting the menu File→Reg Ini File→Load Ini File.
  - Load the .ini file *Load_T1_LBO0_0_133_impMatchOn.ini* (T1 mode) or *Load_E1_75_impMatchOn.ini* (E1 mode).
  - After loading the .ini file, the following may be observed:
    - The DS26521 begins transmitting AIS with impedance match.
    - The AL_LOS LEDs extinguishes upon external loopback.

Miscellaneous:

- The DS26521 uses three register definition files. All three files are loaded when the *DS26521_GLOBAL*.def* file is loaded. Individual files are selected from the **Def File Selection** menu in ChipView.

ADDRESS MAP

The on-board microcontroller is configured to start the user address space at 0x81000000. All offsets given below are relative to the beginning of the user address space.

Table 1. Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0087	FPGA	Board Identification and FPGA Test Registers
0X1000 to 0X2FFF	DS26521	DS26521 Framer, LIU, and BERT Registers

TESTPOINTS AND CONNECTORS

The DS26521DK has several connectors, testpoints, oscillators, and jumpers. Table 2 provides a description of these signals, given in order of appearance on the PC board, from left to right then top to bottom (with the board held so that the RS-232 connector is on the top edge).

Table 2. Main Board PC Board Configuration

SILKSCREEN REFERENCE	FUNCTION	DEFAULT SETTING	SCHEMATIC PAGE	DESCRIPTION
VCC 3.3V (banana plug)	Power supply VDD	3.3V	2	System VDD. Always connected to power supply.
GND (banana plug)	Power supply Ground	GND	2	System Ground. Always connected to power supply.
J05	RS232 Connector	Connected to Host PC	8	Used for Communication with Host PC. Basic setting is 57.6k baud, 8 bits, no stop bit, 1 parity bit (57.6, 8, N, 1).
J09	OnCE BDM Connector	—	8	OnCE Debug Connector for MMC2107 Processor
SW01	System Reset	—	6	System Reset. Connects to all device reset pins.
J11	Flash VPP Jumper	Not Installed	8	Provides Flash Programming Voltage (5V) to Processor
J01	FPGA, JTAG	—	11	JTAG Connector for Lattice EC3 FPGA
TP01, TP02	FPGA, Testpoint	—	11	FPGA Init and Done Pins
J03	DS26521 Testpoints	—	5	Testpoints for DS26521 Pins: RCHBLK_CLK, RLF_LTC, AL_RSIGF, RM_RFSYNC, TCHBLK_CLK
J06	DS26521 JTAG	—-	3	JTAG Connector for DS26521
YB01, YB02 (Bottom side of PC Board)	Oscillators	—	5	Oscillators for 2.048MHz and 1.544MHz
J07, J10	Testpoints	—	10	Testpoints for DS26521 Address/Data Bus and Control Lines
J10.12 + J10.14	Bus Tri-State	Not Jumpered	10	—
JP01	MCLK Selection	Jumpered pins 2+3	5	MCLK Selection: 1.544MHz, 2.048MHz (default)
JP02	RSYSCLK Selection	Jumpered Pins 1+2	5	RSYSCLK Selection: MCLK (default), BPCLK
JP03	TSYSCLK Selection	Jumpered Pins 1+2	5	TSYSCLK Selection: MCLK (default), BPCLK
JP04	TCLK Selection	Jumpered Pins 1.2	5	TCLK Selection: RCLK (default), MCLK
J02	DS26521 Testpoints	—	5	Testpoints for DS26521 Pins: TSER, RSER, TSSYNCIO, TSYNC, RSYNC, REFCLKIO, MCLK, RSIG, TSIG
JP05	SPI_CPOL bias	Not Jumpered	3	SPI_CPOL Selection: Pulldown, Pullup
JP06	SPI_CPHA bias	Not Jumpered	3	SPI_CPHA Selection: Pulldown, Pullup
JP07	SPI_SWAP bias	Not Jumpered	3	SPI_SWAP Selection: Pulldown, Pullup
JP08	SPI_SEL bias	Jumpered Pins 1+2	3	SPI_SEL Selection: Pulldown (default), Pullup
JP09	BTS bias	Jumpered Pins 2+3	3	BTS Selection: Pulldown, Pullup (default)
JP10	TXENABLE bias	Jumpered Pins 2+3	3	TXENABLE Selection: Pulldown, Pullup (default)
J04, J08	Network BNC	—	4	BNC for 75Ω Network Connection
JB02	Network RJ48	—	4	RJ48 Network Connection

DS26521 INFORMATION

For more information about the DS26521, consult the DS26521 data sheet available on our website at www.maxim-ic.com/DS26521. Software downloads are also available for this design kit.

DS26521DK INFORMATION

For more information about the DS26521DK, including software downloads, consult the DS26521DK data sheet available on our website at www.maxim-ic.com/DS26521DK.

TECHNICAL SUPPORT

For additional technical support, please e-mail your questions to telecom.support@dalsemi.com.

SCHEMATICS

The DS26521DK schematics are featured in the following pages.

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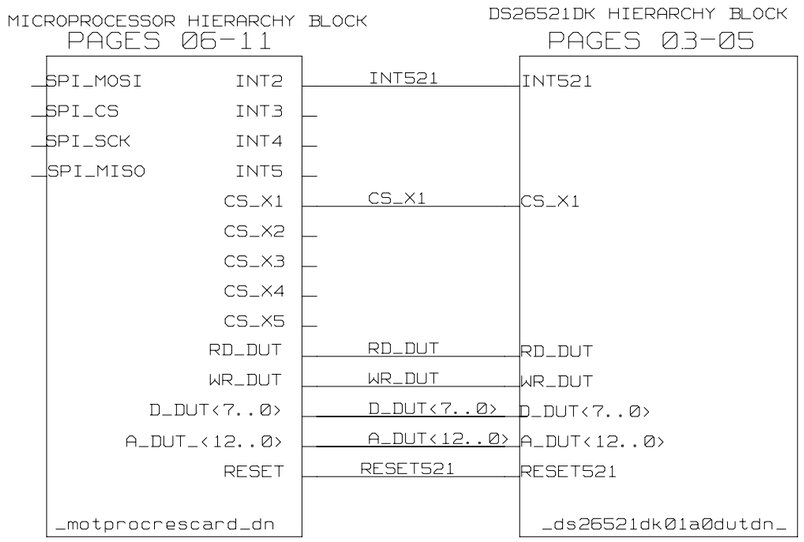


CONTENTS

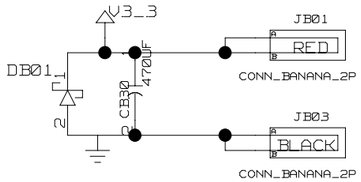
PAGE 01: DS26521 DESIGN KIT AND ENGINEERING EVALUATION TOP LEVEL HIERARCHY BLOCKS
PAGE 02: DECOUPLING / MOUNTING HOLES

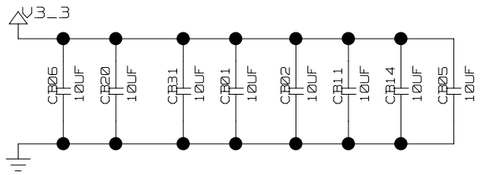
DS26521 DESIGN KIT
PAGES 03-05: DS26521 DEVICE, LINE BUILDOUT AND TESTPOINTS
PAGES 06-11: MICROPROCESSOR AND INTERFACE

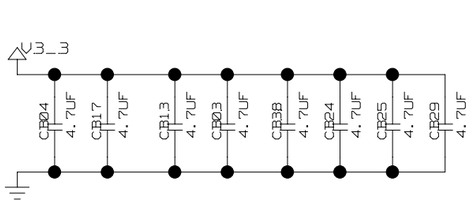
NOTES: EACH HIERARCHY BLOCK IS INDEPENDENT OF THE NEXT.
ONLY SIGNALS WITH IMPORT/OUTPORT CONNECTORS HAVE CONNECTION OUTSIDE THE HIERARCHY BLOCK. THESE SIGNALS APPEAR AS PINS ON THE HIERARCHY BLOCK CONNECTOR

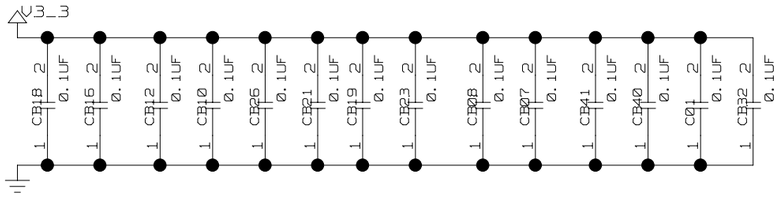
TITLE: DS26521DK02A0 DS26521DK TOP LEVEL	DATE: 10/26/2005
ENGINEER: STEVE SCULLY	PAGE:1/2(BLOCK) 1/11(TOTAL)

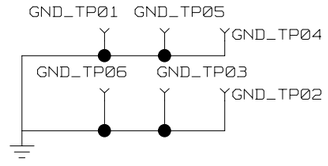
BLOCK NAME: _ds26521topdn_. PARENT BLOCK: <CON_PARENT_NAME>



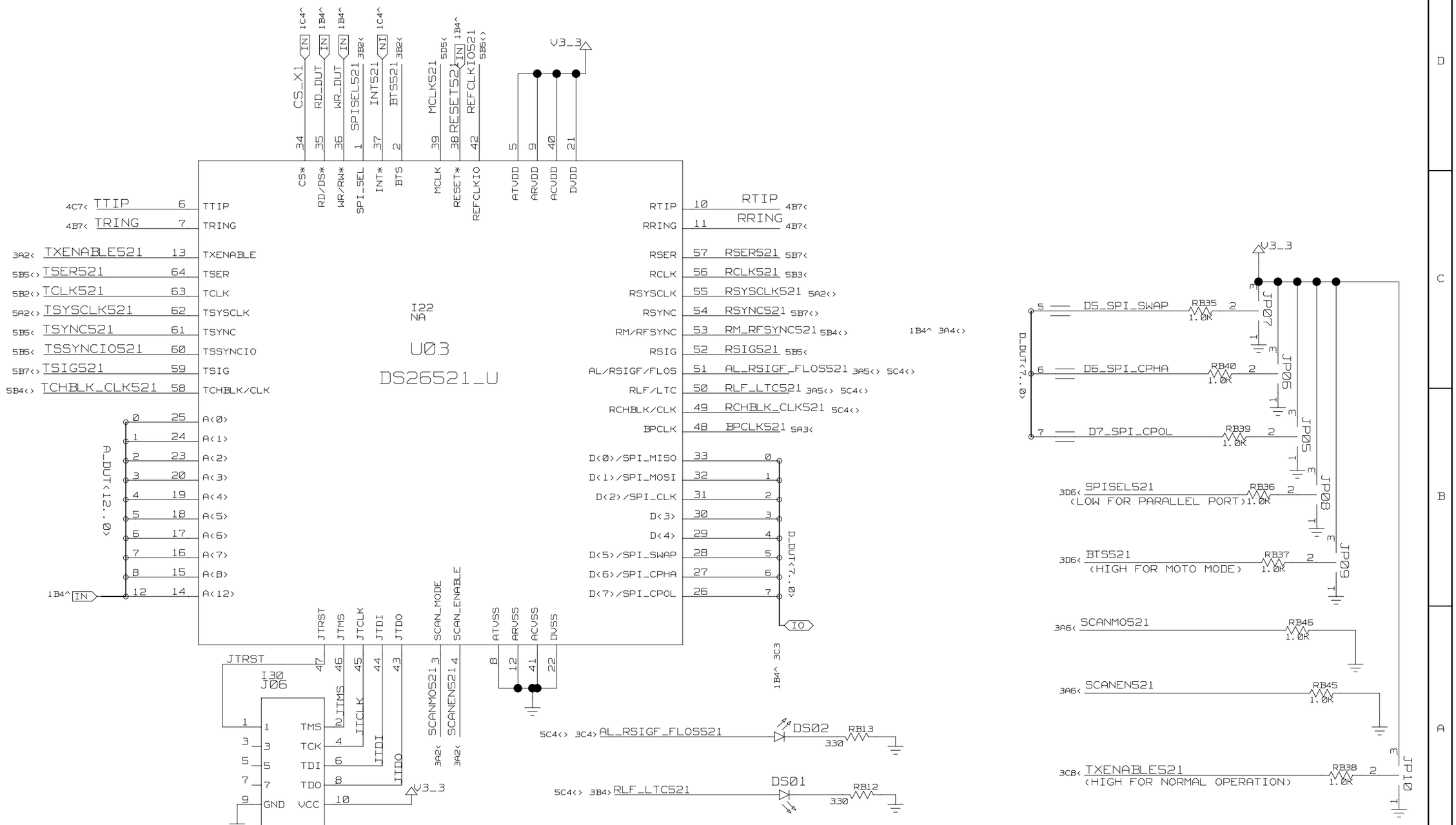








TITLE: DS26521DK02A0	DATE: 10/26/2005
ENGINEER: STEVE SCULLY	PAGE:2/2(BLOCK) 2/11(TOTAL)

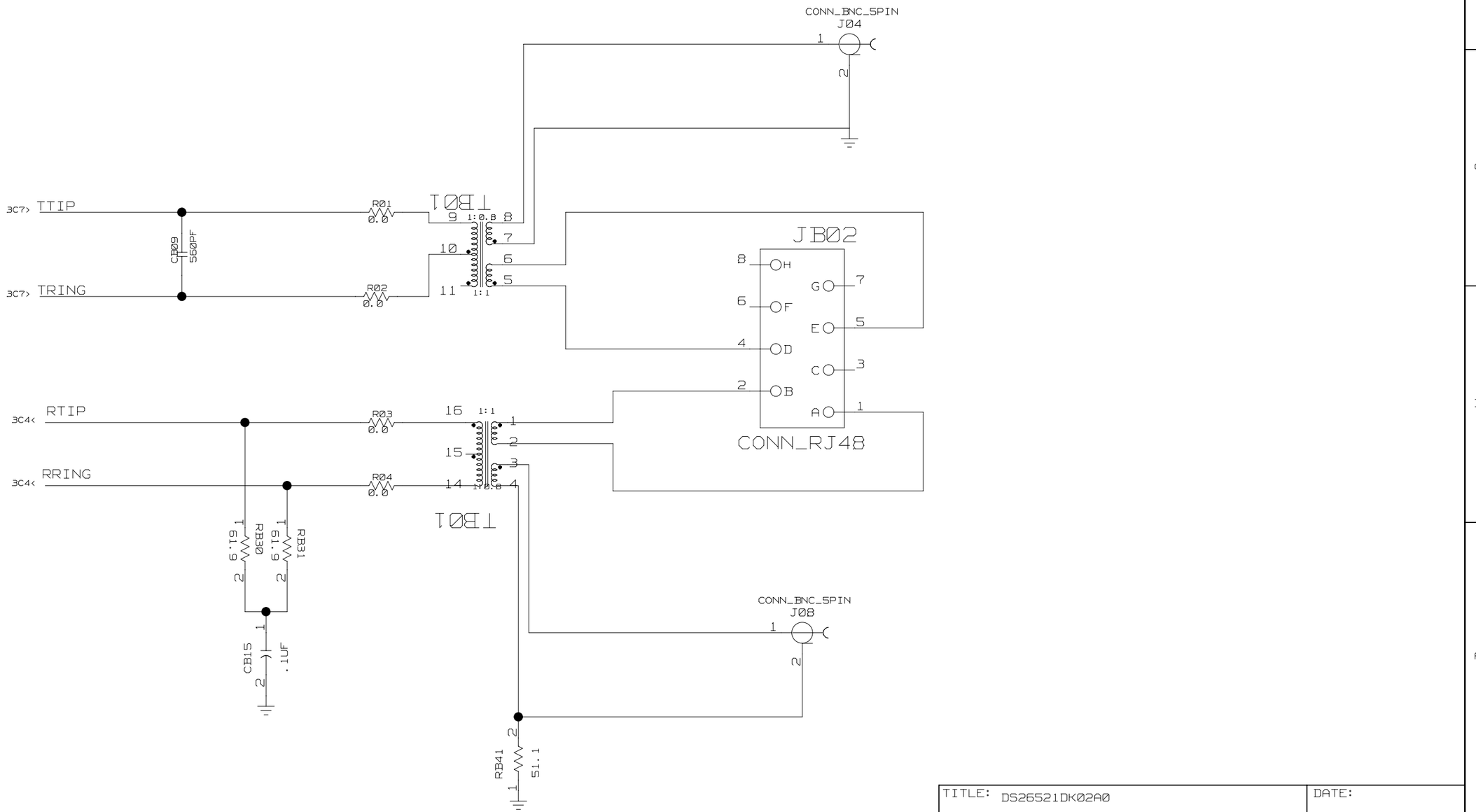


INT_LED AND TESTPOINTS FOR ADDR/DATA/CTRL
ARE IN THE MICRO PROCESSOR BLOCK

BEGINNING OF DS26521DK HIERARCHY BLOCK

TITLE: DS26521DK02A0	DATE: 10/26/2005
ENGINEER: STEVE SCULLY	PAGE:1/3(BLOCK) 3/11(TOTAL)

BLOCK NAME: _ds26521dk01a0dutdn_. PARENT BLOCK: _ds26521topdn_\



TITLE: DS26521DK02A0	DATE: 10/26/2005
ENGINEER: STEVE SCULLY	PAGE:2/3(BLOCK) 4/11(TOTAL)

2.048MHZ_3.3V
YB02
OSC
V3_3
1
1
VCC
8
4
GND
OUT
5
I58
JMP_3m
MCLK521PREBUF
2
JP01
1
RB04
30
MCLK521
3D6<

1.544MHZ_3.3V
YB01
V3_3
OSC
1
1
VCC
8
4
GND
OUT
5

J03
3B4> RCHBLK_CLK521 2 2 1 1
3B4> 3A5<> RLF_LTC521 4 4 3 3
3C4> 3A5<> AL_RSIGF_FLOS521 6 6 5 5
3C4> RM_RFSYNC521 8 8 7 7
3B8> TCHBLK_CLK521 10 10 9 9
CONN_10P

J02
3C4> RSER521 RB23 30 2 2 1 1 TSER521 3C8<
3C4<> RSYNC521 4 4 3 3 RB26 30 TSSYNCIO521 3C8<>
6 6 5 5 RB24 30 TSYNC521 3C8<>
5B3< 5A3< 5D6<> MCLK521PREBUFR RB05 30 8 8 7 7 REFCLKIO521 3D5<>
3C8< TSIG521 10 10 9 9 RB25 30 RSIG521 3C4>
CONN_10P

I56
5B7< 5A3< 5D6<> MCLK521PREBUF RB03 30 JMP_3m
JP04 2 TCLK521 3C8<
3C4> RCLK521 RB11 30 1

5A3< 3B4> BPCLK521 RB28 30 JMP_3m
JP03 2 TSYSCLK521 3C8<
5B7< 5B3< 5A3< 5D6<> MCLK521PREBUFR RB01 30 1

5A3< 3B4> BPCLK521 RB29 30 JMP_3m
JP02 2 RSYSCLK521 3C4<
5B7< 5B3< 5A3< 5D6<> MCLK521PREBUFR RB02 30 1

END OF DS26521DK HIERARCHY BLOCK

TITLE: DS26521DK02A0	DATE: 10/26/2005
ENGINEER: STEVE SCULLY	PAGE:3/3(BLOCK) 5/11(TOTAL)

BLOCK NAME: _ds26521dk01a0dutdn_. PARENT BLOCK: _ds26521topdn_\

MMC2107 CONTROL

MMC2107 PORT

U04

U04 TIM_16H_BL

U04 VSTBY VRH VRL VPP VDDA VDDF VDDH VDDSYN VDD8 VDD7 VDD6 VDD5 VDD4 VDD3 VDD2 VDD1

U04 RW OE* SHS* TA* TEA*

RW 9D5<>
OE 7B4<> 7B7<> 9D5<>
RCON 7D6<
TA
TEA
VRH
FLASH_VPP 8B1<>
RB47 0.0
CB22 .1UF
CB2 10F
VDDSYN
V3_3

INT7* INT5* INT4 INT3* INT2* INT1* INT0* YC0 MOSI MISO XTAL EXTAL TCLK TRST* TMS

USER_LED1 89
USER_LED2 84
INT3 82
INT4 79
RUN_KIT_USR 75
KIT_STATUS 72
INT2 71
YC0 80
SPI_MOSI 90 OUT
SPI_MISO 91 IN
XTAL 124
OSC_MCU 125
ONCE_TCLK 130
ONCE_TRST_B 142
ONCE_TMS 138

INT7* 89
INT5* 84
INT4 82
INT3* 79
INT2* 75
INT1* 72
INT0* 71
YC0 80
MOSI 90
MISO 91
XTAL 124
EXTAL 125
TCLK 130
TRST* 142
TMS 138

TIM_16H_BL 88
EB3* 96 EB3
EB2* 98 EB2
EB1* 100 EB1 7B4<> 9D4<>
EB0* 101 EB0 7B7<> 9D5<>
PQB3 104 PQB3
PQB2 105 PQB2
PQB1 106 PQB1
PQB0 107 PQB0
PQA4 108 PQA4
PQA3 109 PQA3
PQA1 110 PQA1
PQA0 111 PQA0
TDI 133 ONCE_TDI 8D3<>
TDO 135 21107_TDO 8D3<>

ICOC23 52 ICOC23
ICOC22 53 ICOC22
ICOC21 54 ICOC21
ICOC20 55 ICOC20
ICOC13 56 ICOC13
ICOC12 57 ICOC12
ICOC11 58 ICOC11
ICOC10 61 ICOC10
GND TEST 63 TEST
SCI2_OUT 66 TXD2
SCI2_IN 68 RXD2
8B8< SCI1_OUT 69 TXD1
8B8> SCI1_IN 70 RXD1

CSE1 60 CSE1
CSE0 62 CSE0
TC2 67 TC2
TC1 78 TC1
CS3* 81 CS3
CS2* 83 CS2 9D5<>
CS1* 85 CS1 9D5<>
CS0* 86 CS0 7B3<> 7B7<> 9D5<>
RESET* 118 PROC_RESET 8C3<> 6A4<
CLKOUT 128 CPUCLK_OUT 9C8<>
RSTOUT* 120 PROC_RESET_OUT
SCK 93 SPI_SCK OUT
DE* 143 ONCE_DE_B 8C2<>
SS* 94 SPI_CS OUT

D31 31 144
D30 30 1
D29 29 2
D28 28 3
D27 27 4
D26 26 5
D25 25 7
D24 24 10
D23 23 12
D22 22 15
D21 21 16
D20 20 17
D19 19 20
D18 18 21
D17 17 22
D16 16 25
D15 15 27
D14 14 30
D13 13 31
D12 12 34
D11 11 35

D10 10 36
D9 9 37
D8 8 38
D7 7 39
D6 6 40
D5 5 41
D4 4 42
D3 3 43
D2 2 46
D1 1 48
D0 0 51

VSSA 114
VSSF 73
VSSSYN 126
VSS8 140
VSS7 127
VSS6 76
VSS5 64
VSS4 44
VSS3 32
VSS2 18
VSS1 8

PD<31..0> 7A2> 7A6> 7C7< 7D7< 9D6

A22 116 22
A21 117 21
A20 119 20
A19 121 19
A18 122 18
A17 131 17
A16 132 16
A15 134 15
A14 136 14
A13 137 13
A12 139 12
A11 6 11
A10 11 10
A9 13 9
A8 14 8
A7 23 7
A6 24 6
A5 26 5
A4 28 4
A3 29 3
A2 47 2
A1 49 1
A0 50 0

PA<22..0>

2.93V

UB02

MAX811_U

SW01

MR* 3
GND 1
VCC 4 V3_3
RESET* 2 RESET 9C8<> 10C2> 11B4< 1B5^
R05 1.0K PROC_RESET 6B5<> 8C3<>

10C3< 10B6<> INT3
10C5< 10C3< INT4

BEGINNING OF PROCESSOR HIERARCHY BLOCK

TITLE: DS26521DK02A0	DATE: 10/26/2005
ENGINEER: STEVE SCULLY	PAGE: 1/6<BLOCK> 6/11<TOTAL>

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ds26521topdn_\

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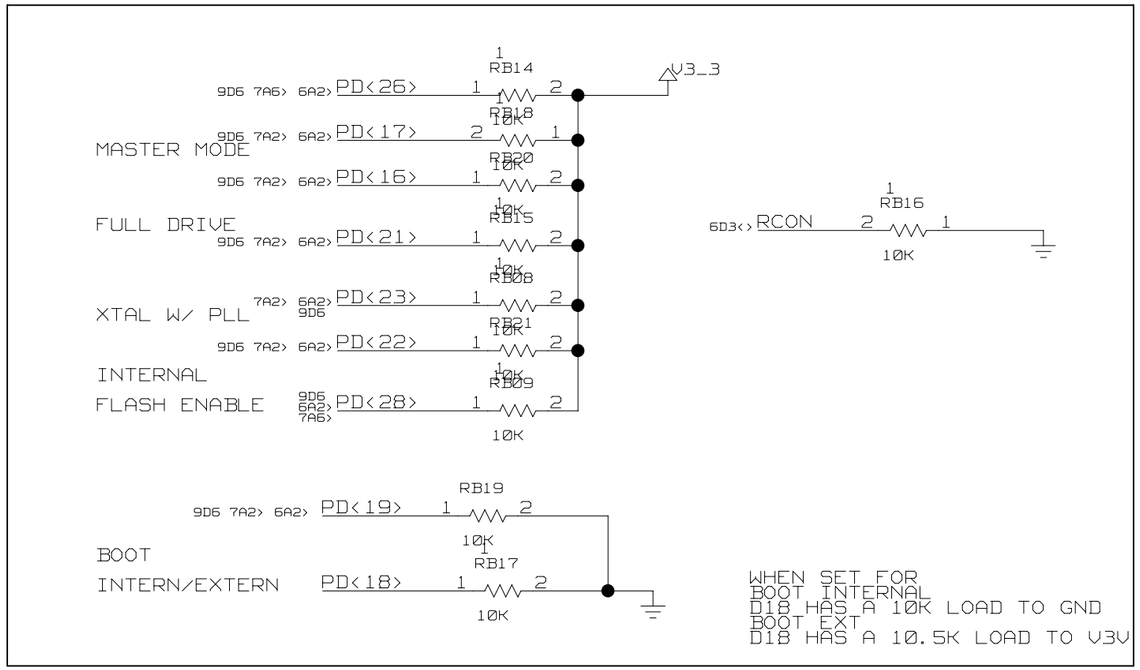
RESET CONFIGURATION



TITLE: DS26521DK02A0	DATE: 10/26/2005
ENGINEER: STEVE SCULLY	PAGE:2/6(BLOCK) 7/11(TOTAL)

XB01
8.0MHZ
RB34 1.0M
PLACE PADS FOR CAP
BUT DO NOT POPULATE
OSC_MCU 6A6<>
XTAL 6A7<>

V3_3
RB32 10K
RB33 10K
J09
CON14P
CON14P
6D6<> ONCE_TDI 1
6D6<> 2107_TDO 3
6A6<> ONCE_TCLK 5
7
8 ALIGN KEY
6A4< 6B5<> PROC_RESET 9
V3_3
10 ONCE_TMS 6A6<>
11 6B5<> 12 ONCE_DE_B
13 6A6<> 14 ONCE_TRST_B
RB43 10K

V3_3
UB01
MAX323.3E
1 R2OUT
2 INVALID*
3 T2IN
6B8<> SCI1_OUT 4 T1IN
5 FORCEON
6B8<> SCI1_IN 6 R1OUT
8A8<> PRT1_OUT 7 T1OUT
8A8<> PRT1_IN 8 R1IN
9 VCC
10 FORCEOFF*
R2IN 20
T2OUT 19
GND 18
V- 17
C2- 16
C2+ 15
C1- 14
C1+ 13
V+2 12
V+1 11

1 CB39 2
0.1UF
6 CXN
MAX1686_U
U06
7 CXP
V3_3
3 IN
2 SHDN
1 V3/5*
OUT 8
GND 4
PGND 5
CB36 10UF
V3_3
RB53 1.0K
J11
FLASH_VPP
6D3<

V3_3
RB10 10K
RB22 10K
RB27 10K
J05
PRT1_OUT 8B8>
PRT1_IN 8B8<
1 A
2 B
3 C
4 D
5 E
F 6
G 7
H 8
J 9
CONN_DB9P

DS04
RB52 330
GREEN
6A7<> KIT_STATUS

TITLE: DS26521DK02A0	DATE: 10/26/2005
ENGINEER: STEVE SCULLY	PAGE:3/6(BLOCK) 8/11(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ds26521topdn_\

PD<31..16>

U05

LFEC_T144_U

I/O PORT

97_IO

BANK 0 BANK 1 BANK 2 BANK 3 BANK 4 BANK 5 BANK 6 BANK 7

PA<16..0>

RESET

CPUCLK_OUT

A_DUT_<12..0>

D_DUT<7..0>

CS_X1 CS_X2 CS_X3 CS_X4 CS_X5

DS05

INT2 INT_LED ALE_DUT WR_DUT RD_DUT

V3_3 RB50 330

MEM_SO MEM_SI MEM_CS MEM_SCK

TRISTATE_AD_BUS

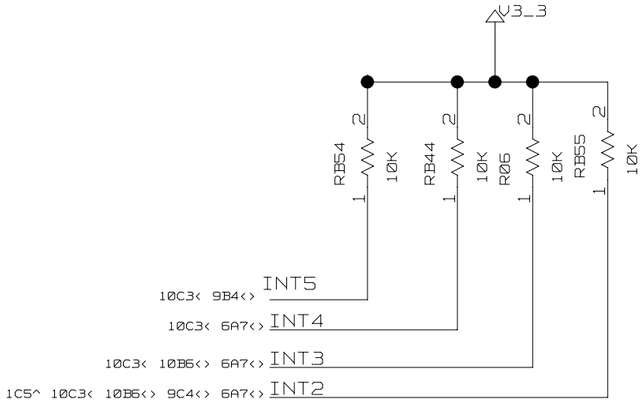
MEM_SCK MUST BE AT PIN77 FOR TQFP144

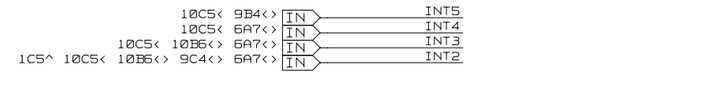
USERFPGA2 INT5

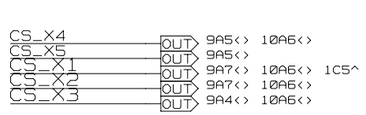
PLL INPUT

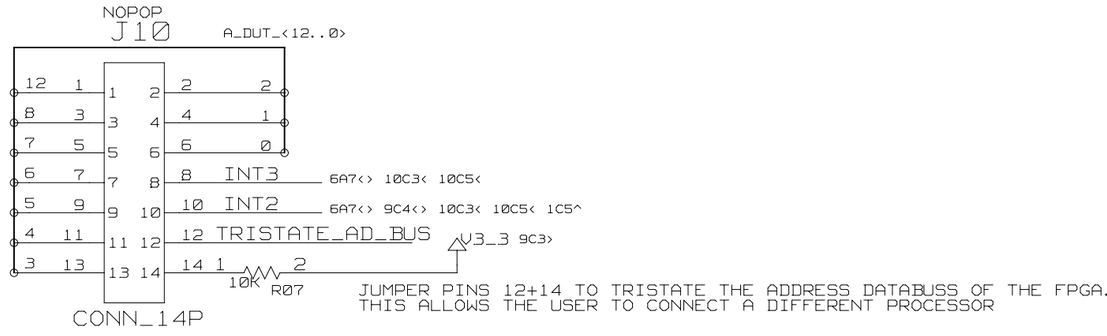
TITLE: DS26521DK02A0	DATE: 10/26/2005
ENGINEER: STEVE SCULLY	PAGE:4/6(BLOCK) 9/11(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ds26521topdn_\

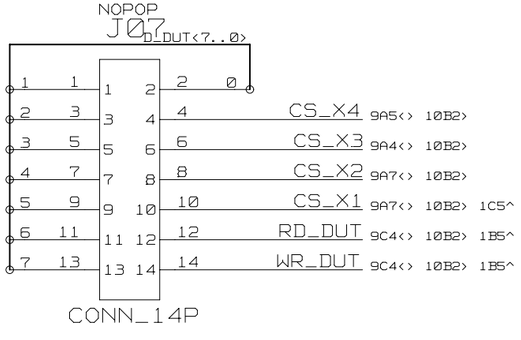








JUMPER PINS 12+14 TO TRISTATE THE ADDRESS DATABUSS OF THE FPGA.
THIS ALLOWS THE USER TO CONNECT A DIFFERENT PROCESSOR



TITLE: DS26521DK02A0	DATE: 10/26/2005
ENGINEER: STEVE SCULLY	PAGE:5/6(BLOCK) 10/11(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ds26521topdn_\

I24
J01
CONN_10P
L_TMS 11C4<
L_TCK 11C4<
L_TDI 11C4<
L_TDO 11C4<
V3_3
RB07 10K
RB06 10K

I25
2.7V

UB04
AT25160A_U
9C4<> MEM_SI
9C4<> MEM_SO
9B3< 11B1<> MEM_SCK
9B4<> MEM_CS
V3_3

I28
UB05
MAX1963
V3_3
V1_2
CB27 .1UF
CB33 .1UF
CB35 .1UF
CB37 10UF
CB34 10UF
CB28 10UF

I10
97_IO
U05
LFEC_T144_U
CONTROL
V3_3
VCCIO0A 136
VCCIO0B 143
VCCIO1A 110
VCCIO1B 125
VCCIO2 108
VCCIO3A 73
VCCIO3B 84
VCCIO4A 55
VCCIO4B 71
VCCIO5A 38
VCCIO5B 44
VCCIO6A 24
VCCIO6B 36
VCCIO7 1
11D6<> L_TCK 14 TCK
11D6<> L_TDI 16 TDI
11D6<> L_TDO 18 TDO
11D6<> L_TMS 17 TMS
89 CFG2
90 CFG1
91 CFG0 ALL LOW FOR SPI3 MODE
1B5^ 10C2> 9C8<> 6A4<> RESET 93 PROGRAM*
VCC1 13 V1_2 11A6<
VCC2 92
VCC3 99
VCCJ 19 V3_3
VCCAUX1 54
VCCAUX2 126
NEEDS 10K,1% RESISTOR PLACE CLOSE TO PIN 11B8< 9B3<
XRES 10 RB42 10K
CCLK 94 MEM_SCK
INIT* 95 I5 YTP02
DONE 97 I6 YTP01
RB48 10K
GND0 128
GND1 117
GND2/GND1 109
GND3A/GND4 72
GND3B 80
GND4 63
GND5 52
GND6A 28
GND6B/GND5 37
GND7/GND0 144
GND8 15
GND9 96
GND10 98
NC1 11
NC2 12

END OF PROCESSOR HIERARCHY BLOCK

TITLE: DS26521DK02A0	DATE: 10/26/2005
ENGINEER: STEVE SCULLY	PAGE: 6/6(BLOCK) 11/11(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ds26521topdn_\