

**FEATURES:**

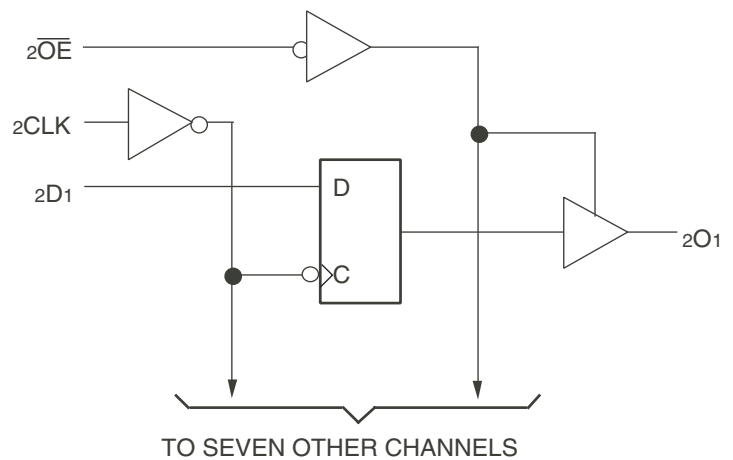
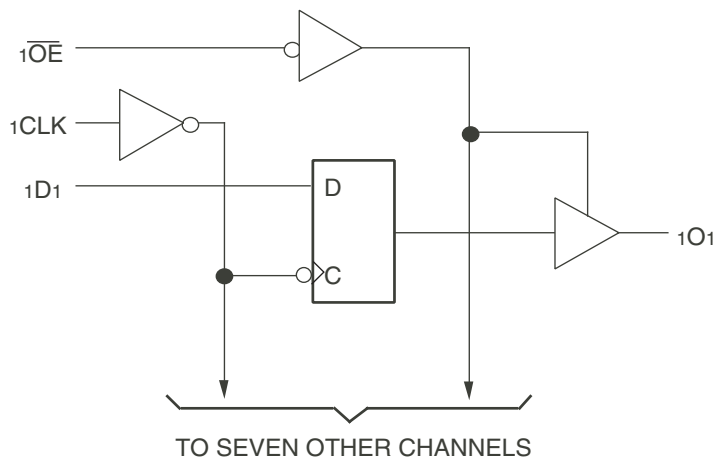
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- Low input and output leakage  $\leq 1\mu A$  (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 5V \pm 10\%$
- High drive outputs (-32mA IOH, 64mA IOL)
- Power off disable outputs permit "live insertion"
- Typical VOLP (Output Ground Bounce) < 1.0V at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$
- Available in the following packages:
  - Industrial: SSOP, TSSOP

**DESCRIPTION:**

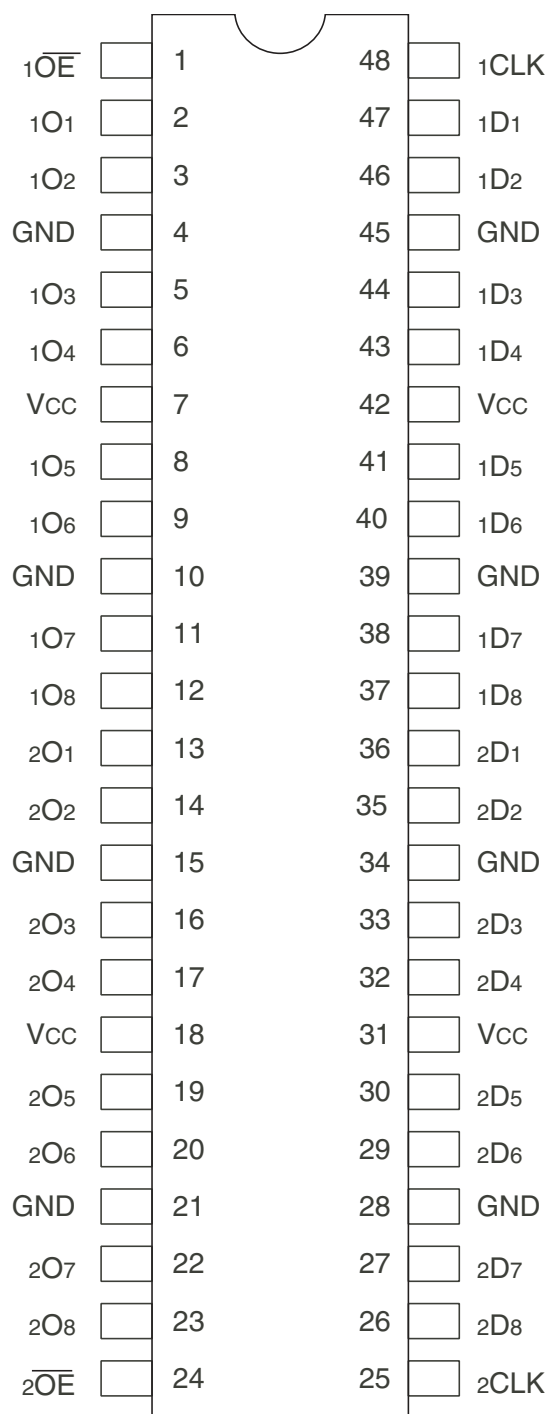
The FCT16374T 16-bit edge-triggered D-type register is built using advanced dual metal CMOS technology. These high-speed, low-power registers are ideal for use as buffer registers for data synchronization and storage. The Output Enable ( $\overline{xOE}$ ) and clock (xCLK) controls are organized to operate each device as two 8-bit registers or one 16-bit register with common clock. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT16374T is ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

**FUNCTIONAL BLOCK DIAGRAM**



## PIN CONFIGURATION



TOP VIEW

Package Type	Package Code	Order Code
TSSOP	PAG48	PAG
SSOP	PVG48	PVG

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to 7	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXX Output and I/O terminals.
- Outputs and I/O terminals for FCT162XXX.

## CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6	pF
COUT	Output Capacitance	VOUT = 0V	3.5	8	pF

### NOTE:

- This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xCLK	Clock Inputs
xOx	3-State Outputs
xOE	3-State Output Enable Input (Active LOW)

## FUNCTION TABLE<sup>(1)</sup>

Function	Inputs			Outputs
	xDx	xCLK	xOE	xOx
Z	X	L	H	Z
	X	H	H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

### NOTE:

- H = HIGH voltage level  
L = LOW voltage level  
X = Don't care  
Z = High-impedance  
↑ = LOW-to-HIGH transition

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current (Input pins) <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_i = V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
	Input HIGH Current (I/O pins) <sup>(5)</sup>		—	—	$\pm 1$		
$I_{IL}$	Input LOW Current (Input pins) <sup>(5)</sup>		$V_i = \text{GND}$	—	—	$\pm 1$	
	Input LOW Current (I/O pins) <sup>(5)</sup>		—	—	$\pm 1$		
$I_{OZH}$	High Impedance Output Current (3-State Output pins) <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_o = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$			$V_o = 0.5\text{V}$	—	—	$\pm 1$	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_o = \text{GND}^{(3)}$		-80	-140	-250	mA
$V_H$	Input Hysteresis	—		—	100	—	mV
$I_{CCL}$	Quiescent Power Supply Current	$V_{CC} = \text{Max}$		—	5	500	$\mu\text{A}$
$I_{CCH}$		$V_{IN} = \text{GND}$ or $V_{CC}$					
$I_{CCZ}$							

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$I_o$	Output Drive Current	$V_{CC} = \text{Max.}, V_o = 2.5\text{V}^{(3)}$		-50	—	-180	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$	$I_{OH} = -3\text{mA}$	2.5	3.5	—	V
			$I_{OH} = -15\text{mA IND}$	2.4	3.5	—	V
			$I_{OH} = -32\text{mA IND}$	2	3	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$	$I_{OL} = 64\text{mA IND}$	—	0.2	0.55	V
$I_{OFF}$	Input/Output Power Off Leakage <sup>(5)</sup>	$V_{CC} = 0\text{V}, V_{IN} = \text{or } V_o \leq 4.5\text{V}$		—	—	$\pm 1$	$\mu\text{A}$

### NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- This test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^{\circ}\text{C}$ .

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max. V <sub>IN</sub> = 3.4V <sup>(3)</sup>		—	0.5	1.5	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(4)</sup>	V <sub>CC</sub> = Max. Outputs Open $\overline{xOE}$ = GND One Input Toggling 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	60	100	$\mu A/$ MHz
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	V <sub>CC</sub> = Max. Outputs Open f <sub>CP</sub> = 10MHz 50% Duty Cycle $\overline{xOE}$ = GND fi = 5MHz 50% Duty Cycle One Bit Toggling	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	0.6	1.5	mA
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	1.1	3	
		V <sub>CC</sub> = Max. Outputs Open f <sub>CP</sub> = 10MHz 50% Duty Cycle $\overline{xOE}$ = GND Sixteen Bits Toggling fi = 2.5MHz 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	3	5.5 <sup>(5)</sup>	
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	7.5	19 <sup>(5)</sup>	

### NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient.
- Per TTL driven input (V<sub>IN</sub> = 3.4V). All other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
- I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$   
 I<sub>CC</sub> = Quiescent Current (I<sub>CC1</sub>, I<sub>CC2</sub> and I<sub>CCZ</sub>)  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)  
 D<sub>H</sub> = Duty Cycle for TTL Inputs High  
 N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 N<sub>CP</sub> = Number of Clock Inputs at f<sub>CP</sub>  
 f<sub>i</sub> = Input Frequency  
 N<sub>i</sub> = Number of Inputs at f<sub>i</sub>

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

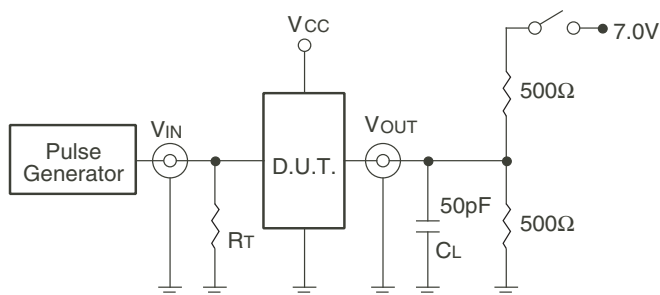
Symbol	Parameter	Condition <sup>(2)</sup>	74FCT16374AT		Unit
			Ind.		
			Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay xCLK to xOx	CL = 50pF RL = 500Ω	2	6.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time		1.5	6.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time		1.5	5.5	ns
t <sub>SU</sub>	Set-up Time HIGH or LOW, xDx to xCLK		2	—	ns
t <sub>H</sub>	Hold Time HIGH or LOW, xDx to xCLK		1.5	—	ns
t <sub>w</sub>	xCLK Pulse Width HIGH or LOW		5	—	ns
t <sub>SK(o)</sub>	Output Skew <sup>(3)</sup>		—	0.5	ns

Symbol	Parameter	Condition <sup>(2)</sup>	74FCT16374CT		74FCT16374ET		Unit
			Ind.		Ind.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay xCLK to xOx	CL = 50pF RL = 500Ω	2	5.2	1.5	3.7	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time		1.5	5.5	1.5	4.4	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time		1.5	5	1.5	3.6	ns
t <sub>SU</sub>	Set-up Time HIGH or LOW, xDx to xCLK		2	—	1.5	—	ns
t <sub>H</sub>	Hold Time HIGH or LOW, xDx to xCLK		1.5	—	0	—	ns
t <sub>w</sub>	xCLK Pulse Width HIGH or LOW		5	—	3 <sup>(4)</sup>	—	ns
t <sub>SK(o)</sub>	Output Skew <sup>(3)</sup>		—	0.5	—	0.5	ns

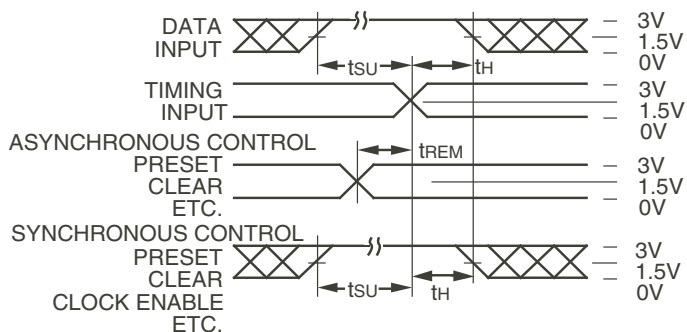
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

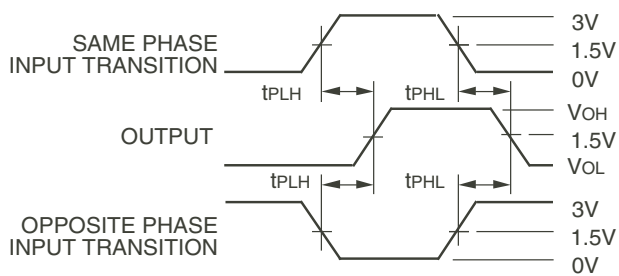
## TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-up, Hold, and Release Times



Propagation Delay

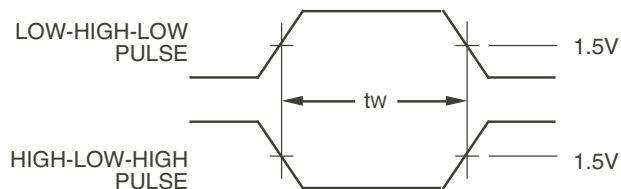
## SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

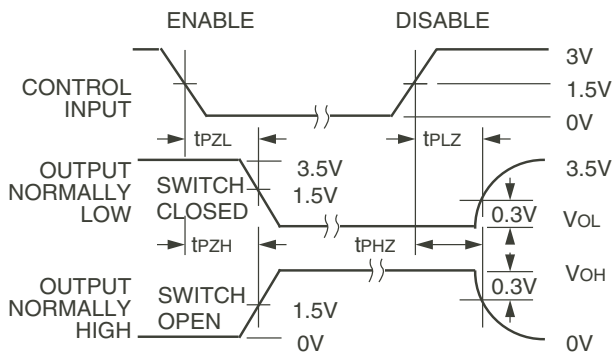
### DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

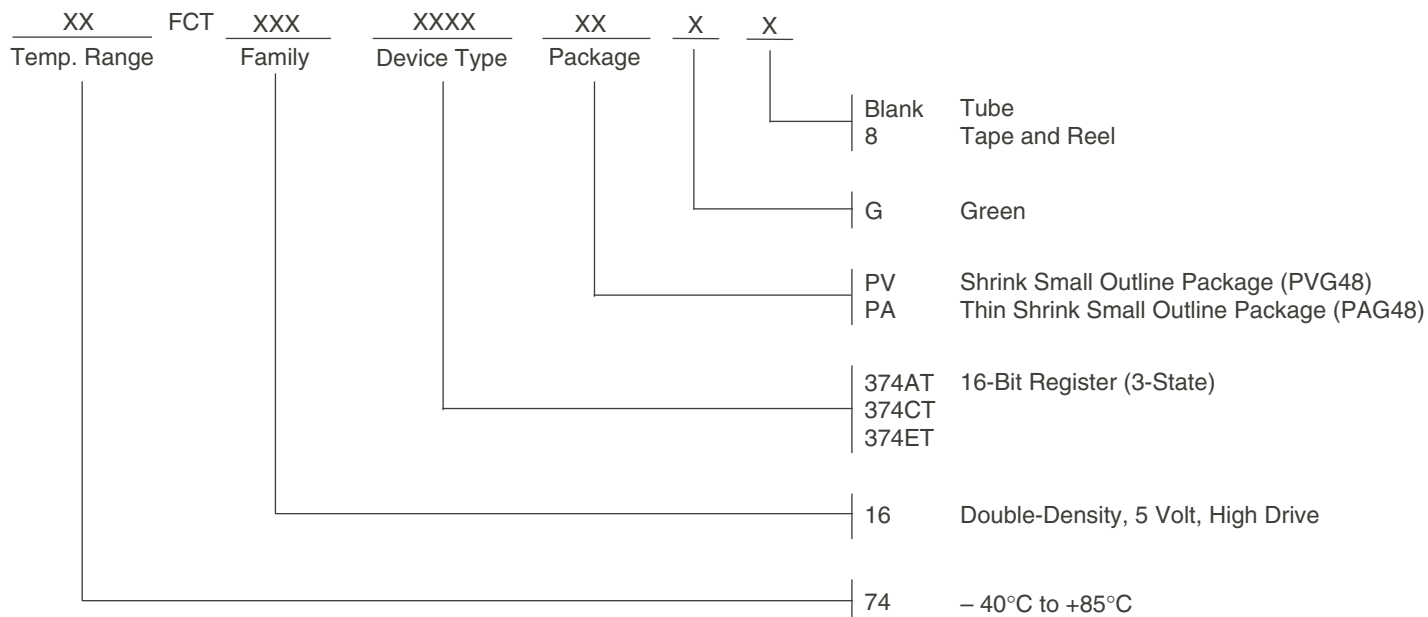


Enable and Disable Times

### NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_f \leq 2.5\text{ns}$ .

## ORDERING INFORMATION



## Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
A	74FCT16374ATPAG	PAG48	TSSOP	I
	74FCT16374ATPAG8	PAG48	TSSOP	I
	74FCT16374ATPVG	PVG48	SSOP	I
	74FCT16374ATPVG8	PVG48	SSOP	I
C	74FCT16374CTPAG	PAG48	TSSOP	I
	74FCT16374CTPAG8	PAG48	TSSOP	I
	74FCT16374CTPVG	PVG48	SSOP	I
	74FCT16374CTPVG8	PVG48	SSOP	I
E	74FCT16374ETPAG	PAG48	TSSOP	I
	74FCT16374ETPAG8	PAG48	TSSOP	I
	74FCT16374ETPVG	PVG48	SSOP	I
	74FCT16374ETPVG8	PVG48	SSOP	I

## Datasheet Document History

09/28/2009	Pg. 7	Updated the ordering information by removing the "IDT" notation and non RoHS part.
05/22/2018	Pg. 1, 2, 5, 7	Added table under pin configuration diagram with detailed package information. Updated the ordering information diagram by deleting 54FCT, MIL, Cerpack package and adding Tube, Tape and Reel. Added orderable part information table.
08/06/2018	Pg. 7	Corrected ordering information diagram symbol for "-"43
03/26/2019	Pg. 7	Typo in above text; should be -40 Not -43

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(Disclaimer Rev.1.0 Mar 2020)

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