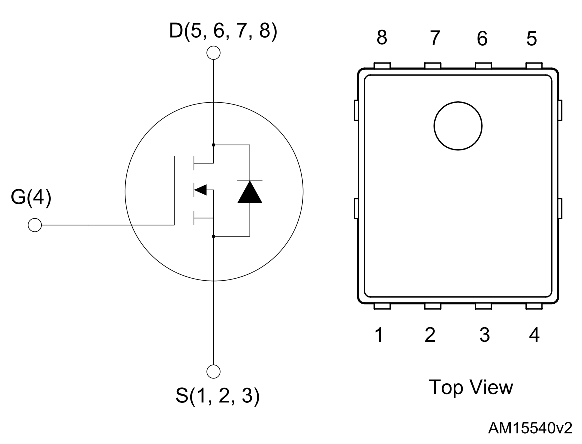
STL70N4LLF5

Automotive-grade N-channel 40 V, 6.1 mΩ typ., 18 A STripFET™ F5 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL70N4LLF5	40 V	6.7 mΩ	18 A

- AEC-Q101 qualified
- Low on-resistance $R_{DS(on)}$
- High avalanche ruggedness
- Low gate drive power loss
- Wettable flank package

Applications

- Switching applications

Description

This N-channel Power MOSFET is developed using the STripFET™ F5 technology and has been optimized to achieve very low on-state resistance, contributing to a FoM that is among the best in its class.

Table 1: Device summary

Order code	Marking	Package	Packing
STL70N4LLF5	70N4LLF5	PowerFLAT™ 5x6	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 22	V
I_D(1)	Drain current (continuous) at T_C = 25 °C	70	A
I_D(1)	Drain current (continuous) at T_c = 100 °C	44	
I_D(2)	Drain current (continuous) at T_{pcb} = 25 °C	18	
I_D(2)	Drain current (continuous) at T_{pcb} = 100 °C	11.5	
I_{DM}(1)(3)	Drain current (pulsed)	72	
P_{TOT}(1)	Total dissipation at T_C = 25 °C	72	W
P_{TOT}(2)	Total dissipation at T_{pcb} = 25 °C	4.8	
T_{stg}	Storage temperature range	-55 to 175	°C
T_J	Operation junction temperature range		

Notes:

(1)The value is rated according to R_{thj-c}.

(2)The value is rated according to $R_{thj-pcb}$.

(3)Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.08	°C/W
$R_{thj-pcb}$(1)	Thermal resistance junction-pcb	31.3	

Notes:

(1)When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 s

Table 4: Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current (pulse width limited by $T_{jmax.}$)	9	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AV}, V_{DD} = 24 V)	470	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0 V	40			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V V_{DS} = 40 V			1	µA
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V V_{DS} = 40 V, T_J = 125 °C [1]			10	
I_{GSS}	Gate-body leakage current	V_{GS} = ± 22 V, V_{DS} = 0 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS} , I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 9 A		6.1	6.7	mΩ
		V_{GS} = 4.5 V, I_D= 9 A		7.6	9.0	

Notes:

[1] Defined by design, not subject to production test

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	1570	-	pF
C_{oss}	Output capacitance		-	257	-	pF
C_{rss}	Reverse transfer capacitance		-	32	-	pF
Q_g	Total gate charge	V_{DD} = 15 V, I_D = 18 A, V_{GS} = 4.5 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	12.9	-	nC
Q_{gs}	Gate-source charge		-	3.9	-	nC
Q_{gd}	Gate-drain charge		-	5.3	-	nC
R_G	Gate input resistance	f = 1 MHz, gate DC bias = 0 V, test signal level = 20 mV, I_D = 0 A	-	1.5	-	Ω

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V, I_D = 9 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"*)	-	14	-	ns
t_r	Rise time		-	42	-	ns
$t_{d(off)}$	Turn-off delay time		-	37	-	ns
t_f	Fall time		-	5.2	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		18	A
I_{SDM}(1)	Source-drain current pulsed		-		72	A
V_{SD}(2)	Forward on voltage	I_{SD} = 18 A, V_{GS} = 0 V			1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 18 A, di/dt = 100 A/µs, V_{DD} = 25 V, T_J = 150 °C	-	27.2		ns
Q_{rr}	Reverse recovery charge		-	24.5		nC
I_{RRM}	Reverse recovery current		-	1.8		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.2 Electrical characteristics (curves)

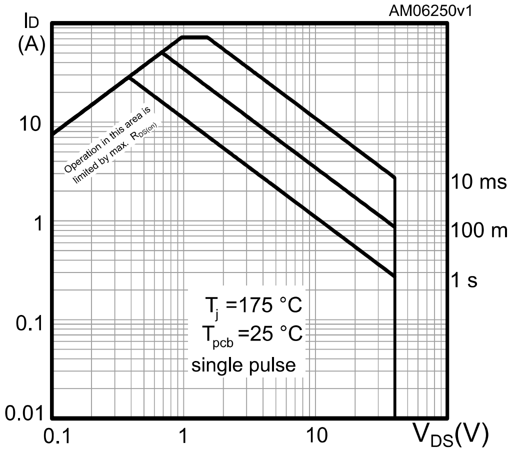


Figure 2: Safe operating area

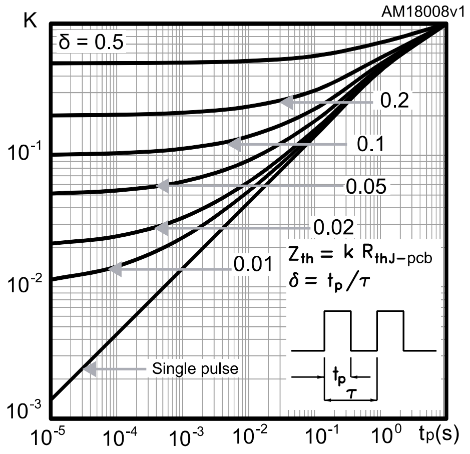


Figure 3: Thermal impedance

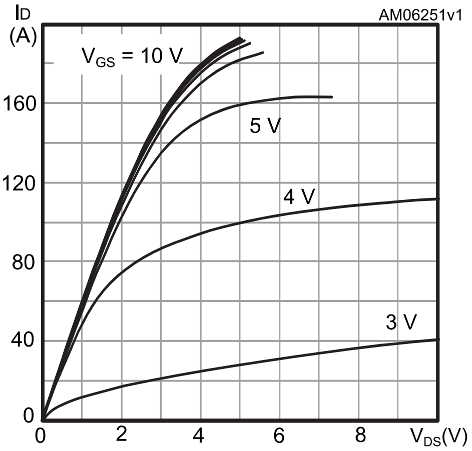


Figure 4: Output characteristics

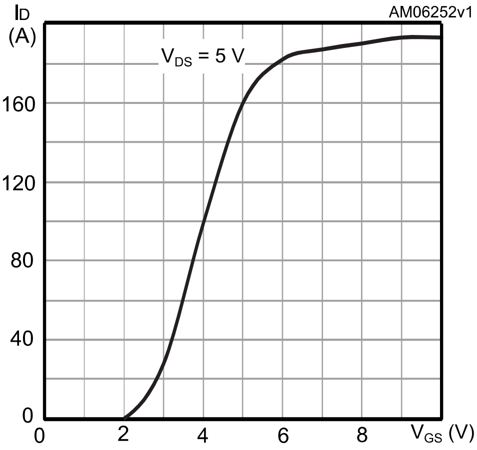


Figure 5: Transfer characteristics

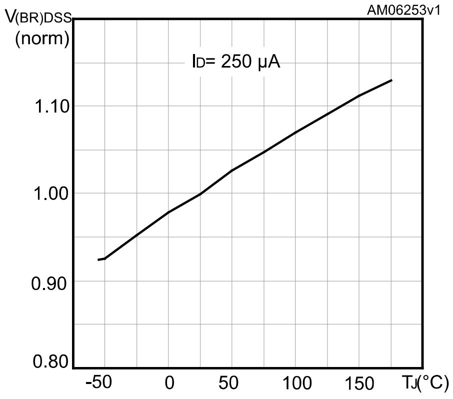


Figure 6: Normalized $V_{(BR)DSS}$ vs. temperature

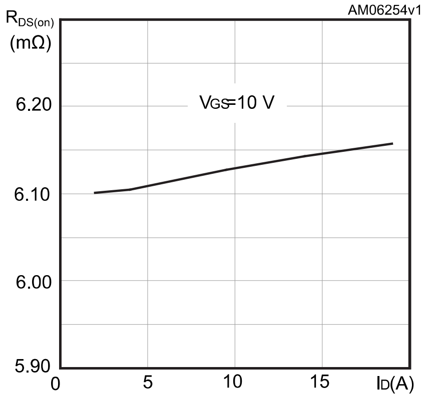


Figure 7: Static drain-source on-resistance

Figure 8: Gate charge vs. gate-source voltage

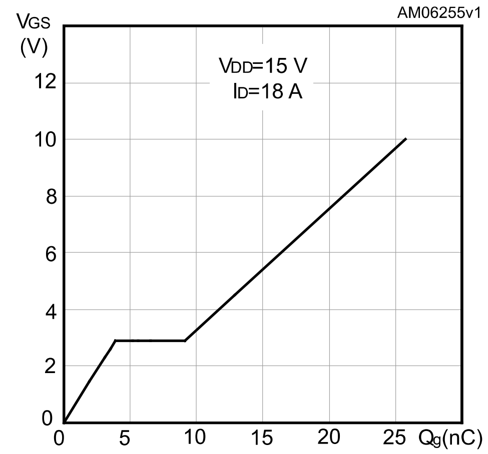


Figure 9: Capacitance variations

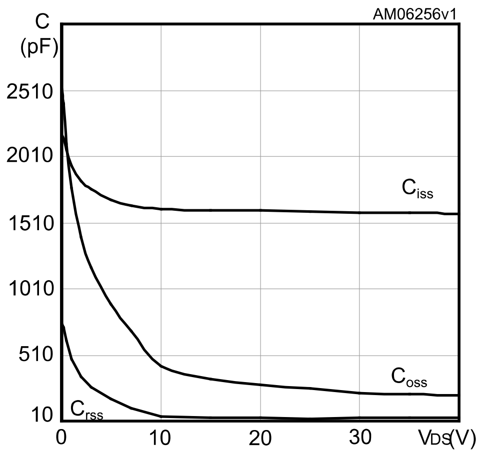


Figure 10: Normalized gate threshold voltage vs. temperature

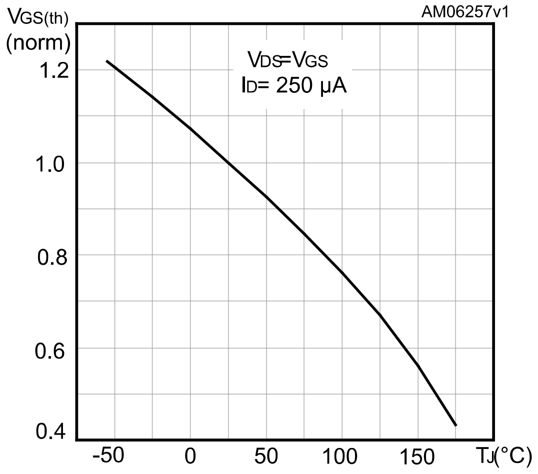


Figure 11: Normalized on-resistance vs. temperature

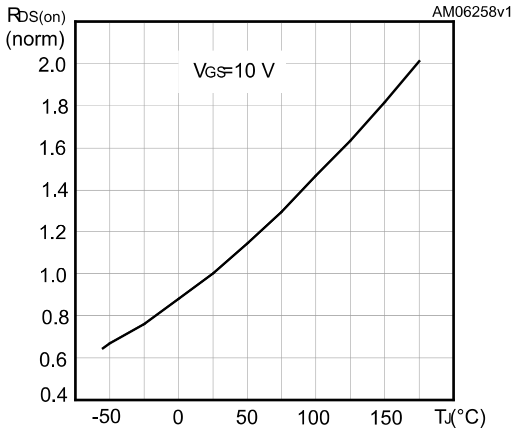
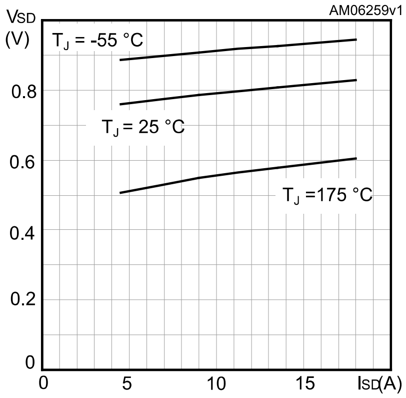


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

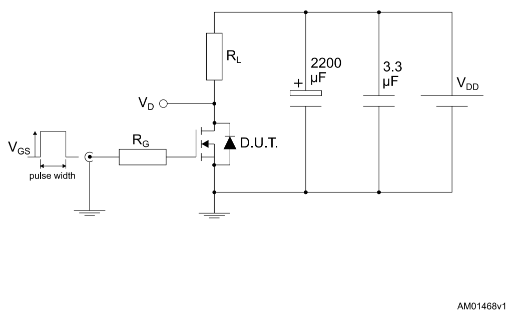


Figure 14: Test circuit for gate charge behavior

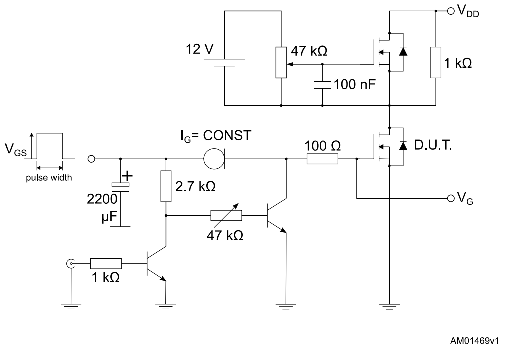


Figure 15: Test circuit for inductive load switching and diode recovery times

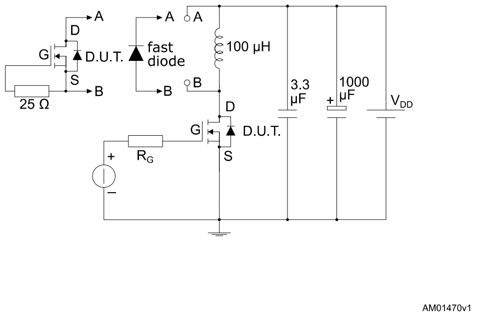


Figure 16: Unclamped inductive load test circuit

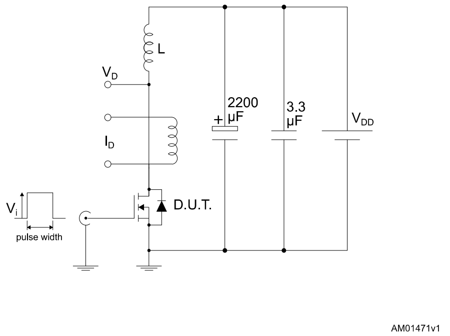


Figure 17: Unclamped inductive waveform

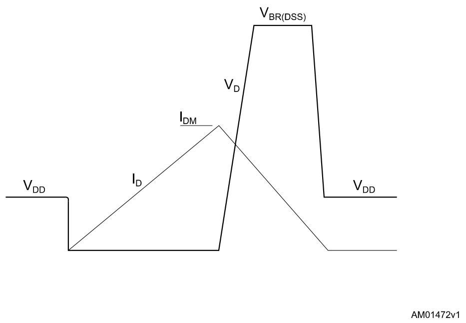
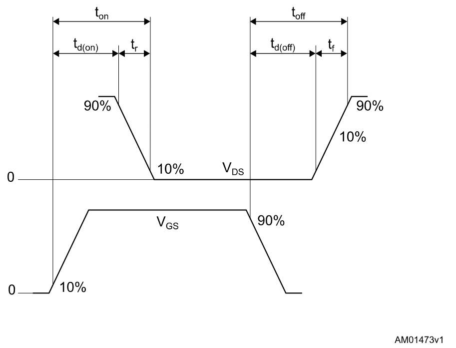


Figure 18: Switching time waveform

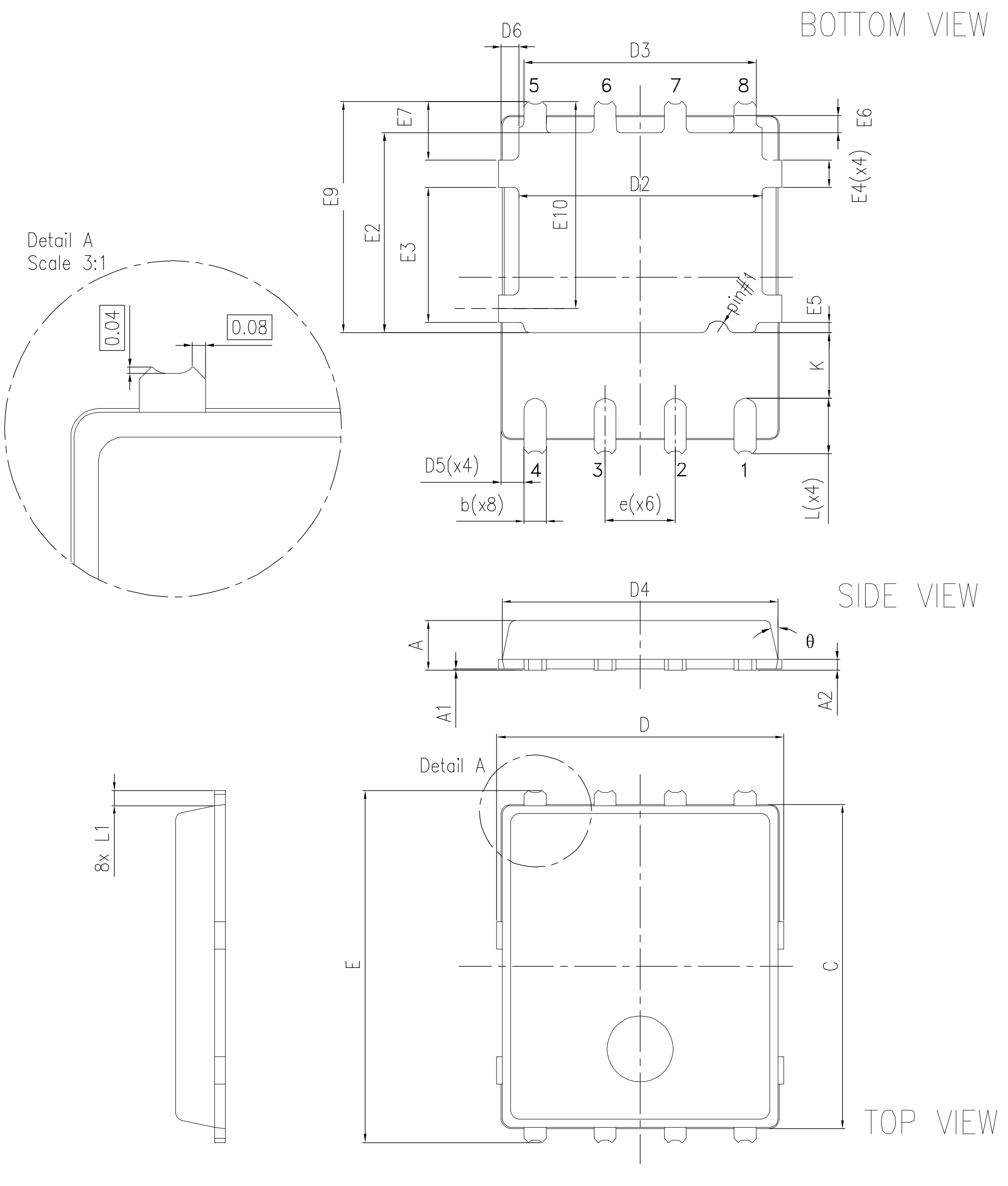


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 single island WF type C package information

Figure 19: PowerFLAT™ 5x6 WF type C package outline

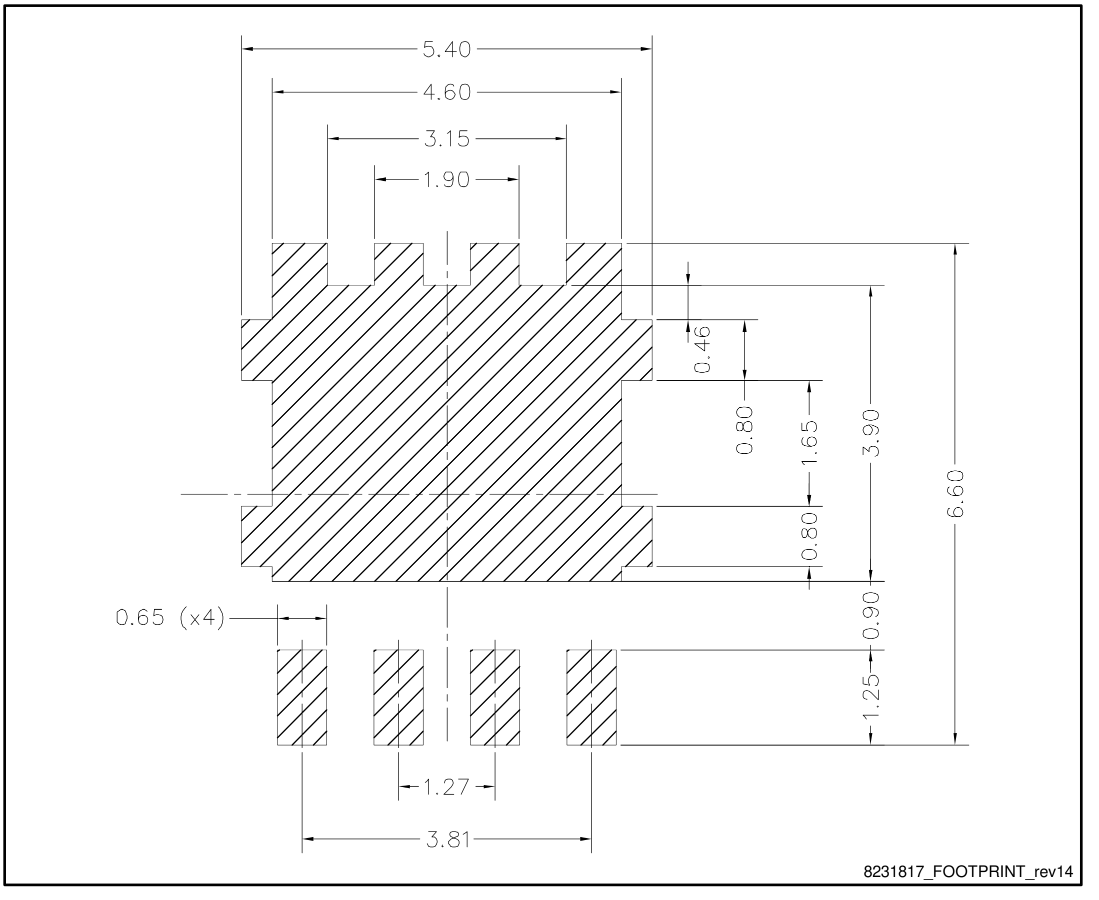


8231817_WF_typeC_r14

Table 9: PowerFLAT™ 5x6 WF type C mechanical data

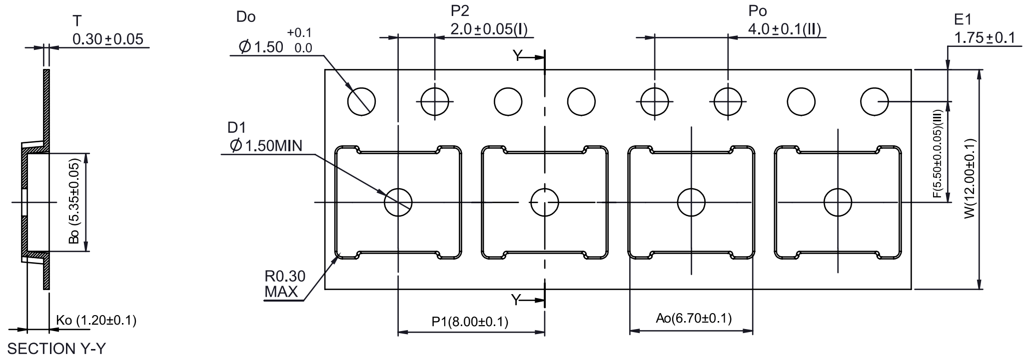
Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.05		1.35
L	0.90	1.00	1.10
L1	0.175	0.275	0.375
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 Packing information

Figure 21: PowerFLAT™ 5x6 WF tape (dimensions are in mm)



(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .

(III) Measured from centreline of sprocket hole to centreline of pocket.

Base and bulk quantity 3000 pcs

8234350_TapeWF_rev_C

Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

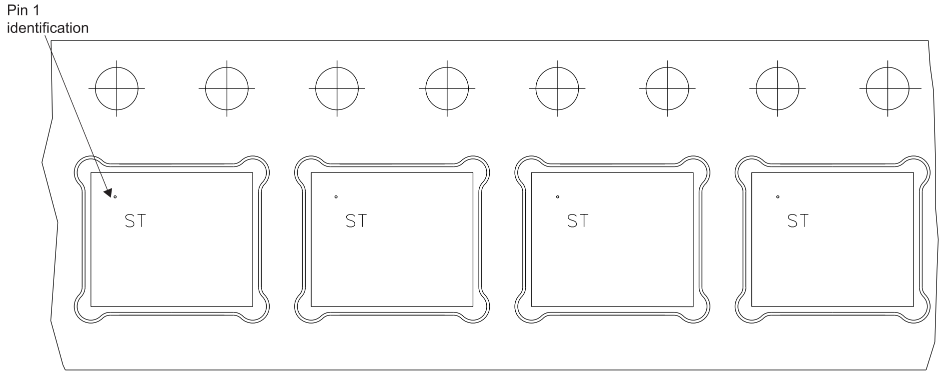
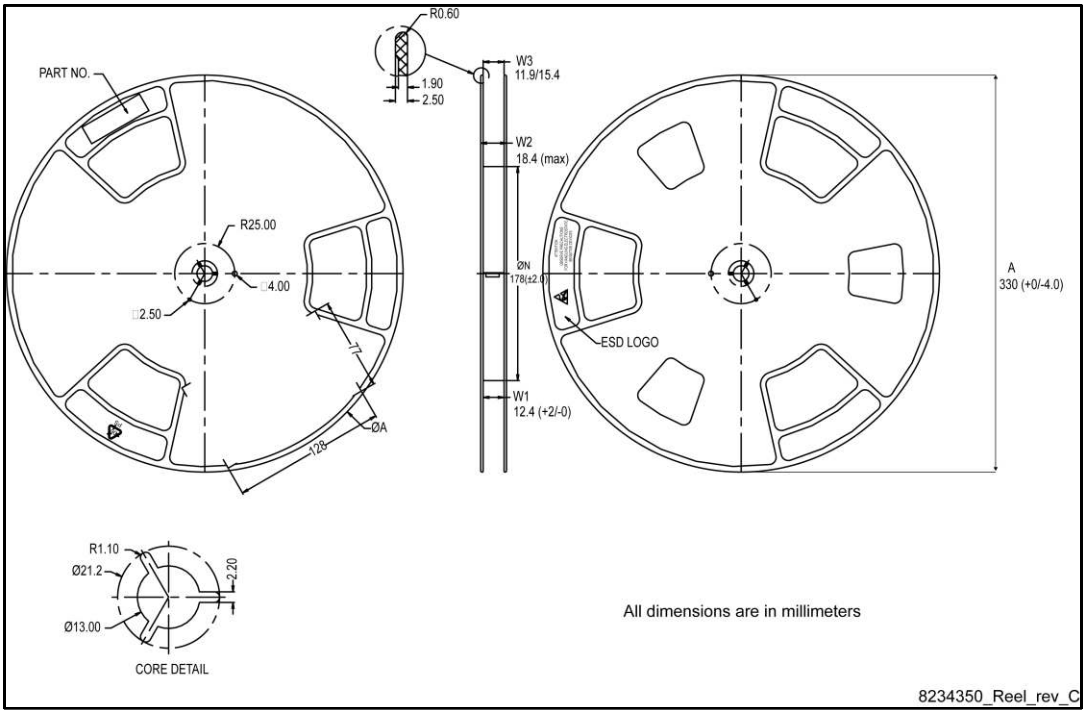


Figure 23: PowerFLAT™ 5x6 reel (dimensions are in mm)



All dimensions are in millimeters

8234350_Reel_rev_C

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
01-Dec-2008	1	First release.
18-Jul-2011	2	Section 4: Package mechanical data has been modified: – Added *Table 9: PowerFLAT™ 5x6 type S-C mechanical data* – Added *Figure 19: PowerFLAT™ 5x6 type S-C mechanical data* – Added *PowerFLAT™ 5x6 type C-B mechanical data* – Added *PowerFLAT™ 5x6 type C-B drawing* Minor text changes.
21-Dec-2011	3	Section 4: Package mechanical data has been modified.
25-Jan-2013	4	– Table 1: Device summary has been updated. -Minor text changes. –Changed: *Figure 1* -Added *Section 5: Packaging mechanical data*.
12-Feb-2013	5	-Updated T_J and T_{stg} in Table 2: Absolute maximum ratings. – Updated *Section 4: Package mechanical data* and *Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape*.
24-May-2013	6	– Modified: title and *Section 4: Package mechanical data* - Minor text changes.
17-Dec-2014	7	– Modified: Figure 2 and 3 – Updated: Figure 13, 14, 15 and 16 – Updated: Section 4: Package mechanical data and Section 5: Packaging mechanical data – Minor text changes.
08-Apr-2016	8	– Updated *Section 4: Package information* and *Section 4.1: Packing information* -Minor text changes.
22-Sep-2016	9	Updated $V_{GS(th)}$ in *Table 5: "On/off-states"*.

IMPORTANT NOTICE – PLEASE READ CAREFULLY