# 18Mb DDR SRAM 4-Word Burst

## MT57V1MH18E
## MT57V512H36E

## Features

- Fast cycle times
- Pipelined, double data rate operation
- Single 2.5V ±0.1V power supply (VDD)
- Separate isolated output buffer supply (VDDQ)
- JEDEC-standard1.5V to 1.8V (±0.1V) HSTL I/O
- User-selectable trip point with VREF
- HSTL programmable impedance outputs synchronized to optional dual-data clocks
- Optional-use echo clocks (CQ and CQ#) for flexible receive data synchronization
- JTAG boundary scan
- Fully-static design for reduced-power standby
- Clock-stop capability
- Common data inputs and data outputs
- Low-control ball count
- Internally self-timed, registered LATE WRITE cycles
- Linear burst order with four-tick burst counter
- 13mm x 15mm, 1mm pitch, 11 x 15 grid FBGA package
- Full data coherency, providing most current data

| Options | Marking[1] |
|---|---|
| • Clock Cycle Timing | |
| 5ns (200 MHz) | -5 |
| 6ns (167 MHz) | -6 |
| 7.5ns (133 MHz) | -7.5 |
| • Configurations | |
| 1 Meg x 18 | MT57V1MH18E |
| 512K x 36 | MT57V512H36E |
| • Operating Temperature Range | |
| Commercial (0°C ≤ $T_A$ ≤ 70°C) | None |
| • Package | |
| 165-ball, 13mm x 15mm FBGA | F |

NOTE:

1. A Part Marking Guide for the FBGA devices can be found on Micron’s Web site—http://www.micron.com/numberguide.

**Figure 1: 165-Ball FBGA**

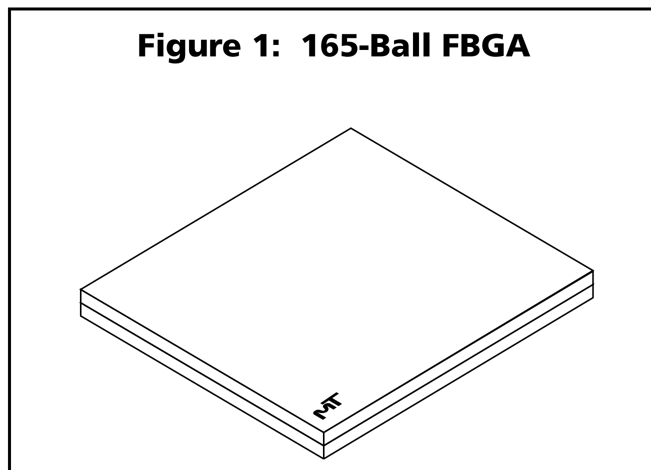

**Table 1: Valid Part Numbers**

| PART NUMBER | DESCRIPTION |
|---|---|
| MT57V1MH18EF-xx | 1 Meg x 18, DDRb4 SRAM |
| MT57V512H36EF-xx | 512K x 36, DDRb4 SRAM |

## General Description

The Micron® DDR synchronous SRAM employs high-speed, low-power CMOS designs using an advanced 6T CMOS process.

The DDR SRAM integrates an 18Mb SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by an input clock pair (K and K#) and are latched on the rising edge of K and K#. The synchronous inputs include all addresses, all data inputs, active LOW load (LD#) and read/write (R/W#). Write data is registered on the rising edges of both K and K#. Read data is driven on the rising edge of C and C# if provided, or on the rising edge of K and K#, if C and C# are not provided.

Asynchronous inputs include impedance match (ZQ). Synchronous data outputs (Q) are closely matched to the two echo clocks (CQ and CQ#), which can be used as data receive clocks. Output data clocks (C and C#) are also provided for maximum system clocking and data synchronization flexibility.


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Additional write registers are incorporated to enhance pipelined WRITE cycles and reduce READ-to-WRITE turnaround time. WRITE cycles are self-timed.

The device does not utilize internal phase-locked loops and can therefore be placed into a stopped-clock state to minimize power without lengthy restart times.

Four balls are used to implement JTAG test capabilities: test mode select (TMS), test data-in (TDI), test clock (TCK), and test data-out (TDO). JTAG circuitry is used to serially shift data to and from the SRAM. JTAG inputs use JEDEC-standard 2.5V I/O levels to shift data during this testing mode of operation.

The device can be used in HSTL systems by supplying an appropriate reference voltage (VREF). The device is ideally suited for applications requiring very rapid data transfer by operation in data-doubled mode. The device is also ideal in applications requiring the cost benefits of pipelined CMOS SRAMs and the reduced READ-to-WRITE turnaround times of Late Write SRAMs.

The SRAM operates from a 2.5V power supply, and all inputs and outputs are HSTL-compatible. The device is ideally suited for cache, network, telecom, DSP, and other applications that benefit from a very wide, high-speed data bus.

Please refer to Micron's Web site (www.micron.com/sramds) for the latest data sheet.

## DDR Operation

The DDR SRAM enables high performance operation through high-clock frequencies (achieved through pipelining) and double data rate mode of operation. At slower frequencies, the DDR SRAM requires a single NO OPERATION (NOP) cycle when transitioning from a READ to a WRITE cycle. At higher frequencies, a second NOP cycle may be required to prevent bus contention. NOP cycles are not required when switching from a WRITE to a READ.

If a READ occurs after a WRITE cycle, address and data for the WRITE are stored in registers. The write information must be stored because the SRAM cannot perform the last word write to the array without conflicting with the READ. The data stays in this register until the next WRITE cycle occurs. On the first WRITE cycle after the READ(s), the stored data from the earlier WRITE will be written into the SRAM array. This is called a posted write.

A read can be made immediately to an address even if that address was written in the previous cycle. During this READ cycle, the SRAM array is bypassed, and data is read instead from the data register storing the recently written data. This is transparent to the user. This feature facilitates system data coherency.

The DDR SRAM differs in some ways from its predecessor, the Claymore DDR SRAM. Single data rate operation is not supported, hence, no SD/DD# ball is provided. Only bursts of four are supported. In addition to the echo clocks, two single-ended input clocks are available (C and C#). The SRAM synchronizes its output data to these data clock rising edges if provided. If not present, C and C# must be tied HIGH and output timing is derived from K and K#. No differential clocks are used in this device. This clocking scheme provides greater system tuning capability than Claymore SRAMs and reduces the number of input clocks required by the bus master.


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## Programmable Impedance Output Buffer

The DDR SRAM is equipped with programmable impedance output buffers. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ ball and VSS. The value of the resistor must be five times the desired impedance. For example, a 350Ω resistor is required for an output impedance of 70Ω. To ensure that output impedance is one-fifth the value of RQ (within 15 percent), the range of RQ is 175Ω to 350Ω. Alternately, the ZQ ball can be connected directly to VDDQ, which will place the device in a minimum impedance mode.

Output impedance updates may be required because variations may occur in supply voltage and temperature over time. The device samples the value of RQ. An update of the impedance is transparent to the system. Impedance updates do not affect device operation, and all data sheet timing and current specifications are met during an update.

The device will power up with an output impedance set at 50Ω. To guarantee optimum output driver impedance after power-up, the SRAM needs 1,024 cycles to update the impedance. The user can operate the part with fewer than 1,024 clock cycles, but optimal output impedance is not guaranteed.

## Clocking

The DDR SRAM supports flexible clocking approaches. C and C# may be supplied to the SRAM to synchronize data output across multiple devices, enabling the bus master to receive all data simultaneously. If C and C# are not provided (tied HIGH) K and K# are used as the output timing reference.

The echo clocks (CQ and CQ#) provide another alternative for data synchronization. The echo clocks are controlled exactly like the DQ signals except that CQ and CQ# have an additional small delay for easier data capture by the bus master. Echo clocks must be separately received for each SRAM in the system. Use of echo clocks maximizes the available data window for each SRAM in the system.

The output echo clocks are precise references to output data. CQ and CQ# are both rising edge and falling edge accurate and are 180° out of phase. Either or both may be used for output data capture. K or C rising edge triggers CQ rising and CQ# falling edge. CQ rising edge indicates first data response for QDRI and DDRI (version 1, non-DLL) SRAM, while CQ# rising edge indicates first data response for QDRII and DDRII (version 2, DLL) SRAM.


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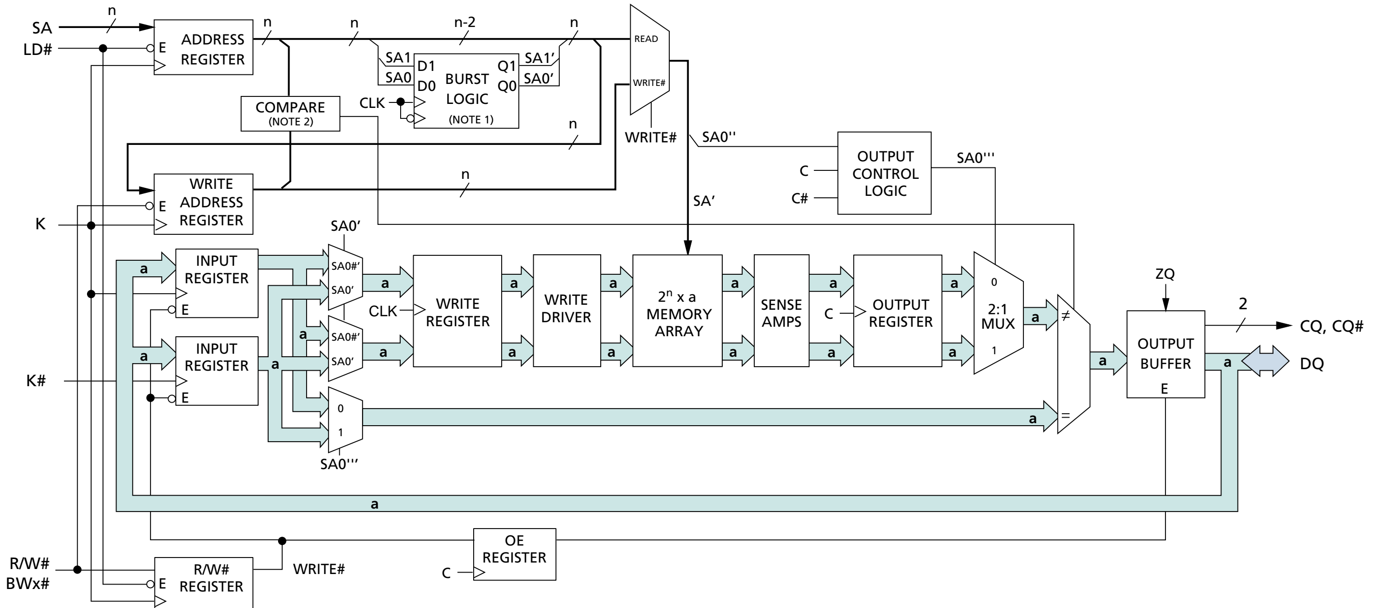
## Figure 2: Functional Block Diagram
## 1 Meg x 18; 512K x 36




NOTE:

1. SA0 and SA1 are advanced in linear burst order at each K and K# rising edge.
2. The compare width is n – 2 bits. The compare is performed only if a WRITE is pending and a READ cycle is requested. If the address matches, data is routed directly to the device outputs, bypassing the memory array.
3. Figure 2 illustrates simplified device operation. See truth tables, ball descriptions, and timing diagrams for detailed information.
4. CQ and CQ# do not tri-state except during some JTAG test modes.
5. For 1 Meg x 18, n = 20 and a = 18.
   For 512K x 36, n = 19 and a = 36.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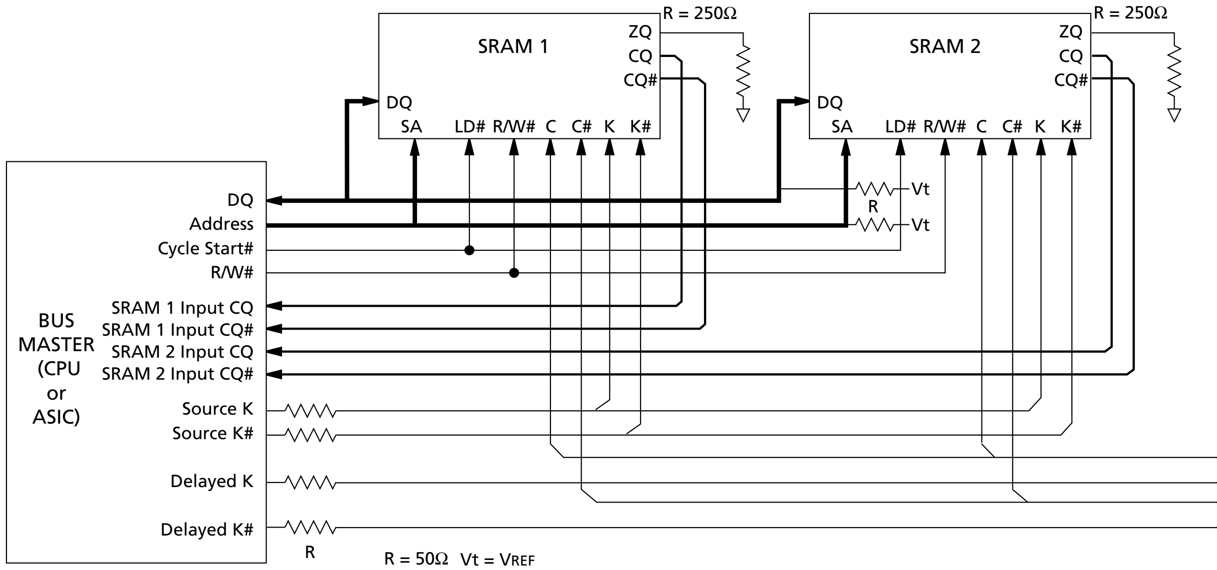
## Figure 3: Application Example




NOTE:

1. Consult Micron Technical Notes for more thorough discussions of clocking schemes.
2. Data capture is possible using only one of the two signals. CQ and CQ# clocks are optional use outputs.
3. For high frequency applications (200 MHz and faster) the CQ and CQ# clocks (for data capture) are recommended over the C and C# clocks (for data alignment). The C and C# clocks are optional use inputs.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## Table 2: 1 Meg x 18 Ball Layout (Top View) 165-Ball FBGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | CQ# | VSS | SA | R/W# | BW1# | K# | NC | LD# | SA | VSS/SA[1] | CQ |
| B | NC | DQ9 | NC | SA | NC | K | BW0# | SA | NC | NC | DQ8 |
| C | NC | NC | NC | VSS | SA | SA0 | SA1 | VSS | NC | DQ7 | NC |
| D | NC | NC | DQ10 | VSS | VSS | VSS | VSS | VSS | NC | NC | NC |
| E | NC | NC | DQ11 | VDDQ | VSS | VSS | VSS | VDDQ | NC | NC | DQ6 |
| F | NC | DQ12 | NC | VDDQ | VDD | VSS | VDD | VDDQ | NC | NC | DQ5 |
| G | NC | NC | DQ13 | VDDQ | VDD | VSS | VDD | VDDQ | NC | NC | NC |
| H | NC | VREF | VDDQ | VDDQ | VDD | VSS | VDD | VDDQ | VDDQ | VREF | ZQ |
| J | NC | NC | NC | VDDQ | VDD | VSS | VDD | VDDQ | NC | DQ4 | NC |
| K | NC | NC | DQ14 | VDDQ | VDD | VSS | VDD | VDDQ | NC | NC | DQ3 |
| L | NC | DQ15 | NC | VDDQ | VSS | VSS | VSS | VDDQ | NC | NC | DQ2 |
| M | NC | NC | NC | VSS | VSS | VSS | VSS | VSS | NC | DQ1 | NC |
| N | NC | NC | DQ16 | VSS | SA | SA | SA | VSS | NC | NC | NC |
| P | NC | NC | DQ17 | SA | SA | C | SA | SA | NC | NC | DQ0 |
| R | TDO | TCK | SA | SA | SA | C# | SA | SA | SA | TMS | TDI |

NOTE:
1. Expansion address: 10A for 36Mb


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## Table 3: 512K x 36 Ball Layout (Top View) 165-Ball FBGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | CQ# | VSS | NC/SA[1] | R/W# | BW2#[2] | K# | BW1#[3] | LD# | SA | VSS | CQ |
| **B** | NC | DQ27 | DQ18 | SA | BW3#[4] | K | BW0#[5] | SA | NC | NC | DQ8 |
| **C** | NC | NC | DQ28 | VSS | SA | SA0 | SA1 | VSS | NC | DQ17 | DQ7 |
| **D** | NC | DQ29 | DQ19 | VSS | VSS | VSS | VSS | VSS | NC | NC | DQ16 |
| **E** | NC | NC | DQ20 | VDDQ | VSS | VSS | VSS | VDDQ | NC | DQ15 | DQ6 |
| **F** | NC | DQ30 | DQ21 | VDDQ | VDD | VSS | VDD | VDDQ | NC | NC | DQ5 |
| **G** | NC | DQ31 | DQ22 | VDDQ | VDD | VSS | VDD | VDDQ | NC | NC | DQ14 |
| **H** | NC | VREF | VDDQ | VDDQ | VDD | VSS | VDD | VDDQ | VDDQ | VREF | ZQ |
| **J** | NC | NC | DQ32 | VDDQ | VDD | VSS | VDD | VDDQ | NC | DQ13 | DQ4 |
| **K** | NC | NC | DQ23 | VDDQ | VDD | VSS | VDD | VDDQ | NC | DQ12 | DQ3 |
| **L** | NC | DQ33 | DQ24 | VDDQ | VSS | VSS | VSS | VDDQ | NC | NC | DQ2 |
| **M** | NC | NC | DQ34 | VSS | VSS | VSS | VSS | VSS | NC | DQ11 | DQ1 |
| **N** | NC | DQ35 | DQ25 | VSS | SA | SA | SA | VSS | NC | NC | DQ10 |
| **P** | NC | NC | DQ26 | SA | SA | C | SA | SA | NC | DQ9 | DQ0 |
| **R** | TDO | TCK | SA | SA | SA | C# | SA | SA | SA | TMS | TDI |

NOTE:
1. Expansion address: 3A for 36Mb
2. BW2# controls writes to DQ18:DQ26
3. BW1# controls writes to DQ9:DQ17
4. BW3# controls writes to DQ27:DQ35
5. BW0# controls writes to DQ0:DQ8


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## Table 4: Ball Descriptions

| SYM | TYPE | DESCRIPTION |
|---|---|---|
| BW_# | Input | Synchronous Byte Writes: When LOW, these inputs cause their respective bytes to be registered and written if W# had initiated a WRITE cycle. These signals must meet setup and hold times around the rising edges of K and K# for each of the four rising edges comprising the WRITE cycle. See Ball Layout figures for signal to data relationships. |
| C<br>C# | Input | Output Clock: This clock pair provides a user-controlled means of tuning device output data. The rising edge of C# is used as the output reference for second and fourth output data. The rising edge of C is used as the output timing reference for first and third output data. Ideally, C# is 180 degrees out of phase with C. C and C# may be tied HIGH to force the use of K and K# as the output reference clocks instead of having to provide C and C# clocks. If tied HIGH, C and C# must remain HIGH and not be toggled during device operation. |
| K<br>K# | Input | Input Clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of K#. K# is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges. |
| LD# | Input | Synchronous Load: This input is brought LOW when a bus cycle sequence is to be defined. This definition includes address and read/write direction. All transactions operate on a burst of four data (two clock periods of bus activity). |
| R/W# | Input | Synchronous Read/Write Input: When LD# is LOW, this input designates the access type (READ when R/W# is HIGH, WRITE when R/W# is LOW) for the loaded address. R/W# must meet the setup and hold times around the rising edge of K. |
| SA0<br>SA1<br>SA | Input | Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K. SA0 and SA1 are used as the lowest address bit for BURST READ and BURST WRITE operations. These inputs are ignored when device is deselected or once BURST operation is in progress. |
| TCK | Input | IEEE 1149.1 Clock Input: JEDEC-standard 2.5V I/O levels. This ball must be tied to VSS if the JTAG function is not used in the circuit. |
| TMS<br>TDI | Input | IEEE 1149.1 Test Inputs: JEDEC-standard 2.5V I/O levels. These balls may be left as No Connects if the JTAG function is not used in the circuit. |
| VREF | Input | HSTL Input Reference Voltage: Nominally VDDQ/2. Provides a reference voltage for the input buffers. |
| ZQ | Input | Output Impedance Matching Input: This input is used to tune the device outputs to the system data bus impedance. DQ and CQ output impedance is set to 0.2 x RQ, where RQ is a resistor from this ball to ground. Alternately, this ball can be connected directly to VDDQ, which enables the minimum impedance mode. This ball cannot be connected directly to GND or left unconnected. |
| DQ_ | Input/ Output | Synchronous Data I/Os: Input data must meet setup and hold times around the rising edges of K and K#. Output data is synchronized to the respective C and C# data clocks or to K and K# if C and C# are tied HIGH. See Ball Layout figures for ball site location of individual signals. The x18 devices uses DQ0:DQ17, and the x36 device uses DQ0:DQ35. |
| CQ,<br>CQ# | Output | Echo Clocks: The edges of these outputs are tightly matched to the synchronous data outputs and can be used as data valid indication. These signals run freely and do not stop when Q tri-states. |
| TDO | Output | IEEE 1149.1 Test Output: JEDEC-standard 2.5V I/O level. |
| VDD | Supply | Power Supply: 2.5V nominal. See DC Electrical Characteristics and Operating Conditions for range. |
| VDDQ | Supply | Power Supply: Isolated Output Buffer Supply. Nominally 1.5V. See DC Electrical Characteristics and Operating Conditions for range. |
| VSS | Supply | Power Supply: GND. |
| NC | – | No Connect: These balls are internally connected to the die, but have no function and may be left not connected to board to minimize ball count. |


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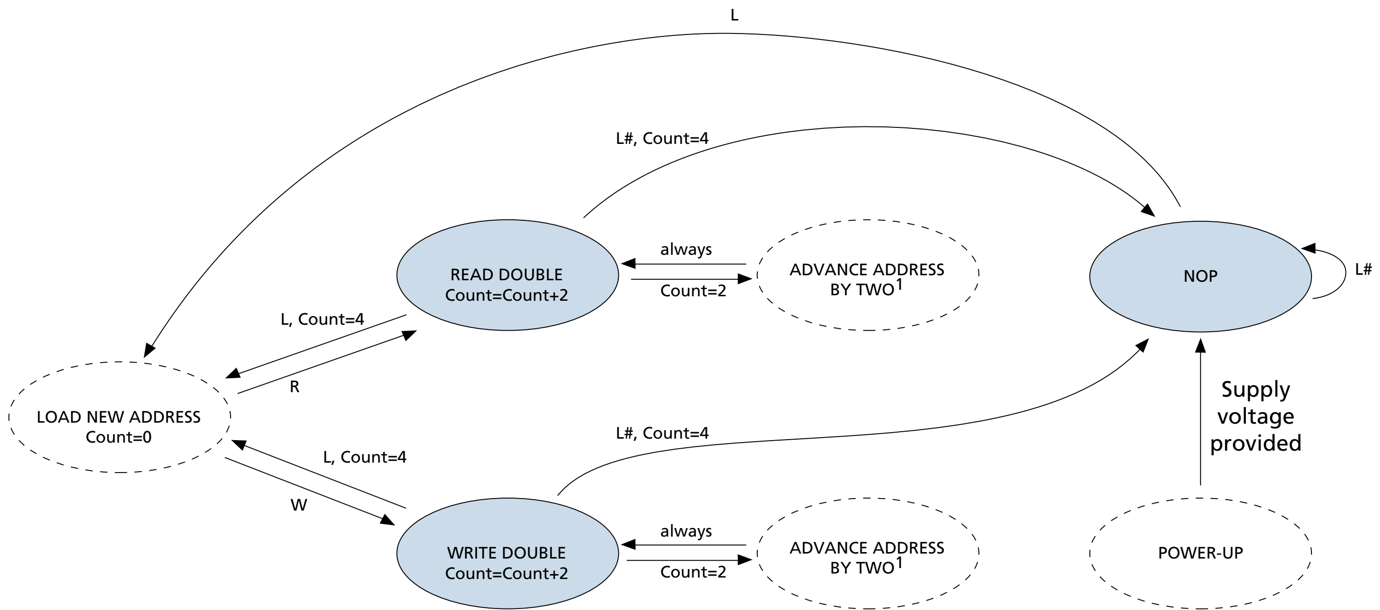
## Table 5: Linear Burst Address

| FIRST ADDRESS (EXTERNAL) | SECOND ADDRESS (INTERNAL) | THIRD ADDRESS (INTERNAL) | FOURTH ADDRESS (INTERNAL) |
|---|---|---|---|
| X...X00 | X...X01 | X...X10 | X...X11 |
| X...X01 | X...X10 | X...X11 | X...X00 |
| X...X10 | X...X11 | X...X00 | X...X01 |
| X...X11 | X...X00 | X...X01 | X...X10 |

## Figure 4: Bus Cycle State Diagram




NOTE:
1. SA0 and SA1 are internally advanced in accordance with the burst order table. Bus cycle is terminated after burst count = 4.
2. State transitions: L = (LD# = LOW); L# = (LD# = HIGH); R = (R/W# = HIGH); W = (R/W# = LOW).
3. State machine control timing sequence is controlled by K.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## Table 6: Truth Table

Notes 1-6

| OPERATION | LD# | R/W# | K | DQ | DQ | DQ | DQ |
|---|---|---|---|---|---|---|---|
| WRITE Cycle:<br>Load address, input write data on two consecutive K and K# rising edges | L | L | L→H | DIN(A0) at K(t)↑ | DIN(A0 + 1) at K#(t + 1)↑ | DIN(A0 + 2) at K(t + 2)↑ | DIN(A0 + 3) at K#(t + 3)↑ |
| READ Cycle:<br>Load address, read data on two consecutive C and C# rising edges | L | H | L→H | QOUT(A0) at C(t)↑ | QOUT(A0 + 1) at C#(t + 1)↑ | QOUT(A0 + 2) at C(t + 2)↑ | QOUT(A0 + 3) at C#(t + 3)↑ |
| NOP: No operation | H | X | L→H | High-Z | High-Z | High-Z | High-Z |
| STANDBY: Clock stopped | X | X | Stopped | Previous State | Previous State | Previous State | Previous State |

## Table 7: BYTE WRITE Operation

Note 7, 8

| OPERATION | K | K# | BW0# | BW1# |
|---|---|---|---|---|
| WRITE D0:17 at K rising edge | L→H | | 0 | 0 |
| WRITE D0:17 at K# rising edge | | L→H | 0 | 0 |
| WRITE D0:8 at K rising edge | L→H | | 0 | 1 |
| WRITE D0:8 at K# rising edge | | L→H | 0 | 1 |
| WRITE D9:17 at K rising edge | L→H | | 1 | 0 |
| WRITE D9:17 at K# rising edge | | L→H | 1 | 0 |
| WRITE nothing at K rising edge | L→H | | 1 | 1 |
| WRITE nothing at K# rising edge | | L→H | 1 | 1 |

NOTE:

1. X means "Don't Care." H means logic HIGH. L means logic LOW. ↑ means rising edge; ↓ means falling edge.
2. Data inputs are registered at K and K# rising edges. Data outputs are delivered at C and C# rising edges, except if C and C# are HIGH, then data outputs are delivered at K and K# rising edges.
3. R/W# and LD# must meet setup and hold times around the rising edge (LOW to HIGH) of K. All control inputs are registered during the rising edge of K.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
5. Refer to state diagram and timing diagrams for clarification. A0 refers to the address input during a WRITE or READ cycle. A0 + 1 refers to the next internal burst address in accordance with the burst sequence.
6. It is recommended that K = K# = C = C# when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
7. Assumes a WRITE cycle was initiated. BW0# and BW1# can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.
8. This table illustrates operation for x18 devices. The x36 operation is similar except for the addition of BW2# (controls DQ18:DQ26) and BW3# (controls DQ27:DQ35).


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## Absolute Maximum Ratings

Voltage on VDD Supply Relative to VSS..... -0.5V to +3.4V
Voltage on VDDQ Supply
Relative to VSS ...................................... -0.5V to +VDD
VIN ..................................................... -0.5V to VDD +0.5V
Storage Temperature.............................-55°C to +125°C
Junction Temperature......................................... +125°C
Short Circuit Output Current ............................. ±70mA

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Maximum Junction Temperature depends upon package type, cycle time, loading, ambient temperature, and airflow.

## Table 8: DC Electrical Characteristics and Operating Conditions

Notes appear following parameter tables on page 14; 0°C ≤ $T_A$ ≤ +70°C; VDD = 2.5V ±0.1V unless otherwise noted

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input High (Logic 1) Voltage | | VIH(DC) | VREF + 0.1 | VDDQ + 0.3 | V | 3, 4 |
| Input Low (Logic 0) Voltage | | VIL(DC) | -0.3 | VREF - 0.1 | V | 3, 4 |
| Clock Input Signal Voltage | | VIN | -0.3 | VDDQ + 0.3 | V | 3, 4 |
| Input Leakage Current | 0V ≤ VIN ≤ VDDQ | ILI | -5 | 5 | µA | |
| Output Leakage Current | Output(s) disabled, 0V ≤ VIN ≤ VDDQ (Q) | ILO | -5 | 5 | µA | |
| Output High Voltage | \|IOH\| ≤ 0.1mA | VOH (LOW) | VDDQ - 0.2 | VDDQ | V | 3, 5, 6 |
| | Note 1 | VOH | VDDQ/2 - 0.12 | VDDQ/2 + 0.12 | V | 3, 5, 6 |
| Output Low Voltage | IOL ≤ 0.1mA | VOL (LOW) | VSS | 0.2 | V | 3, 5, 6 |
| | Note 2 | VOL | VDDQ/2 - 0.12 | VDDQ/2 + 0.12 | V | 3, 5, 6 |
| Supply Voltage | | VDD | 2.4 | 2.6 | V | 3 |
| Isolated Output Buffer Supply | | VDDQ | 1.4 | 1.9 | V | 3, 7 |
| Reference Voltage | | VREF | 0.68 | 0.95 | V | 3 |

## Table 9: AC Electrical Characteristics and Operating Conditions

Notes appear following parameter tables on page 14; 0°C ≤ $T_A$ ≤ +70°C; VDD = 2.5V ±0.1V unless otherwise noted

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input High (Logic 1) Voltage | | VIH(AC) | VREF + 0.2 | – | V | 3, 4, 8 |
| Input Low (Logic 0) Voltage | | VIL(AC) | – | VREF - 0.2 | V | 3, 4, 8 |


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## Table 10: IDD Operating Conditions and Maximum Limits

Notes appear following parameter tables on page 14; 0°C ≤ $T_A$ ≤ +70°C; VDD = 2.5V ±0.1V unless otherwise noted

| DESCRIPTION | CONDITIONS | SYM | TYP | MAX -5 | MAX -6 | MAX -7.5 | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|
| Operating Supply Current: DDR | All inputs ≤ VIL or ≥ VIH; Cycle time ≥ tKHKH (MIN); Outputs open x:1 ratio for READs to WRITEs; 50% address and data bits toggling on each clock cycle | IDD<br>x18<br>x36 | TBD | 225<br>300 | 200<br>260 | 175<br>225 | mA | 9, 10 |
| Standby Supply Current: NOP | tKHKH = tKHKH (MIN);<br>Device in NOP state;<br>All addresses/data static | ISB1<br>x18<br>x36 | TBD | 170<br>180 | 150<br>160 | 125<br>135 | mA | 10, 11 |
| Stop Clock Current | Cycle time = 0; Input Static | ISB | TBD | 75 | 75 | 75 | mA | 10 |
| Output Supply Current: DDR (Information only) | CL = 15pF | IDDQ<br>x18<br>x36 | – | 41<br>81 | 34<br>68 | 28<br>55 | mA | 12 |

## Table 11: Capacitance

Note 13; notes appear following parameter tables on page 14

| DESCRIPTION | CONDITIONS | SYMBOL | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Address/Control Input Capacitance | $T_A$ = 25°C; f = 1 MHz | CI | 4.5 | 5.5 | pF |
| Output Capacitance (D,Q) | | CO | 6 | 7 | pF |
| Clock Capacitance | | CCK | 5.5 | 6.5 | pF |

## Table 12: Thermal Resistance

Note 13; notes appear following parameter tables on page 14

| DESCRIPTION | CONDITIONS | SYMBOL | TYP | UNITS | NOTES |
|---|---|---|---|---|---|
| Junction to Ambient (Airflow of 1m/s) | Soldered on a 4.25 x 1.125 inch, 4-layer, printed circuit board | $\theta_{JA}$ | 19.4 | °C/W | 14 |
| Junction to Case (Top) | | $\theta_{JC}$ | 1.0 | °C/W | |
| Junction to Balls (Bottom) | | $\theta_{JB}$ | 9.6 | °C/W | 15 |



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## Table 13: AC Electrical Characteristics and Recommended Operating Conditions

Notes 16-18; notes appear following parameter tables; $0°C \leq T_A \leq +70°C$; $T_J \leq +95°C$; VDD = 2.5V ±0.1V

| DESCRIPTION | SYM | -5 | | -6 | | -7.5 | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| **Clock** | | | | | | | | | |
| Clock cycle time (K, K#, C, C#) | $^t$KHKH | 5.0 | | 6.0 | | 7.5 | | ns | |
| Clock HIGH time (K, K#, C, C#) | $^t$KHKL | 2.0 | | 2.4 | | 3.0 | | ns | |
| Clock LOW time (K, K#, C, C#) | $^t$KLKH | 2.0 | | 2.4 | | 3.0 | | ns | |
| Clock to clock# (K↑→K#↑, C↑→C#↑) | $^t$KHK#H | 2.4 | | 2.8 | | 3.4 | | ns | |
| Clock# to clock (K#↑→K↑, C#↑→C↑) | $^t$K#HKH | 2.4 | | 2.8 | | 3.4 | | ns | |
| Clock to data clock (K↑→C↑, K#↑→C#↑) | $^t$KHCH | 0.0 | 1.5 | 0.0 | 2.0 | 0.0 | 2.5 | ns | |
| **Output Times** | | | | | | | | | |
| C, C# HIGH to output valid | $^t$CHQV | | 2.4 | | 3.0 | | 3.6 | ns | |
| C, C# HIGH to output hold | $^t$CHQX | 0.8 | | 0.8 | | 0.8 | | ns | |
| C HIGH to output High-Z | $^t$CHQZ | | 2.4 | | 3.0 | | 3.6 | ns | 13, 19 |
| C HIGH to output Low-Z | $^t$CHQX1 | 0.8 | | 0.8 | | 0.8 | | ns | 19 |
| C, C# HIGH to CQ, CQ# HIGH | $^t$CHCQH | 0.8 | 2.6 | 0.8 | 3.2 | 0.8 | 3.8 | ns | 18 |
| CQ, CQ# HIGH to output valid | $^t$CQHQV | | 0.35 | | 0.40 | | 0.45 | ns | |
| CQ, CQ# HIGH to output hold | $^t$CQHQX | -0.35 | | -0.40 | | -0.45 | | ns | |
| CQ HIGH to output High-Z | $^t$CQHQZ | | 0.35 | | 0.40 | | 0.45 | ns | 13, 19 |
| CQ HIGH to output Low-Z | $^t$CQHQX1 | -0.35 | | -0.40 | | -0.45 | | ns | 19 |
| **Setup Times** | | | | | | | | | |
| Address valid to K rising edge | $^t$AVKH | 0.6 | | 0.7 | | 0.8 | | ns | 20 |
| Control inputs valid to K rising edge | $^t$IVKH | 0.6 | | 0.7 | | 0.8 | | ns | 20 |
| Data-in valid to K, K# rising edge | $^t$DVKH | 0.6 | | 0.7 | | 0.8 | | ns | 20 |
| **Hold Times** | | | | | | | | | |
| K rising edge to address hold | $^t$KHAX | 0.6 | | 0.7 | | 0.8 | | ns | 20 |
| K rising edge to control inputs hold | $^t$KHIX | 0.6 | | 0.7 | | 0.8 | | ns | 20 |
| K, K# rising edge to data-in hold | $^t$KHDX | 0.6 | | 0.7 | | 0.8 | | ns | 20 |


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## Notes

1. Outputs are impedance-controlled. $|I_{OH}| = (V_{DDQ}/2)/(RQ/5)$ for values of $175\Omega \leq RQ \leq 350\Omega$.
2. Outputs are impedance-controlled. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of $175\Omega \leq RQ \leq 350\Omega$.
3. All voltages referenced to $V_{SS}$ (GND).
4. Overshoot: $V_{IH(AC)} \leq V_{DD} + 0.7V$ for $t \leq {}^tKHKH/2$
   Undershoot: $V_{IL(AC)} \geq -0.5V$ for $t \leq {}^tKHKH/2$
   Power-up: $V_{IH} \leq V_{DDQ} + 0.3V$ and $V_{DD} \leq 2.4V$ and $V_{DDQ} \leq 1.4V$ for $t \leq 200ms$
   During normal operation, $V_{DDQ}$ must not exceed $V_{DD}$. Control input signals may not have pulse widths less than $^tKHKL$ (MIN) or operate at cycle rates less than $^tKHKH$ (MIN).
5. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
6. HSTL outputs meet JEDEC HSTL Class I and Class II standards.
7. The nominal value of $V_{DDQ}$ may be set within the range of 1.5V to 1.8V DC, and the variation of $V_{DDQ}$ must be limited to ±0.1V DC.
8. To maintain a valid level, the transitioning edge of the input must:
   a. Sustain a constant slew rate from the current AC level through the target AC level, $V_{IL(AC)}$ or $V_{IH(AC)}$
   b. Reach at least the target AC level
   c. After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL(DC)}$ or $V_{IH(DC)}$
9. $I_{DD}$ is specified with no output current and increases with faster cycle times. $I_{DDQ}$ increases with faster cycle times and greater output loading. Typical value is measured at 6ns cycle time.
10. Typical values are measured at $V_{DD}$ =2.5V, $V_{DDQ}$ = 1.5V, and temperature = 25°C.
11. NOP currents are valid when entering NOP after all pending READ and WRITE cycles are completed.
12. Average I/O current and power is provided for informational purposes only and is not tested. Calculation assumes that all outputs are loaded with $C_L$ (in farads), f = input clock frequency, half of outputs toggle at each transition (for example, n = 18 for x36), $C_O$ = 6pF, $V_{DDQ}$ = 1.5V and uses the equations: Average I/O Power as dissipated by the SRAM is:
    $P = 0.5 \times n \text{ x } f \text{ x } V_{DDQ}^2 \text{ x } (C_L + 2C_O)$. Average $I_{DDQ} = n \text{ x } f \text{ x } V_{DDQ} \text{ x } (C_L + C_O)$.
13. This parameter is sampled.
14. Average thermal resistance between the die and the case top surface per MIL SPEC 883 Method 1012.1.
15. Junction temperature is a function of total device power dissipation and device mounting environment. Measured per SEMI G38-87.
16. Control input signals may not be operated with pulse widths less than $^tKHKL$ (MIN).
17. Test conditions as specified with the output loading as shown in Figure 5, unless otherwise noted.
18. If C and C# are tied HIGH, then K, K# become the references for C and C# timing parameters.
19. $^tCHQXI$ is greater than $^tCHQZ$ at any given voltage and temperature.
20. This is a synchronous device. All addresses, data, and control lines must meet the specified setup and hold times for all latching clock edges.


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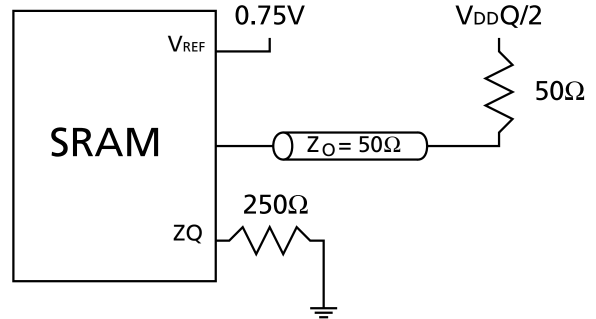
## AC Test Conditions

Input pulse levels . . . . . . . . . . . . . . . . . . . 0.25V to 1.25V
Input rise and fall times . . . . . . . . . . . . . . . . . . . . . 0.7ns
Input timing reference levels . . . . . . . . . . . . . . . . . 0.75V
Output reference levels . . . . . . . . . . . . . . . . . . . $V_{DD}Q/2$
ZQ for 50Ω impedance . . . . . . . . . . . . . . . . . . . . . 250Ω
Output load . . . . . . . . . . . . . . . . . . . . . . . . . See Figure 5

**Figure 5: Output Load Equivalent**





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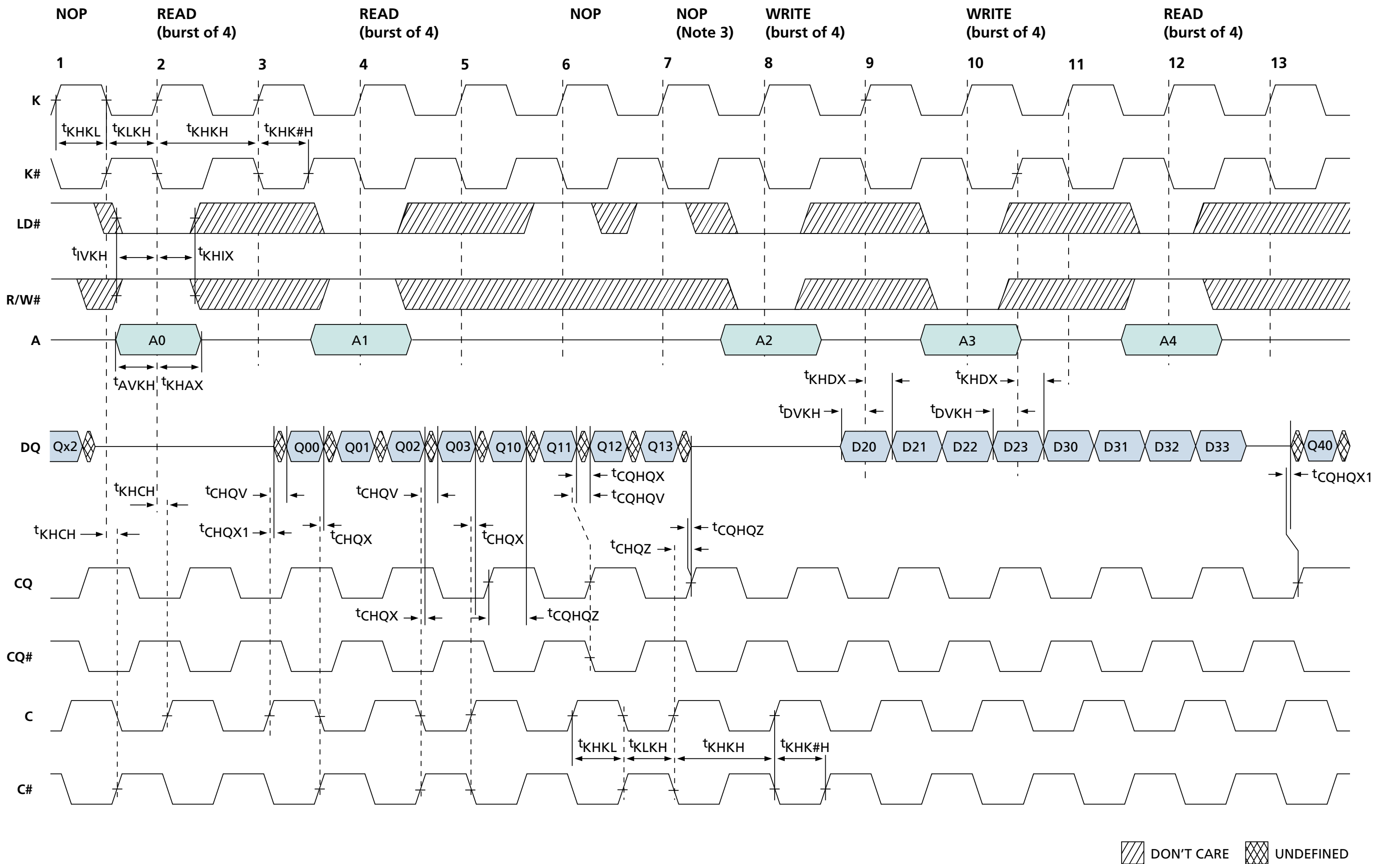
## Figure 6: READ/WRITE Timing




NOTE:

1. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, etc.
2. Outputs are disabled (High-Z) one clock cycle after a NOP.
3. The second NOP cycle is not necessary for correct device operation; however, at high clock frequencies it may be required to prevent bus contention.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## IEEE 1149.1 Serial Boundary Scan (JTAG)

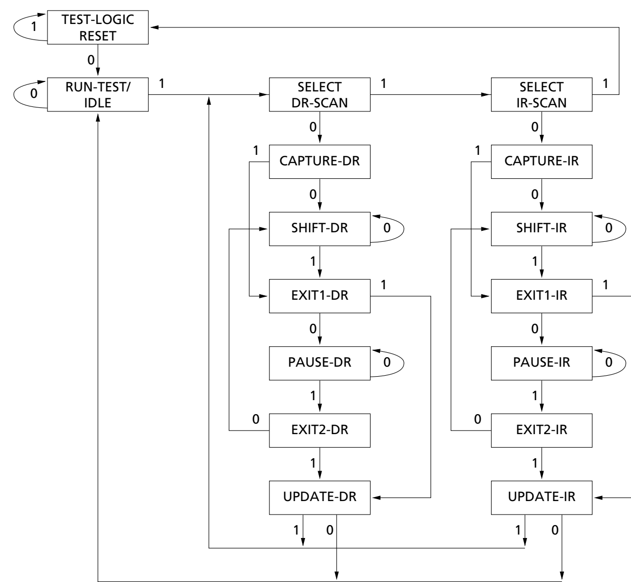
The SRAM incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully-compliant TAPs. The TAP operates using JEDEC-standard 2.5V I/O logic levels.

The SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

### *Disabling the JTAG Feature*

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (VSS) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. Alternately, they may be connected to VDD through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

**Figure 7: TAP Controller State Diagram**




NOTE:

The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

### *Test Access Port (TAP)*

### *Test Clock (TCK)*

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

### *Test MODE SELECT (TMS)*

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

### *Test Data-In (TDI)*

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 7. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register, as illustrated in Figure 8.


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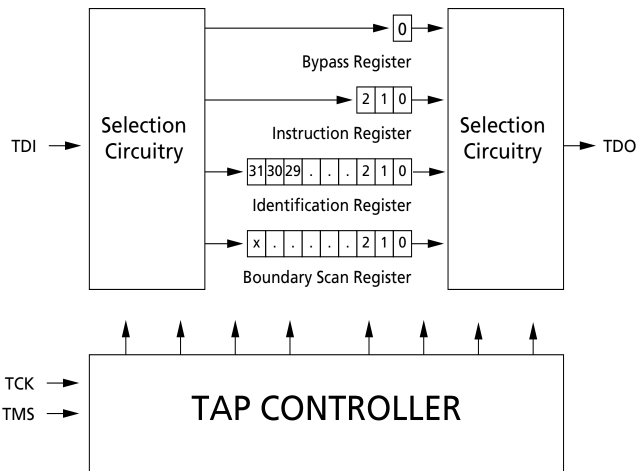
**Figure 8:**
**TAP Controller Block Diagram**




NOTE:
X = 106.

## Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine, as shown in Figure 7. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register, as depicted in Figure 8.

## Performing a TAP RESET

A RESET is performed by forcing TMS HIGH (VDD) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

## TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

## Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls, as shown in Figure 8. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two LSBs are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

## Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (Vss) when the BYPASS instruction is executed.

## Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. The SRAM has a 107-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the balls on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

## Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.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### TAP Instruction Set Overview

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

### EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller; therefore, this device is not 1149.1-compliant.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. EXTEST does not place the SRAM outputs (including CQ and CQ#) in a High-Z state.

### IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

### SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

### SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1-compliant.

Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

### BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

### Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.


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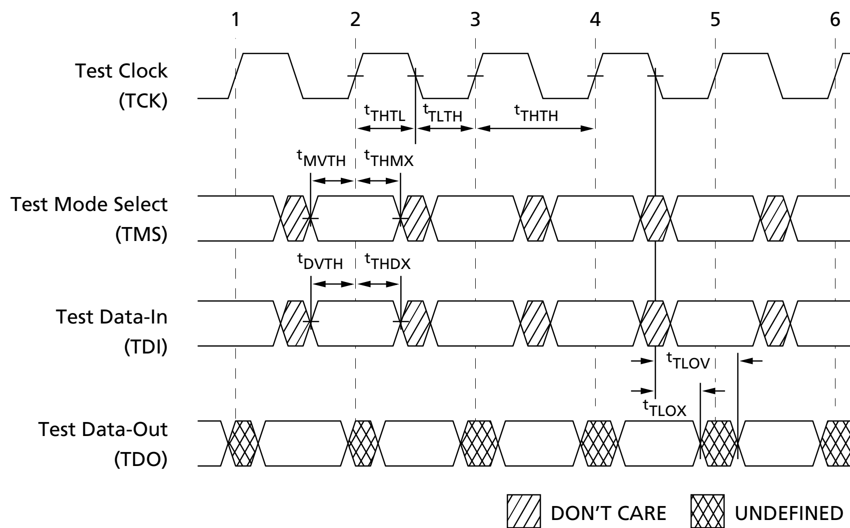
## Figure 9: TAP Timing




NOTE:

Timing for SRAM inputs and outputs is congruent with TDI and TDO, respectively, as shown in Figure 9.

## Table 14: TAP AC Electrical Characteristics

Notes 1, 2; 0°C ≤ $T_A$ ≤ +70°C; VDD = 2.5V ±0.1V

| DESCRIPTION | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|
| **Clock** | | | | |
| Clock cycle time | $^tTHTH$ | 100 | | ns |
| Clock frequency | $^fTF$ | | 10 | MHz |
| Clock HIGH time | $^tTHTL$ | 40 | | ns |
| Clock LOW time | $^tTLTH$ | 40 | | ns |
| **Output Times** | | | | |
| TCK LOW to TDO unknown | $^tTLOX$ | 0 | | ns |
| TCK LOW to TDO valid | $^tTLOV$ | | 20 | ns |
| TDI valid to TCK HIGH | $^tDVTH$ | 10 | | ns |
| TCK HIGH to TDI invalid | $^tTHDX$ | 10 | | ns |
| **Setup Times** | | | | |
| TMS setup | $^tMVTH$ | 10 | | ns |
| Capture setup | $^tCS$ | 10 | | ns |
| **Hold Times** | | | | |
| TMS hold | $^tTHMX$ | 10 | | ns |
| Capture hold | $^tCH$ | 10 | | ns |

NOTE:

1. $^tCS$ and $^tCH$ refer to the setup and hold time requirements of latching data from the boundary scan register.
2. Test conditions are specified using the load in Figure 10.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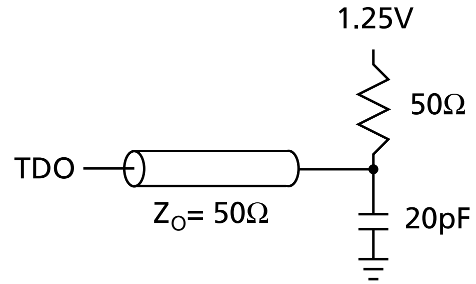
## TAP AC Test Conditions

Input pulse levels . . . . . . . . . . . . . . . . . . . . . . . . . .VSS to 2.5V
Input rise and fall times . . . . . . . . . . . . . . . . . . . . . . . 1ns
Input timing reference levels . . . . . . . . . . . . . . 1.25V
Output reference levels . . . . . . . . . . . . . . . . . . . . . 1.25V
Test load termination supply voltage . . . . . . . . . 1.25V

**Figure 10:**
**TAP AC Output Load Equivalent**




## Table 15: TAP DC Electrical Characteristics and Operating Conditions

Note 2; 0°C ≤ $T_A$ ≤ +70°C; VDD = 2.5V ±0.1V unless otherwise noted

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input High (Logic 1) Voltage | | VIH | 1.7 | VDD + 0.3 | V | 1, 2 |
| Input Low (Logic 0) Voltage | | VIL | -0.3 | 0.7 | V | 1, 2 |
| Input Leakage Current | 0V ≤ VIN ≤ VDD | ILI | -5.0 | 5.0 | µA | 2 |
| Output Leakage Current | Output(s) disabled, 0V ≤ VIN ≤ VDDQ | ILO | -5.0 | 5.0 | µA | 2 |
| Output Low Voltage | IOLC = 100µA | VOL1 | | 0.2 | V | 1, 2 |
| Output Low Voltage | IOLT = 2mA | VOL2 | | 0.7 | V | 1, 2 |
| Output High Voltage | \|IOHC\| = 100µA | VOH1 | 2.1 | | V | 1, 2 |
| Output High Voltage | \|IOHT\| = 2mA | VOH2 | 1.7 | | V | 1, 2 |

NOTE:
1. All voltages referenced to VSS (GND).
2. This table defines DC values for TAP control and data balls only. The DQ SRAM balls used in the JTAG operation will have the same values as defined in Table 8, "DC Electrical Characteristics and Operating Conditions," on page 11.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## Table 16: Identification Register Definitions

| INSTRUCTION FIELD | ALL DEVICES | DESCRIPTION |
|---|---|---|
| REVISION NUMBER (31:28) | 000 | Revision number. |
| DEVICE ID (28:12) | 00def0wx0t0q0b0s0 | def = 010 for 36Mb density<br>def = 001 for 18Mb density<br>def = 000 for 9Mb density<br>wx = 11 for x36 width<br>wx = 10 for x18 width<br>wx = 01 for x8 width<br>t = 1 for DLL version<br>t = 0 for non-DLL version<br>q = 1 for QDR<br>q = 0 for DDR<br>b = 1 for 4-word burst<br>b = 0 for 2-word burst<br>s = 1 for separate I/O<br>s = 0 for common I/O |
| MICRON JEDEC ID CODE (11:1) | 00000101100 | Allows unique identification of SRAM vendor. |
| ID Register Presence Indicator (0) | 1 | Indicates the presence of an ID register. |

## Table 17: Scan Register Size

| REGISTER NAME | BIT SIZE |
|---|---|
| Instruction | 3 |
| Bypass | 1 |
| ID | 32 |
| Boundary Scan | 107 |

## Table 18: Instruction Codes

| INSTRUCTION | CODE | DESCRIPTION |
|---|---|---|
| EXTEST | 000 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This instruction is not 1149.1-compliant. |
| IDCODE | 001 | Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations. |
| SAMPLE Z | 010 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state. |
| RESERVED | 011 | Do Not Use: This instruction is reserved for future use. |
| SAMPLE/PRELOAD | 100 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant. |
| RESERVED | 101 | Do Not Use: This instruction is reserved for future use. |
| RESERVED | 110 | Do Not Use: This instruction is reserved for future use. |
| BYPASS | 111 | Places the bypass register between TDI and TDO. This operation does not affect SRAM operations. |


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## Table 19: Boundary Scan (Exit) Order

| BIT# | FBGA BALL |
|---|---|
| 1 | 6R |
| 2 | 6P |
| 3 | 6N |
| 4 | 7P |
| 5 | 7N |
| 6 | 7R |
| 7 | 8R |
| 8 | 8P |
| 9 | 9R |
| 10 | 11P |
| 11 | 10P |
| 12 | 10N |
| 13 | 9P |
| 14 | 10M |
| 15 | 11N |
| 16 | 9M |
| 17 | 9N |
| 18 | 11L |
| 19 | 11M |
| 20 | 9L |
| 21 | 10L |
| 22 | 11K |
| 23 | 10K |
| 24 | 9J |
| 25 | 9K |
| 26 | 10J |
| 27 | 11J |
| 28 | 11H |
| 29 | 10G |
| 30 | 9G |
| 31 | 11F |
| 32 | 11G |
| 33 | 9F |
| 34 | 10F |
| 35 | 11E |
| 36 | 10E |
| 37 | 10D |
| 38 | 9E |
| 39 | 10C |
| 40 | 11D |
| 41 | 9C |
| 42 | 9D |
| 43 | 11B |
| 44 | 11C |
| 45 | 9B |
| 46 | 10B |
| 47 | 11A |
| 48 | 10A |
| 49 | 9A |
| 50 | 8B |
| 51 | 7C |
| 52 | 6C |
| 53 | 8A |
| 54 | 7A |
| 55 | 7B |
| 56 | 6B |
| 57 | 6A |
| 58 | 5B |
| 59 | 5A |
| 60 | 4A |
| 61 | 5C |
| 62 | 4B |
| 63 | 3A |
| 64 | 2A |
| 65 | 1A |
| 66 | 2B |
| 67 | 3B |
| 68 | 1C |
| 69 | 1B |
| 70 | 3D |
| 71 | 3C |
| 72 | 1D |
| 73 | 2C |
| 74 | 3E |
| 75 | 2D |
| 76 | 2E |
| 77 | 1E |
| 78 | 2F |
| 79 | 3F |
| 80 | 1G |
| 81 | 1F |
| 82 | 3G |
| 83 | 2G |
| 84 | 1J |
| 85 | 2J |
| 86 | 3K |
| 87 | 3J |
| 88 | 2K |
| 89 | 1K |
| 90 | 2L |
| 91 | 3L |
| 92 | 1M |
| 93 | 1L |
| 94 | 3N |
| 95 | 3M |
| 96 | 1N |
| 97 | 2M |
| 98 | 3P |
| 99 | 2N |
| 100 | 2P |
| 101 | 1P |
| 102 | 3R |
| 103 | 4R |
| 104 | 4P |
| 105 | 5P |
| 106 | 5N |
| 107 | 5R |


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**Figure 11:**
**165-Ball FBGA**

0.85 ±0.075
0.12 C
SEATING PLANE
C
BALL A11
165X Ø 0.45
SOLDER BALL DIAMETER REFERS TO POST REFLOW CONDITION. THE PRE-REFLOW DIAMETER IS Ø 0.40
10.00
1.00 TYP
BALL A1
PIN A1 ID
1.20 MAX
PIN A1 ID
7.50 ±0.05
15.00 ±0.10
14.00
7.00 ±0.05
1.00 TYP
6.50 ±0.05
5.00 ±0.05
13.00 ±0.10
MOLD COMPOUND: EPOXY NOVOLAC
SUBSTRATE: PLASTIC LAMINATE
SOLDER BALL MATERIAL:
EUTECTIC 62% Sn, 36% Pb, 2% Ag
SOLDER BALL PAD: Ø .33mm

NOTE:
1. All dimensions are in millimeters.

## Data Sheet Designation

**No Marking:** This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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## Document Revision History

Rev. F, Pub 3/03 ........................................................................ 3/03

- Updated JTAG Section
- Removed Preliminary Status

Rev. E, Pub 2/03 ........................................................................ 2/03

- Added definitive notes to Figure 3
- Added definitive note to Table 9
- Updated Truth Table for clarity
- Added 1.5V references
- Update READ/WRITE Timing Diagram
- Updated JTAG section to reflect 1149.1 specification compliance with EXTEST features
- Updated JTAG description to reflect 1149.1 specification compliance with EXTEST feature
- Added definitive note concerning SRAM (DQ) I/O balls used for JTAG DC values and timing
- Changed process information in header to die revision indicator
- Updated Thermal Resistance Values to Table 12:
  $C_I$ = 4.5 TYP; 5.5 MAX
  $C_O$ = 6 TYP; 7 MAX
  $C_{CK}$ = 5.5 TYP; 6.5 MAX
- Updated Thermal Resistance values to Table 12:
  $J_A$ = 19.4 TYP
  $J_C$ = 1.0 TYP
  $J_B$ = 9.6 TYP
- Added $T_J \leq +95°C$ to Table 13
- Modified Figure 2 regarding depth, configuration, and byte controls
- Added definitive notes regarding I/O behavior during JTAG operation
- Added definitive notes regarding $I_{DD}$ test conditions for read to write ratio
- Removed note regarding AC derating information for full I/O range
- Remove references to JTAG scan chain logic levels being at logic zero for NC pins in Tables 5 and 19
- Revised ball description for NC balls:
  These balls are internally connected to the die, but have no function and may be left not connected to the board to minimize ball count.

Rev. D, Pub 6/02 ........................................................................ 6/02

- Removed ADVANCE designation
- Added note 8 on page 8
- Deleted note 6 on page 9
- Revised note 5 on page 10
- Added "t" and description to Device ID code

Rev. C, Pub. 5/02, ADVANCE ........................................................................ 5/02

- Fixed voltage range error in AC Electrical Characteristics and Operating Conditions table
- Added new Output Times values

Rev. B, Pub. 5/02, ADVANCE ........................................................................ 8/02

- Updated DC Electrical Characteristics and Operating Conditions table
- Added AC Electrical Characteristics and Operating Conditions table

Rev. A, Pub. 4/02, ADVANCE ........................................................................ 4/02

- New ADVANCE data sheet



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