

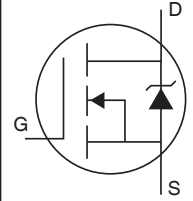
## Applications

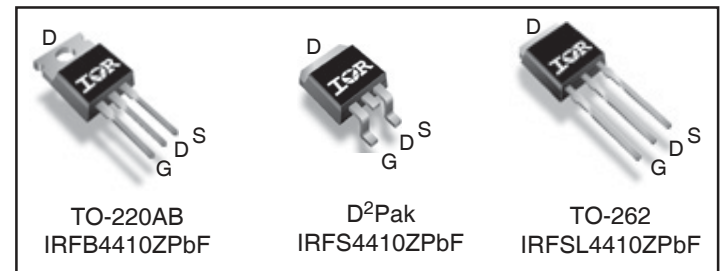
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

## Benefits

- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode  $dV/dt$  and  $dI/dt$  Capability
- Lead-Free
- RoHS Compliant, Halogen-Free

## HEXFET® Power MOSFET

	$V_{DSS}$	<b>100V</b>
	$R_{DS(on)}$ <b>typ.</b>	<b>7.2m<math>\Omega</math></b>
	<b>max.</b>	<b>9.0m<math>\Omega</math></b>
$I_D$ (Silicon Limited)		<b>97A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFB4410ZPbF	TO-220	Tube	50	IRFB4410ZPbF
IRFSL4410ZPbF	TO-262	Tube	50	IRFSL4410ZPbF
IRFS4410ZPbF	D2Pak	Tube	50	IRFS4410ZPbF
		Tape and Reel Left	800	IRFS4410ZTRLpBF
		Tape and Reel Right	800	IRFS4410ZTRRpBF

## Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	97	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	69	
$I_{DM}$	Pulsed Drain Current ①	390	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	230	W
	Linear Derating Factor	1.5	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$dv/dt$	Peak Diode Recovery ③	16	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		
	Mounting torque, 6-32 or M3 screw	300	
		10lb·in (1.1N·m)	

## Avalanche Characteristics

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ②	242	mJ
$I_{AR}$	Avalanche Current	See Fig. 14, 15, 22a, 22b,	A
$E_{AR}$	Repetitive Avalanche Energy ④		mJ

## Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤	—	0.65	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface, TO-220	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, TO-220 ⑥	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount), D²Pak ⑦⑧	—	40	

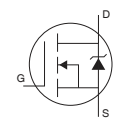
**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 5mA$ ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	7.2	9.0	m $\Omega$	$V_{GS} = 10V, I_D = 58A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 150\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
$R_G$	Internal Gate Resistance	—	0.70	—	$\Omega$	

**Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	140	—	—	S	$V_{DS} = 10V, I_D = 58A$
$Q_g$	Total Gate Charge	—	83	120	nC	$I_D = 58A$ $V_{DS} = 50V$ $V_{GS} = 10V$ ④ $I_D = 58A, V_{DS} = 0V, V_{GS} = 10V$ ④
$Q_{gs}$	Gate-to-Source Charge	—	19	—		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	27	—		
$Q_{sync}$	Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )	—	56	—		
$t_{d(on)}$	Turn-On Delay Time	—	16	—	ns	
$t_r$	Rise Time	—	52	—		$V_{DD} = 65V$ $I_D = 58A$ $R_G = 2.7\Omega$ $V_{GS} = 10V$ ④
$t_{d(off)}$	Turn-Off Delay Time	—	43	—		
$t_f$	Fall Time	—	57	—		
$C_{iss}$	Input Capacitance	—	4820	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	340	—		$V_{DS} = 50V$
$C_{riss}$	Reverse Transfer Capacitance	—	170	—		$f = 1.0\text{MHz}$ , See Fig.5
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related) ⑥	—	420	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V$ ⑦, See Fig.11
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related) ⑤	—	690	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V$ ⑧

**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	97	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	390	A	
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 58A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	38	57	ns	$T_J = 25^\circ\text{C}$
		—	46	69		$T_J = 125^\circ\text{C}$
$Q_{rr}$	Reverse Recovery Charge	—	53	80	nC	$T_J = 25^\circ\text{C}$
		—	82	120		$T_J = 125^\circ\text{C}$
$I_{RRM}$	Reverse Recovery Current	—	2.5	—	A	$T_J = 25^\circ\text{C}$
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.143\text{mH}$   
 $R_G = 25\Omega, I_{AS} = 58A, V_{GS} = 10V$ . Part not recommended for use above this value.
- ③  $I_{SD} \leq 58A, di/dt \leq 610A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss \text{ eff. (TR)}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥  $C_{oss \text{ eff. (ER)}}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧  $R_{\theta}$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .

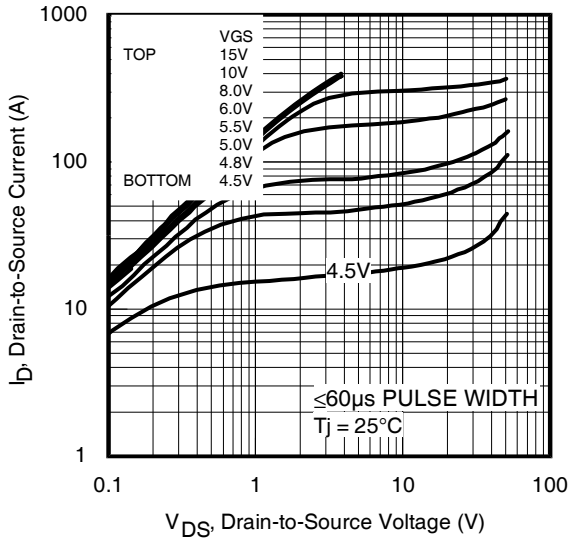


Fig 1. Typical Output Characteristics

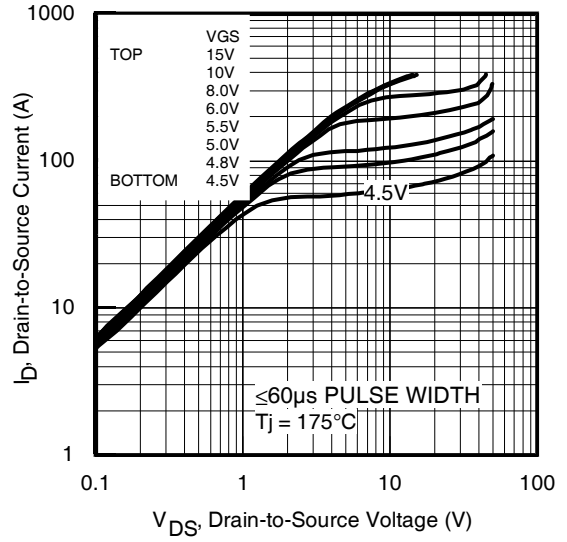


Fig 2. Typical Output Characteristics

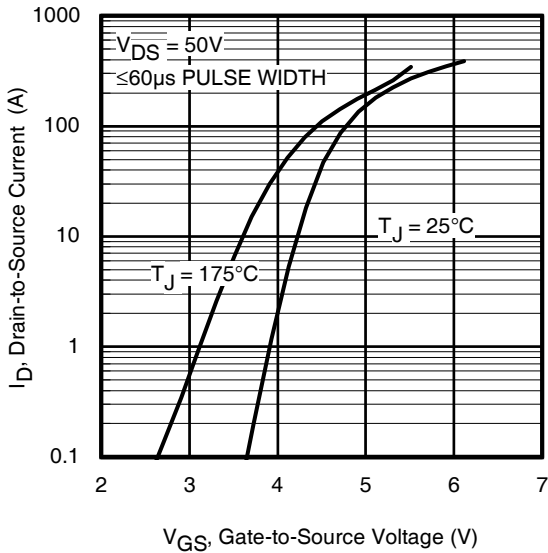


Fig 3. Typical Transfer Characteristics

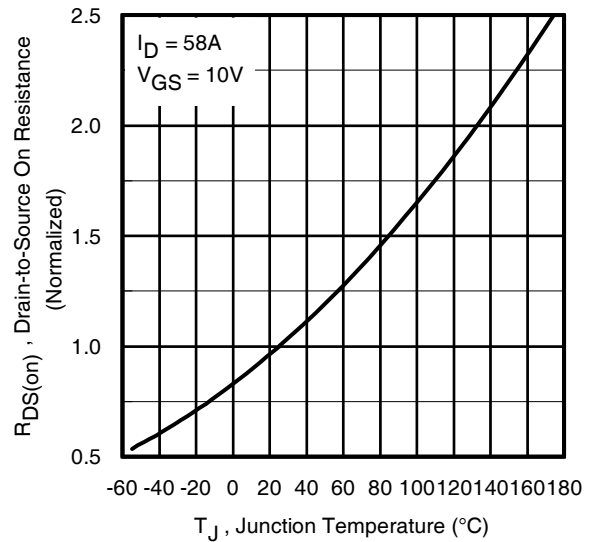


Fig 4. Normalized On-Resistance vs. Temperature

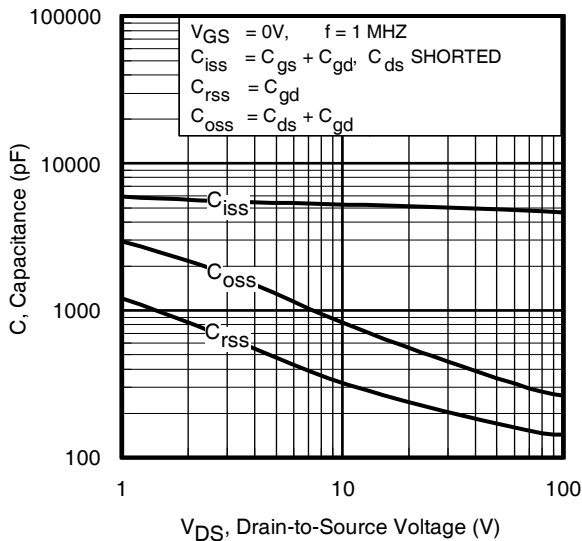


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

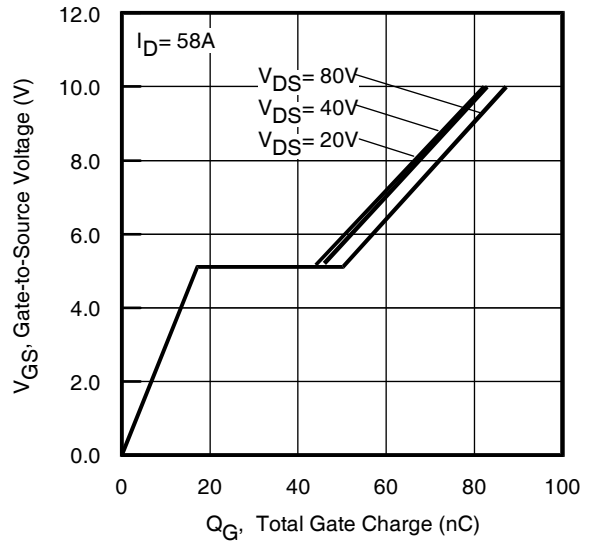
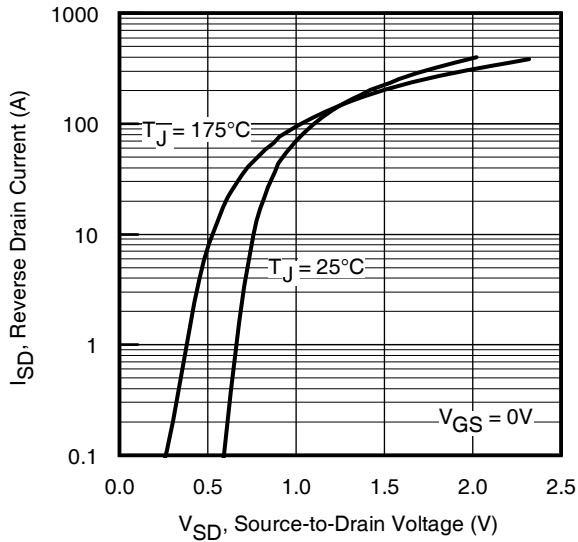
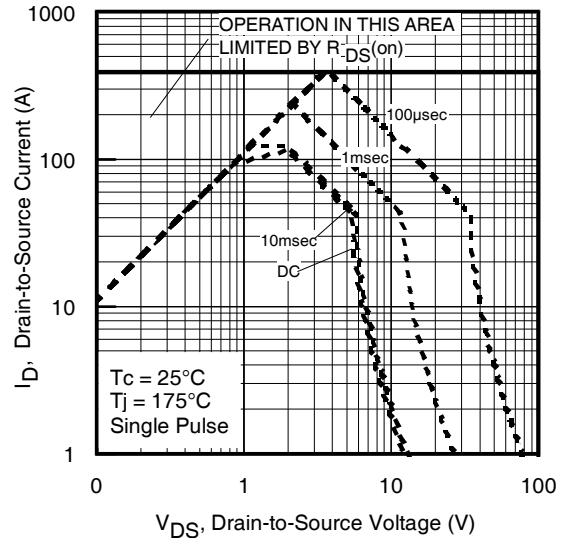


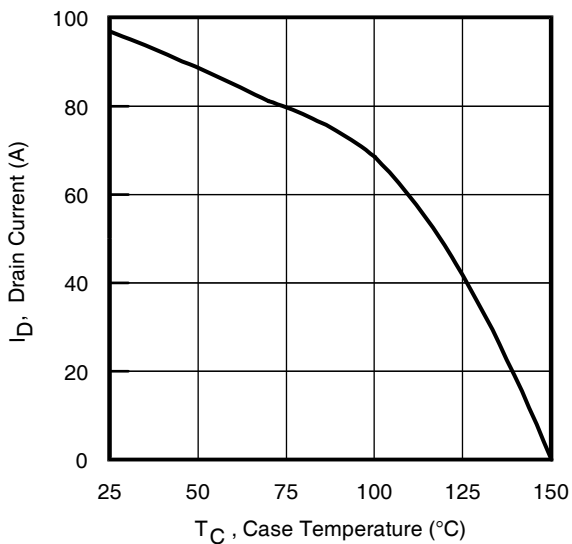
Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage



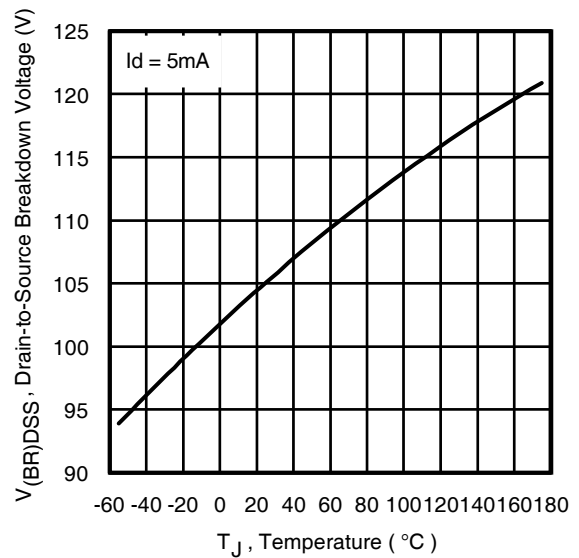
**Fig 7.** Typical Source-Drain Diode Forward Voltage



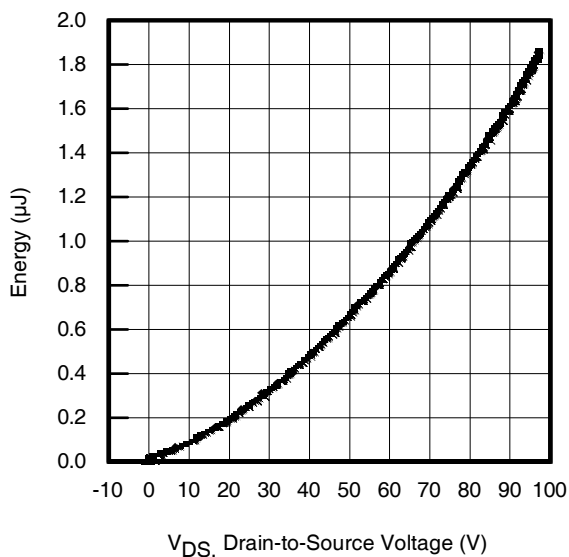
**Fig 8.** Maximum Safe Operating Area



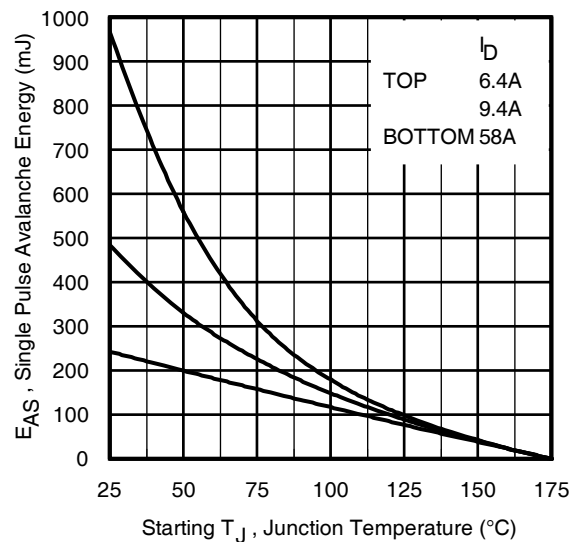
**Fig 9.** Maximum Drain Current vs. Case Temperature



**Fig 10.** Drain-to-Source Breakdown Voltage



**Fig 11.** Typical  $C_{OSS}$  Stored Energy



**Fig 12.** Maximum Avalanche Energy vs. Drain Current

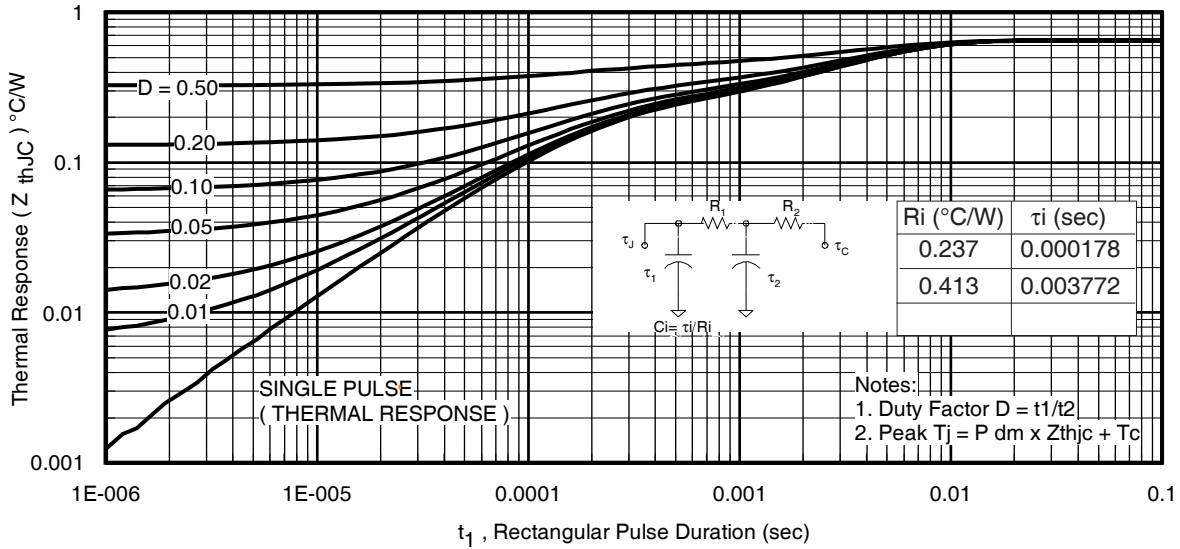


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

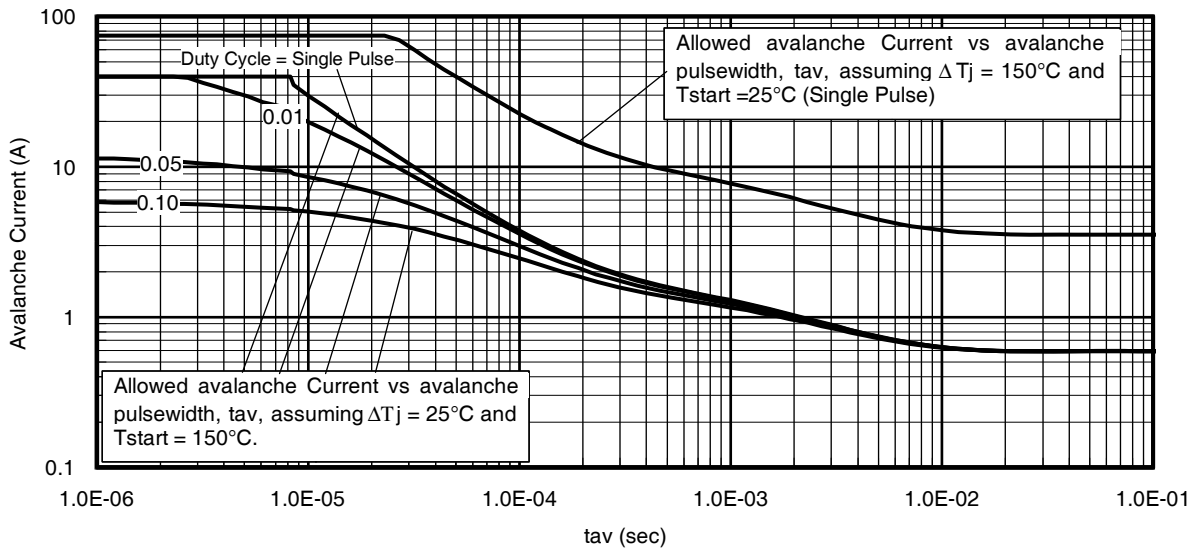
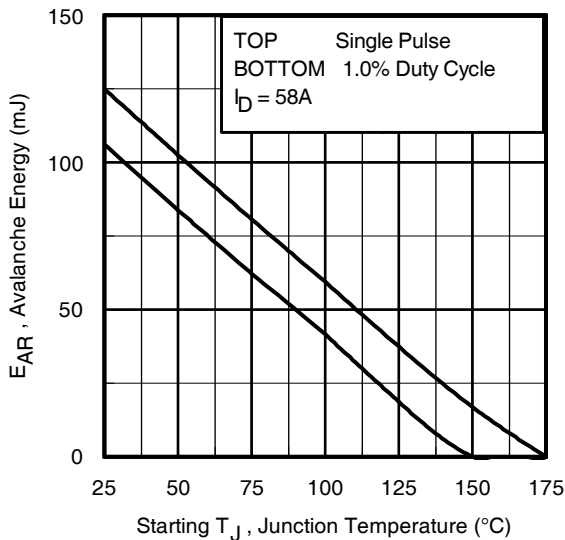


Fig 14. Typical Avalanche Current vs. Pulsewidth



**Notes on Repetitive Avalanche Curves , Figures 14, 15:**  
 (For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
 Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

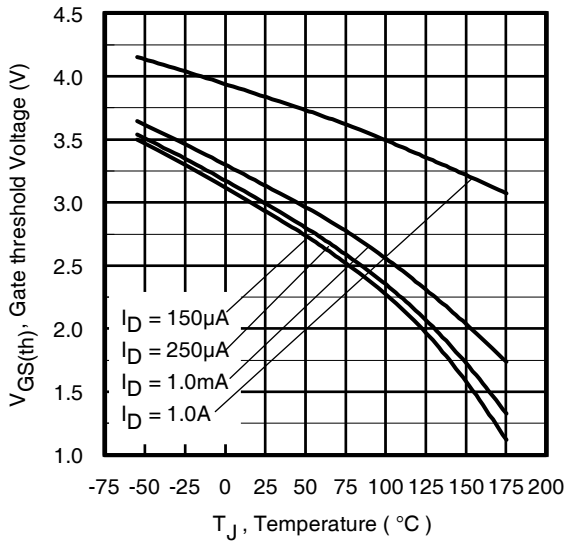


Fig 16. Threshold Voltage vs. Temperature

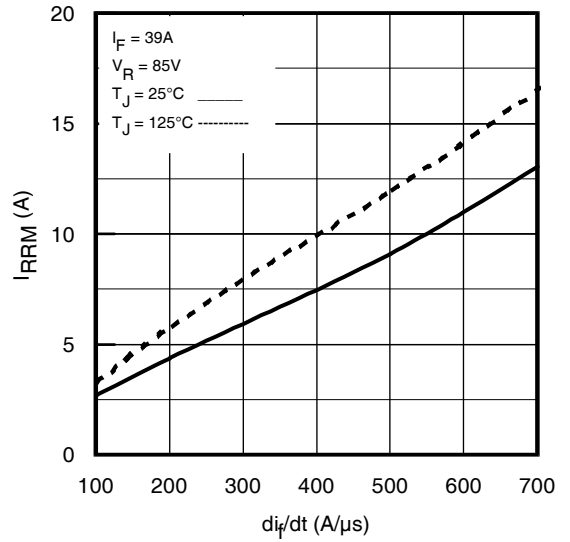


Fig. 17 - Typical Recovery Current vs.  $di_T/dt$

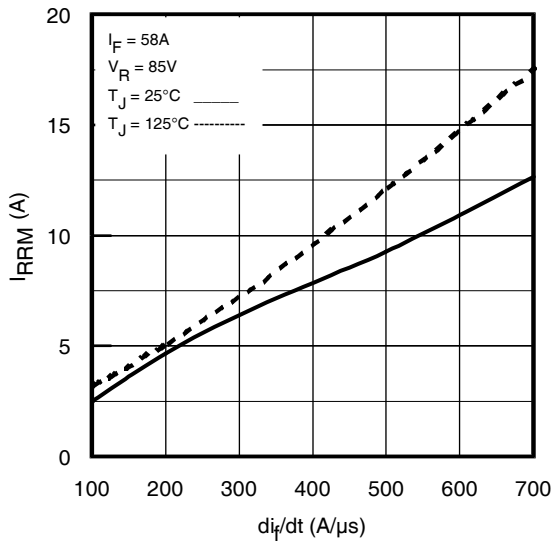


Fig. 18 - Typical Recovery Current vs.  $di_T/dt$

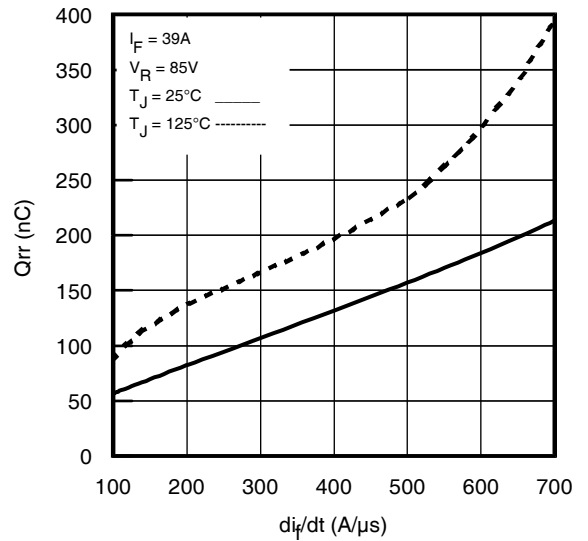


Fig. 19 - Typical Stored Charge vs.  $di_T/dt$

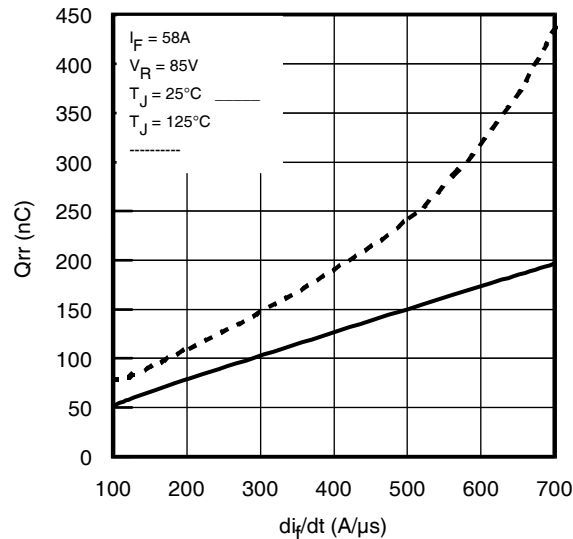
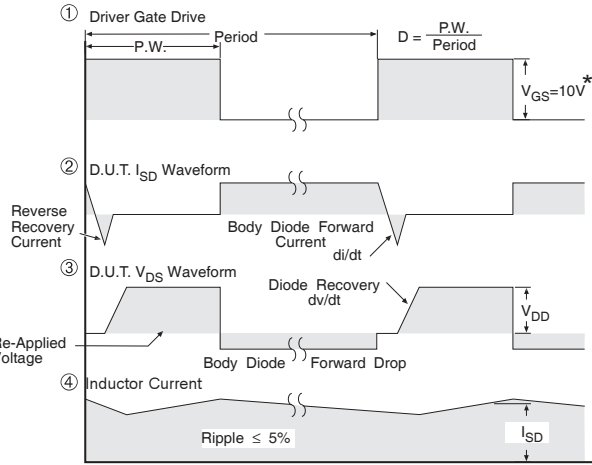
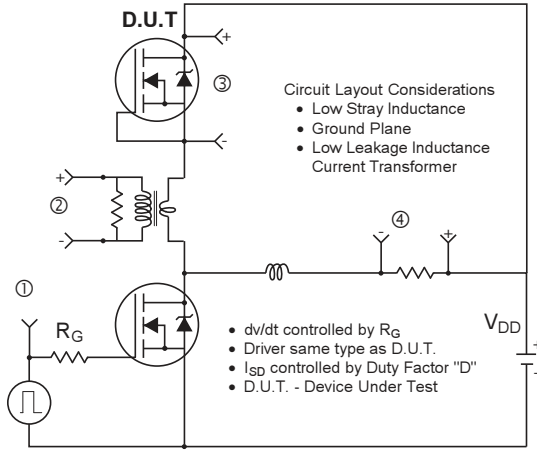
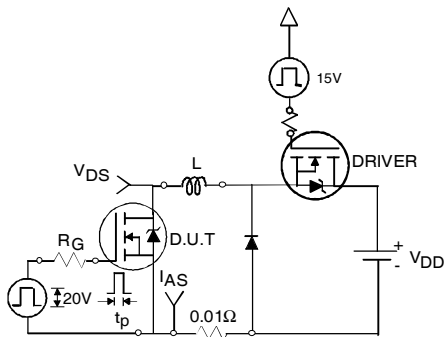


Fig. 20 - Typical Stored Charge vs.  $di_T/dt$

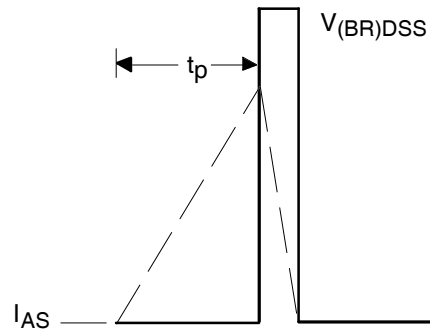


\*  $V_{GS} = 5V$  for Logic Level Devices

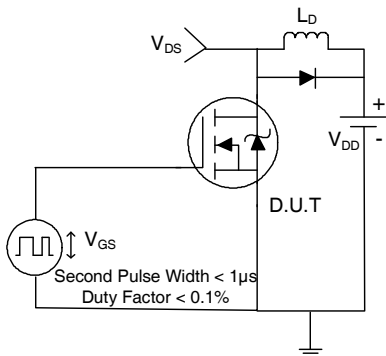
**Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**



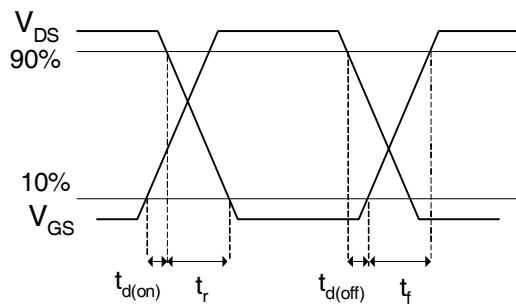
**Fig 22a. Unclamped Inductive Test Circuit**



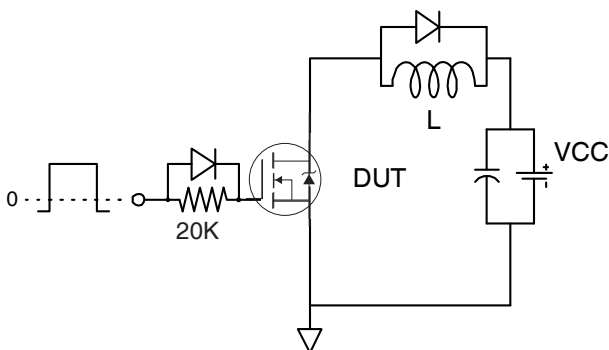
**Fig 22b. Unclamped Inductive Waveforms**



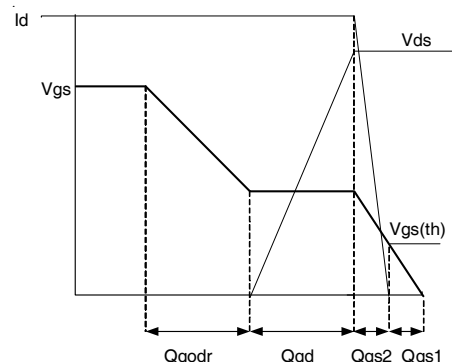
**Fig 23a. Switching Time Test Circuit**



**Fig 23b. Switching Time Waveforms**



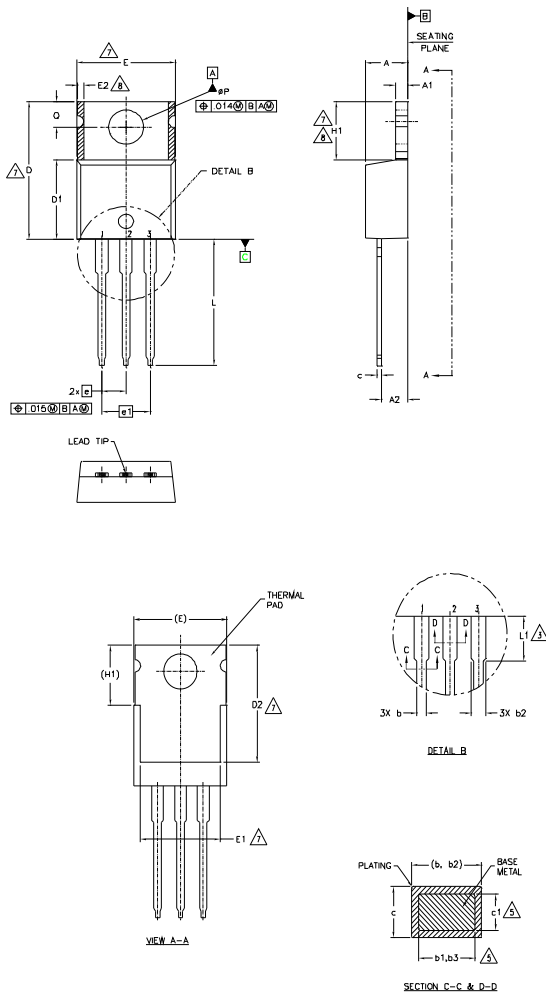
**Fig 24a. Gate Charge Test Circuit**



**Fig 24b. Gate Charge Waveform**

# TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



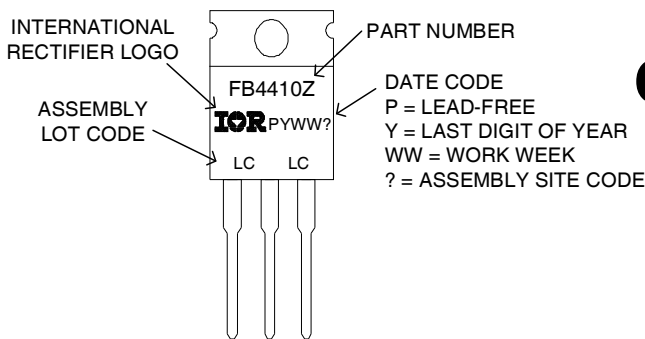
NOTES:

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

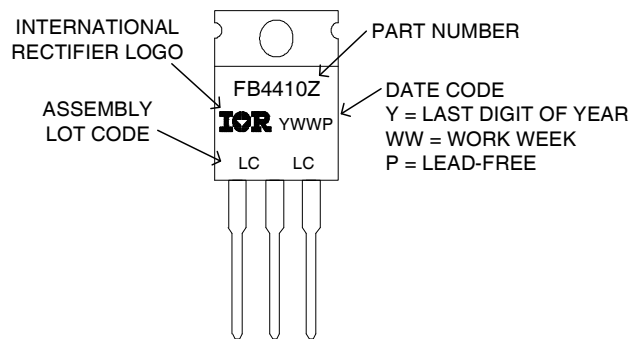
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	1.14	1.40	.045	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

- LEAD ASSIGNMENTS
- HEXFET
- 1.- GATE
  - 2.- DRAIN
  - 3.- SOURCE
- IGBTs, CoPACK
- 1.- GATE
  - 2.- COLLECTOR
  - 3.- EMITTER
- DIODES
- 1.- ANODE
  - 2.- CATHODE
  - 3.- ANODE

## TO-220AB Part Marking Information



OR

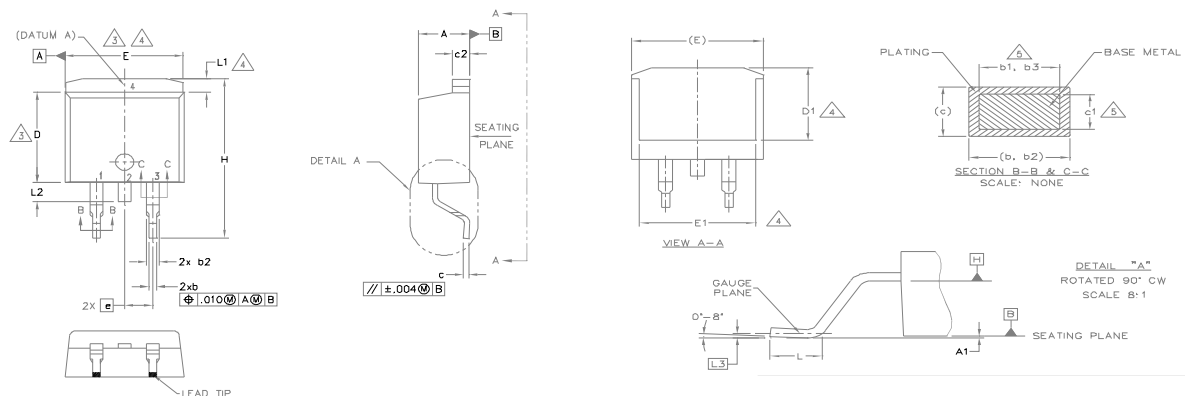


TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>



## D<sup>2</sup>Pak Package Outline (Dimensions are shown in millimeters (inches))



SYM BO L	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	-	1.68	-	.066	4
L2	-	1.78	-	.070	
L3	0.25 BSC		.010 BSC		

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [“.005”] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

**LEAD ASSIGNMENTS**

**DIODES**

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.- CATHODE
- 3.- ANODE

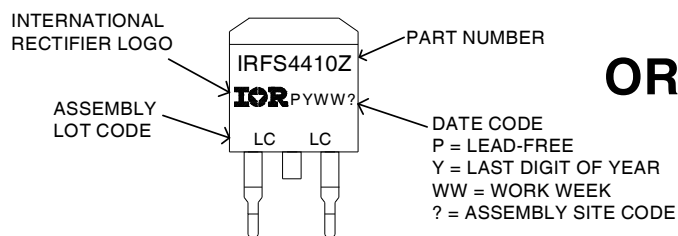
**HEXFET**

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

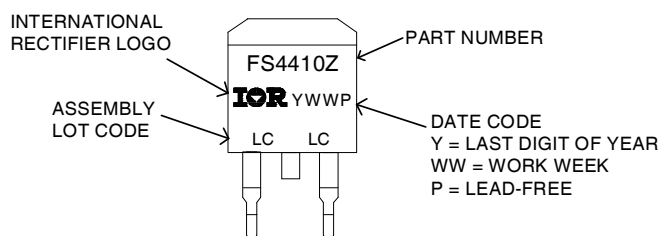
**IGBTs, CoPACK**

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

## D<sup>2</sup>Pak Part Marking Information

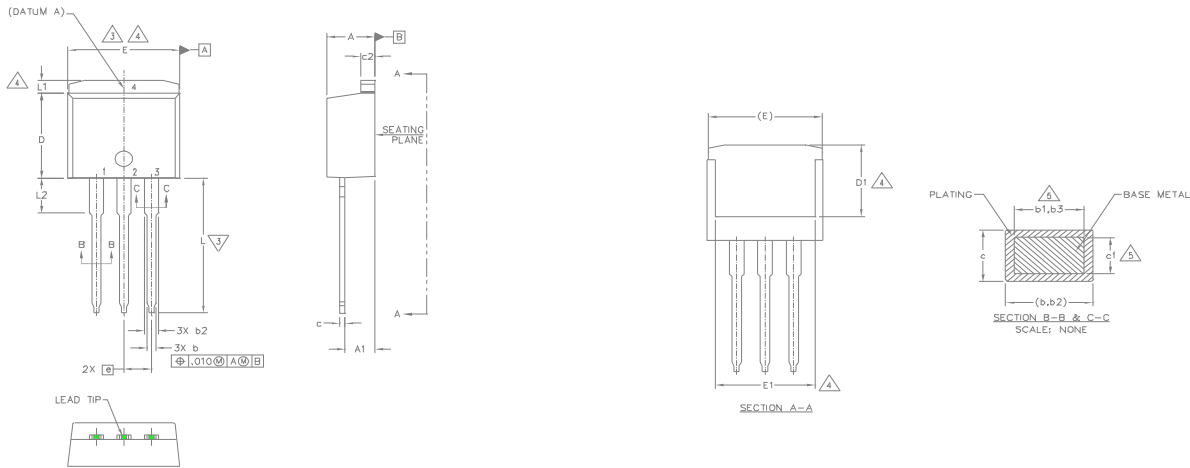


OR



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

## TO-262 Package Outline (Dimensions are shown in millimeters (inches))



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54	BSC	.100	BSC	
L	13.46	14.10	.530	.555	
L1	-	1.65	-	.065	4
L2	3.56	3.71	.140	.146	

**NOTES:**

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
- DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
- CONTROLLING DIMENSION: INCH.
- OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

**LEAD ASSIGNMENTS**

**IGBTs, CoPACK**

- GATE
- COLLECTOR
- EMITTER
- COLLECTOR

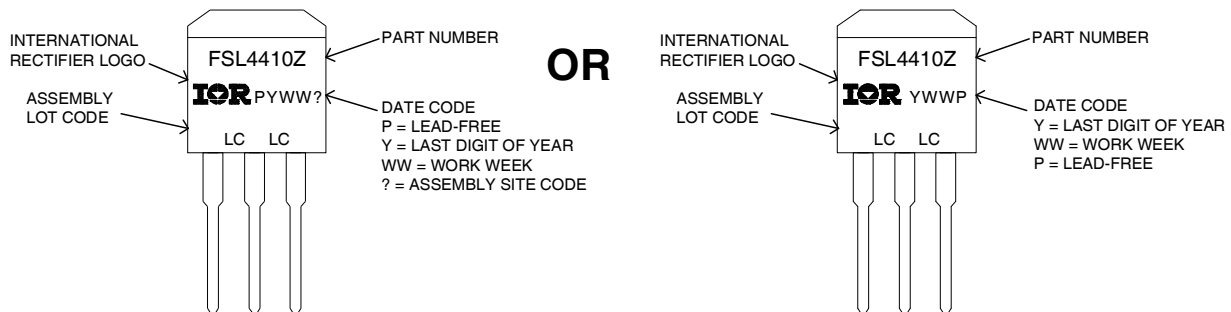
**HEXFET**

- GATE
- DRAIN
- SOURCE
- DRAIN

**DIODES**

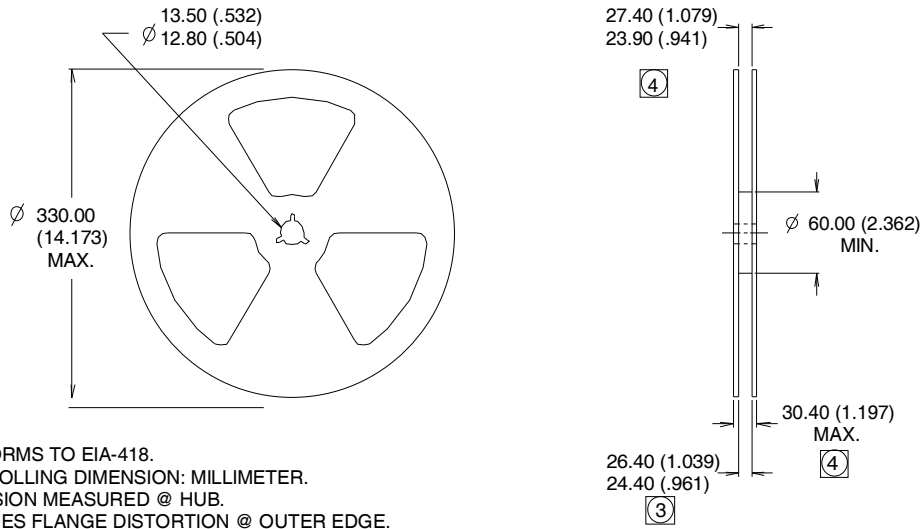
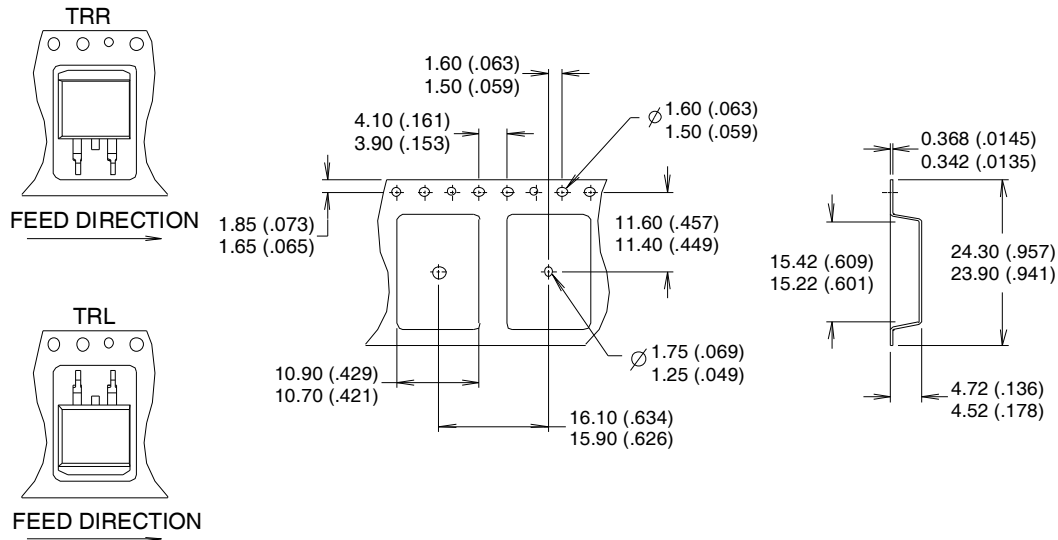
- ANODE (TWO DIE) / OPEN (ONE DIE)
- CATHODE
- ANODE

## TO-262 Part Marking Information



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

## D<sup>2</sup>Pak Tape & Reel Information



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

**Qualification information**<sup>†</sup>

Qualification level	Industrial	
	(per JEDEC JESD47F <sup>††</sup> guidelines)	
Moisture Sensitivity Level	TO-220	N/A
	D2Pak	MSL1
	TO-262	
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comment
4/25/2014	<ul style="list-style-type: none"> <li>• Updated data sheet with new IR corporate template.</li> <li>• Updated package outline &amp; part marking on page 8, 9 &amp; 10.</li> <li>• Added bullet point in the Benefits "RoHS Compliant, Halogen -Free" on page 1.</li> </ul>

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