

PHB95NQ04LT

N-channel TrenchMOS™ logic level FET

Rev. 01 — 11 May 2004

Product data

1. Product profile

1.1 Description

Logic level N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Logic level threshold
- Low on-state resistance.

1.3 Applications

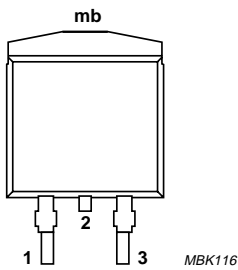
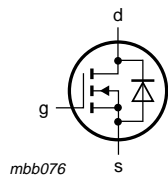
- Motors, lamps, solenoids
- DC-to-DC converters
- Uninterruptible power supplies
- General industrial applications.

1.4 Quick reference data

- $V_{DS} \leq 40$ V
- $I_D \leq 75$ A
- $P_{tot} \leq 157$ W
- $R_{DSon} \leq 7$ m Ω .

2. Pinning information

Table 1: Pinning - SOT404 (D²-PAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d) ^[1]		
3	source (s)		
mb	mounting base; connected to drain (d)	SOT404 (D²-PAK)	

[1] It is not possible to make connection to pin 2 of the SOT404 package.



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3. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
PHB95NQ04LT	D ² -PAK	Plastic single-ended surface mounted package; 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

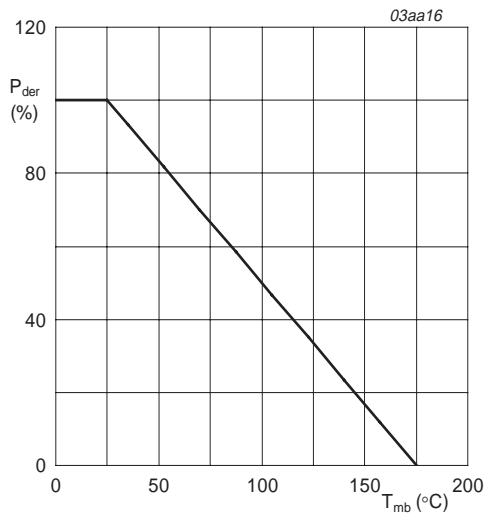
Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage (DC)	25 °C ≤ T _j ≤ 175 °C	-	40	V
V _{DGR}	drain-gate voltage (DC)	25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	40	V
V _{GS}	gate-source voltage (DC)		-	±15	V
I _D	drain current (DC)	T _{mb} = 25 °C; V _{GS} = 10 V; Figure 2 and 3	-	75	A
		T _{mb} = 100 °C; V _{GS} = 10 V; Figure 2	-	75	A
I _{DM}	peak drain current	T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs; Figure 3	-	240	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Figure 1	-	157	W
T _{stg}	storage temperature		-55	+175	°C
T _j	junction temperature		-55	+175	°C

Source-drain diode

I _S	source (diode forward) current (DC)	T _{mb} = 25 °C	-	75	A
I _{SM}	peak source (diode forward) current	T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs	-	240	A

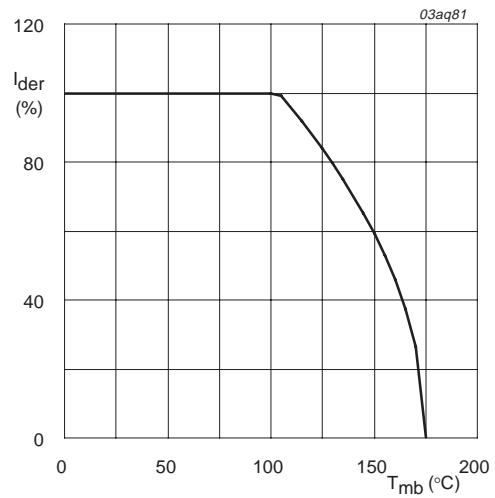
Avalanche ruggedness

E _{DS(AL)S}	non-repetitive drain-source avalanche energy	unclamped inductive load; I _D = 45 A; t _p = 0.17 ms; V _{DD} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; starting T _j = 25 °C	-	200	mJ
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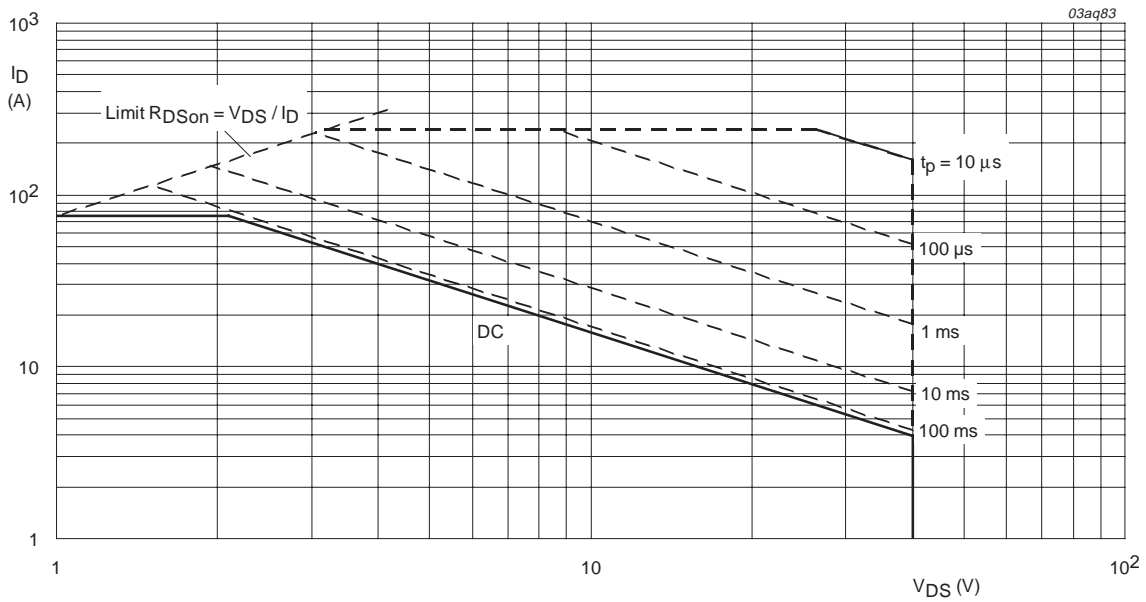
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse; $V_{GS} = 10 V$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.95	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	50	-	K/W

5.1 Transient thermal impedance

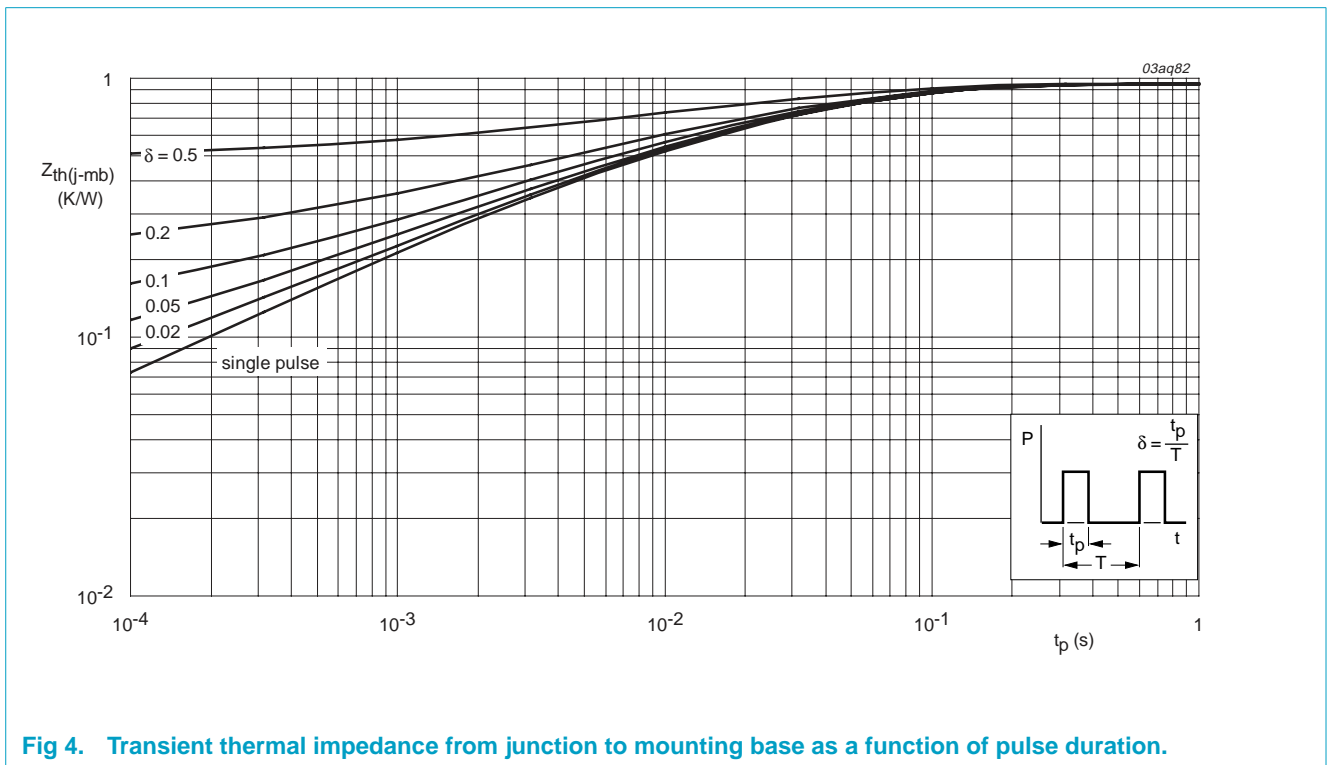


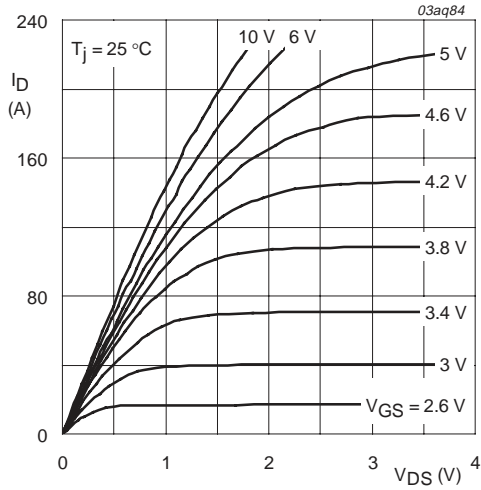
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

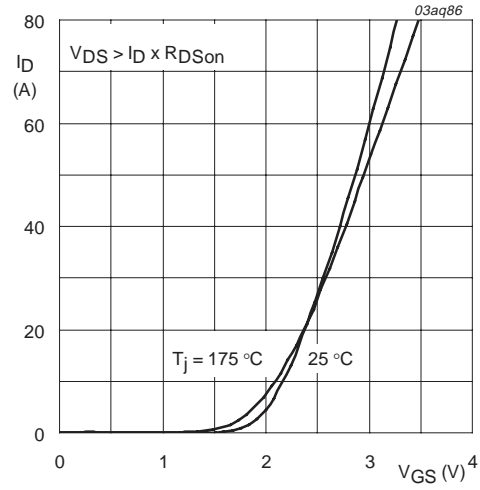
$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	40	-	-	V
		$T_j = -55\text{ °C}$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; Figure 9 and 10 $T_j = 25\text{ °C}$	1	1.5	2	V
		$T_j = 175\text{ °C}$	0.5	-	-	V
		$T_j = -55\text{ °C}$	-	-	2.2	V
I_{DSS}	drain-source leakage current	$V_{DS} = 40\ \text{V}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	-	-	1	μA
		$T_j = 175\text{ °C}$	-	-	500	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 15\ \text{V}$; $V_{DS} = 0\ \text{V}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$; $I_D = 25\ \text{A}$; Figure 7 and 8 $T_j = 25\text{ °C}$	-	6.2	7	m Ω
		$T_j = 175\text{ °C}$	-	11.8	13.3	m Ω
		$V_{GS} = 5\ \text{V}$; $I_D = 25\ \text{A}$; Figure 7 and 8	-	7.6	9	m Ω
		$V_{GS} = 4.5\ \text{V}$; $I_D = 25\ \text{A}$	-	-	10	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 25\ \text{A}$; $V_{DD} = 32\ \text{V}$; $V_{GS} = 5\ \text{V}$; Figure 13	-	32.7	-	nC
Q_{gs}	gate-source charge		-	7.2	-	nC
Q_{gd}	gate-drain (Miller) charge		-	12.4	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}$; $V_{DS} = 25\ \text{V}$; $f = 1\ \text{MHz}$; Figure 11	-	2700	-	pF
C_{oss}	output capacitance		-	450	-	pF
C_{rss}	reverse transfer capacitance		-	210	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 30\ \text{V}$; $R_G = 1.2\ \Omega$; $V_{GS} = 5\ \text{V}$; $R_G = 10\ \Omega$	-	29	-	ns
t_r	rise time		-	106	-	ns
$t_{d(off)}$	turn-off delay time		-	108	-	ns
t_f	fall time		-	89	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 25\ \text{A}$; $V_{GS} = 0\ \text{V}$; Figure 12	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\ \text{A}$; $dI_S/dt = -100\ \text{A}/\mu\text{s}$;	-	57	-	ns
Q_r	recovered charge	$V_{GS} = 0\ \text{V}$; $V_R = 30\ \text{V}$	-	47	-	nC



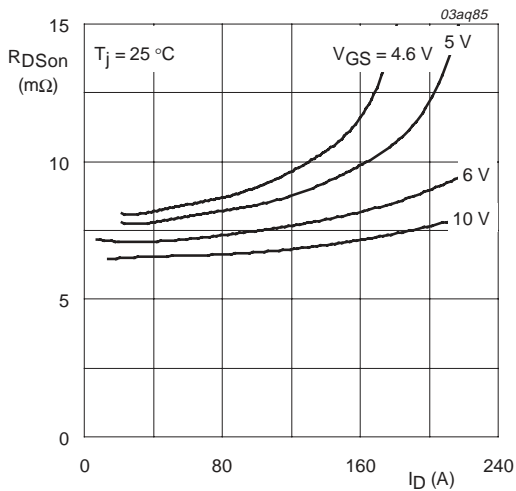
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



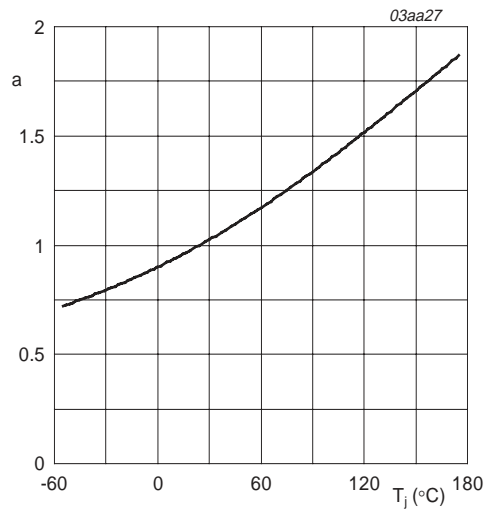
$T_j = 25\text{ }^\circ\text{C}$ and $175\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



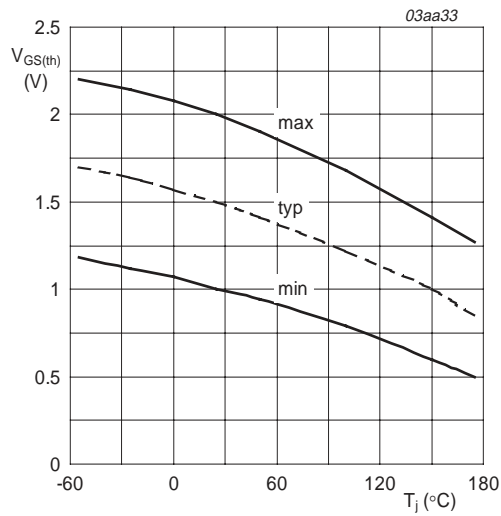
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



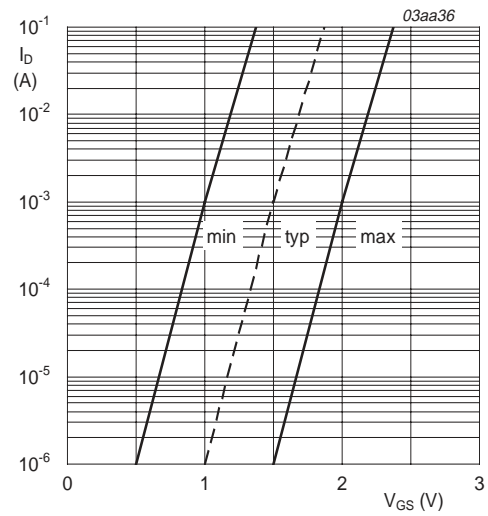
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



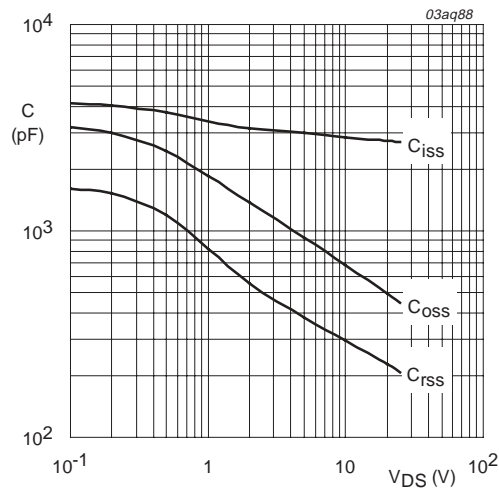
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



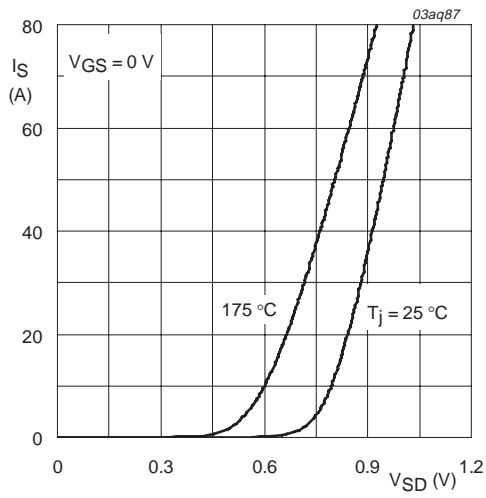
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



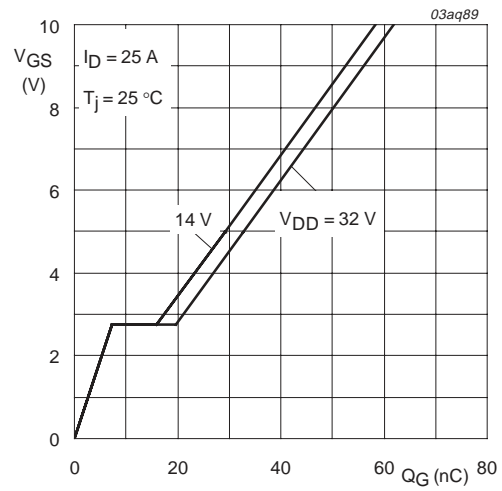
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25$ °C and 175 °C; $V_{GS} = 0$ V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 25$ A; $V_{DD} = 14$ V and 32 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

Plastic single-ended surface mounted package (Philips version of D²-PAK); 3 leads (one lead cropped)

SOT404

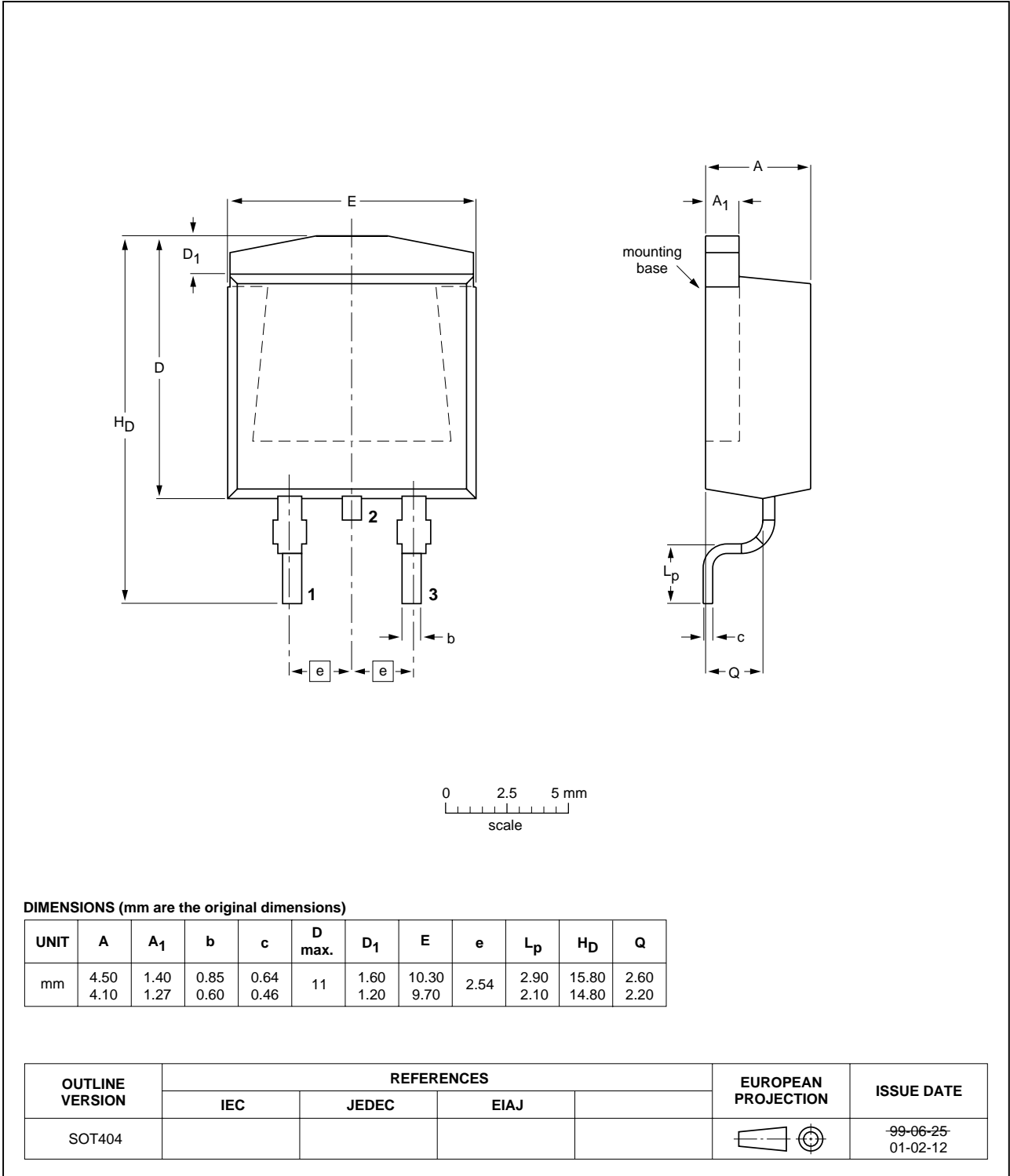


Fig 14. SOT404 (D²-PAK).

8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20040511	-	Product data (9397 750 13166)

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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