

MOSFET

700V CoolMOS™ CE Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE is a price-performance optimized platform enabling to target cost sensitive applications in Consumer and Lighting markets by still meeting highest efficiency standards. The new series provides all benefits of a fast switching Superjunction MOSFET while not sacrificing ease of use and offering the best cost down performance ratio available on the market.

PG - TO220 FullPAK WideCreepage



Features

- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and Eoss
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for standard grade applications

Applications

Adapter, LCD & PDP TV and Indoor lighting

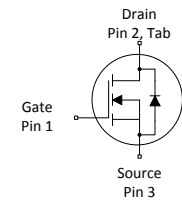


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	750	V
$R_{DS(on),max}$	950	mΩ
$Q_{g,typ}$	15.3	nC
I_d	7.4	A
$I_{D,pulse}$	12	A
$E_{oss@400V}$	1.5	μJ



Type / Ordering Code	Package	Marking	Related Links
IPAW70R950CE	PG - TO220 FullPAK WideCreepage	70S950CE	see Appendix A

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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	7.4 4.7	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	12	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	50	mJ	$I_D=1\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.15	mJ	$I_D=1\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, repetitive	I_{AR}	-	-	1.0	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS}=0\dots480\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation (TO252)	P_{tot}	-	-	68	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-40	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-40	-	150	$^\circ\text{C}$	-
Continuous diode forward current	I_S	-	-	5.2	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	12	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di _f /dt	-	-	500	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8
Power dissipation (FullPAK) TO-220	P_{tot}	-	-	33	W	-
Insulation withstand voltage for TO-220FP	V_{ISO}	-	-	2500	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$. Maximum duty cycle $D=0.5$, TO252 equivalent

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics (Full PAK)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.8	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	700	-	-	V	$V_{GS}=0\text{V}$, $I_D=1\text{mA}$
Gate threshold voltage	$V_{(GS)th}$	2.5	3.0	3.5	V	$V_{DS}=V_{GS}$, $I_D=0.15\text{mA}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=700\text{V}$, $V_{GS}=0\text{V}$, $T_j=25^\circ\text{C}$ $V_{DS}=700\text{V}$, $V_{GS}=0\text{V}$, $T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{V}$, $V_{DS}=0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.86	0.95	Ω	$V_{GS}=10\text{V}$, $I_D=1.5\text{A}$, $T_j=25^\circ\text{C}$ $V_{GS}=10\text{V}$, $I_D=1.5\text{A}$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	5.5	-	Ω	$f=1\text{MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	328	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=100\text{V}$, $f=1\text{MHz}$
Output capacitance	C_{oss}	-	23	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=100\text{V}$, $f=1\text{MHz}$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	14	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=0\dots480\text{V}$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	58.5	-	pF	$I_D=\text{constant}$, $V_{GS}=0\text{V}$, $V_{DS}=0\dots480\text{V}$
Turn-on delay time	$t_{d(on)}$	-	6.6	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=2.2\text{A}$, $R_G=10.2\Omega$; see table 9
Rise time	t_r	-	5.2	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=2.2\text{A}$, $R_G=10.2\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	41	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=2.2\text{A}$, $R_G=10.2\Omega$; see table 9
Fall time	t_f	-	13.6	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=2.2\text{A}$, $R_G=10.2\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{GS}	-	1.8	-	nC	$V_{DD}=480\text{V}$, $I_D=2.2\text{A}$, $V_{GS}=0$ to 10V
Gate to drain charge	Q_{gd}	-	8	-	nC	$V_{DD}=480\text{V}$, $I_D=2.2\text{A}$, $V_{GS}=0$ to 10V
Gate charge total	Q_g	-	15.3	-	nC	$V_{DD}=480\text{V}$, $I_D=2.2\text{A}$, $V_{GS}=0$ to 10V
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	$V_{DD}=480\text{V}$, $I_D=2.2\text{A}$, $V_{GS}=0$ to 10V

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 480V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 480V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V, I_F=2.2A, T_j=25^\circ C$
Reverse recovery time	t_{rr}	-	226	-	ns	$V_R=400V, I_F=2.2A, di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	1.3	-	μC	$V_R=400V, I_F=2.2A, di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	9.9	-	A	$V_R=400V, I_F=2.2A, di_F/dt=100A/\mu s$; see table 8

4 Electrical characteristics diagrams

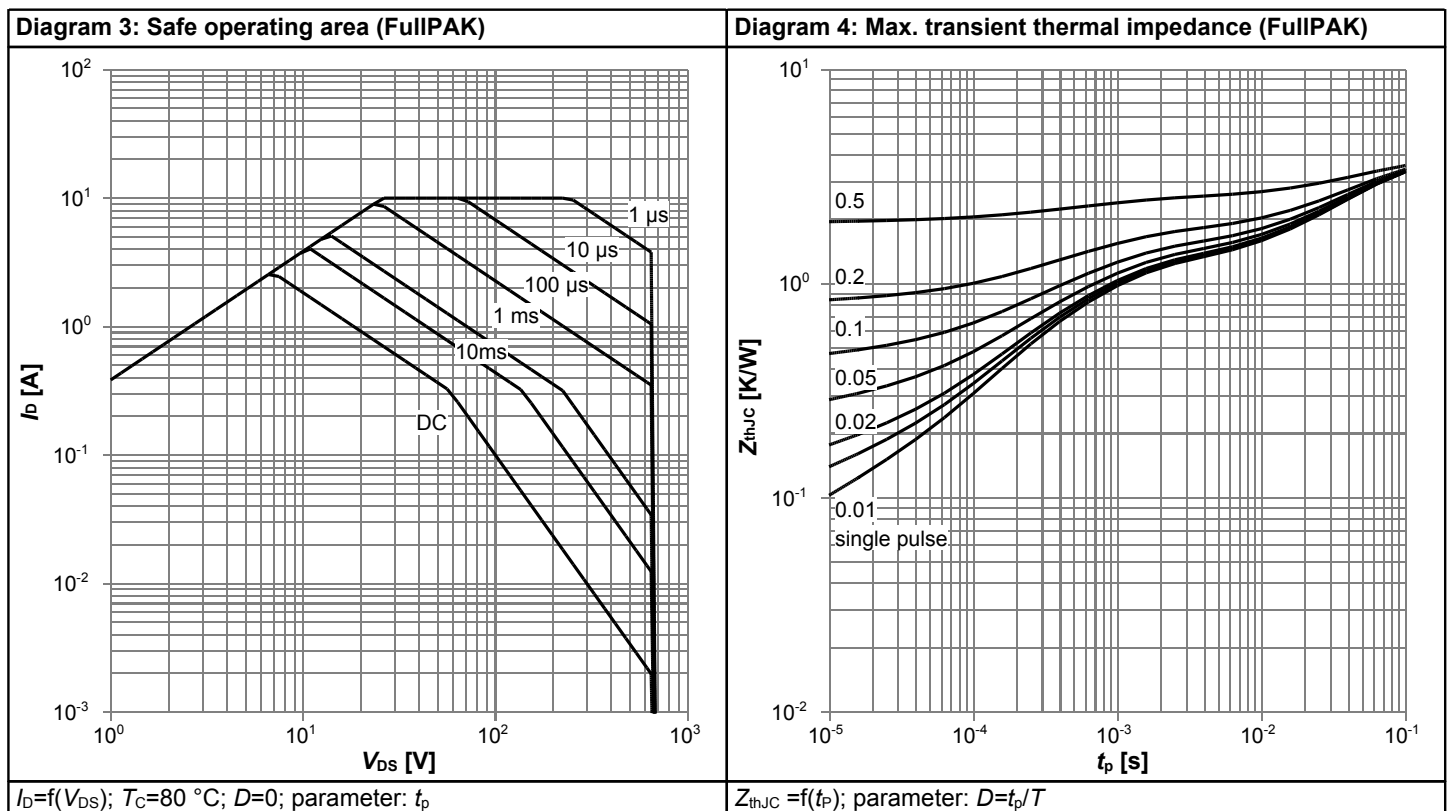
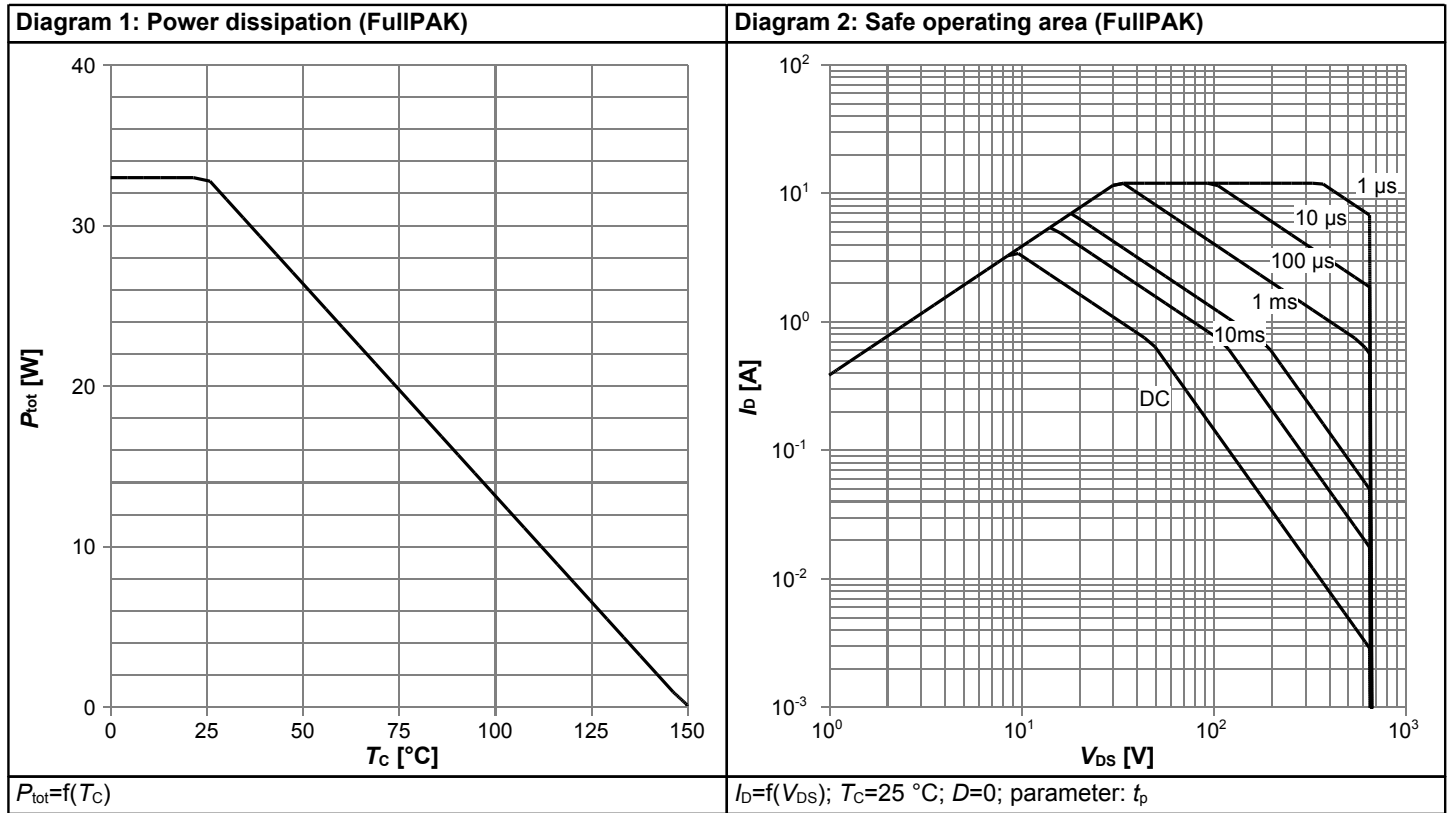
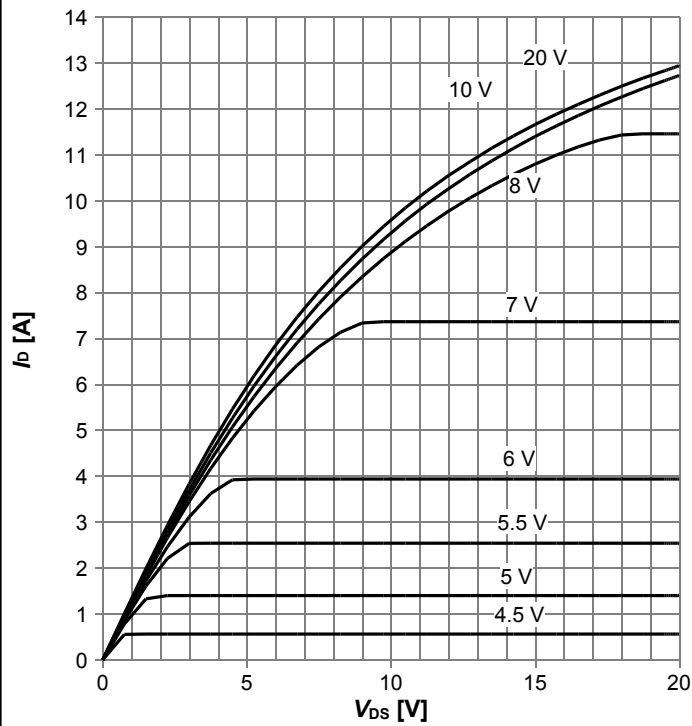
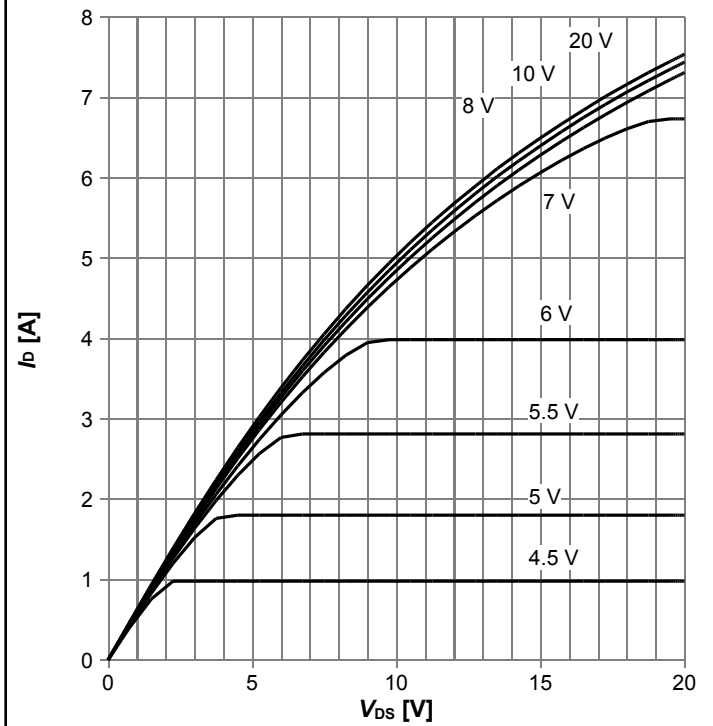


Diagram 5: Typ. output characteristics



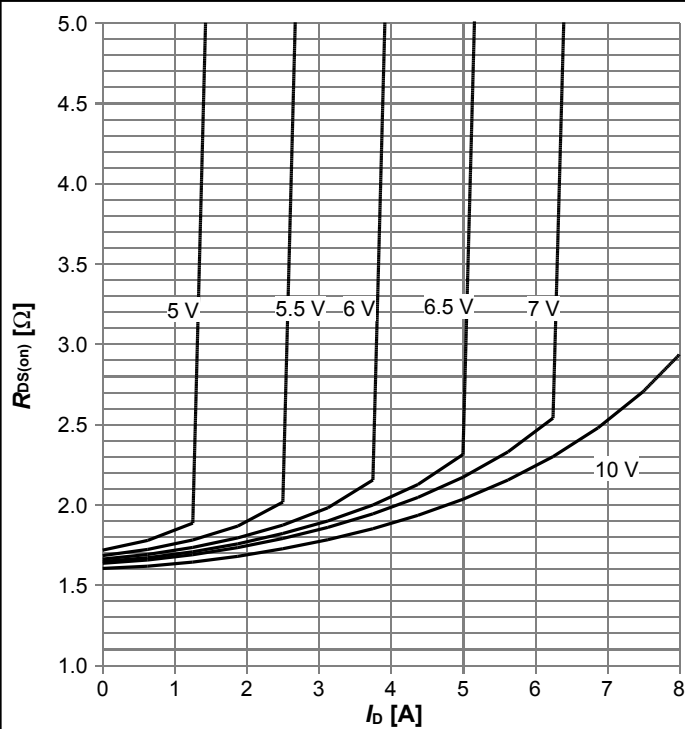
$I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



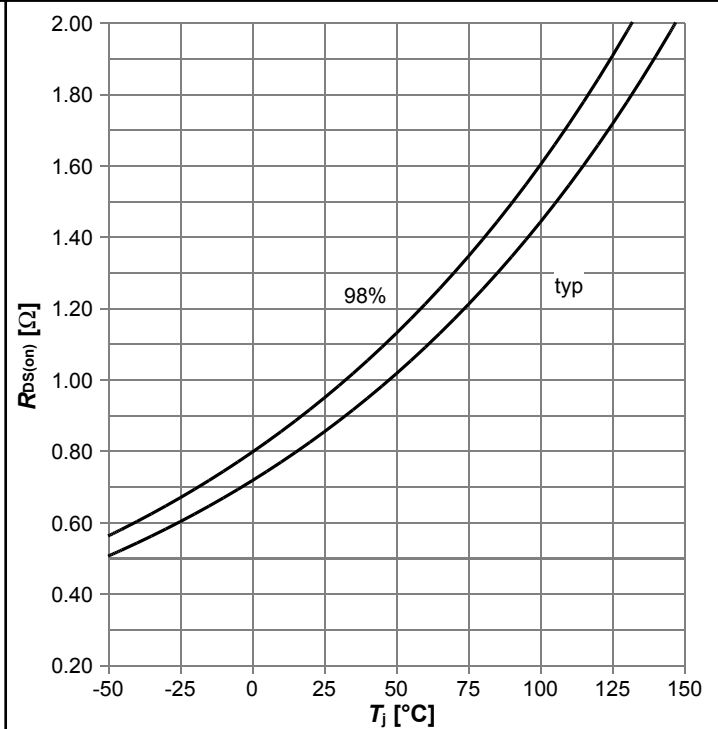
$I_D = f(V_{DS})$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



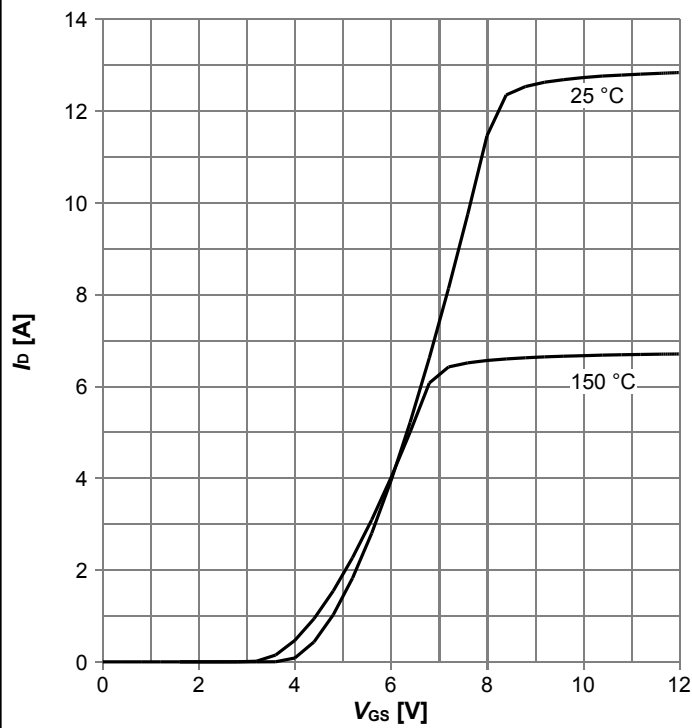
$R_{DS(on)} = f(I_D)$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



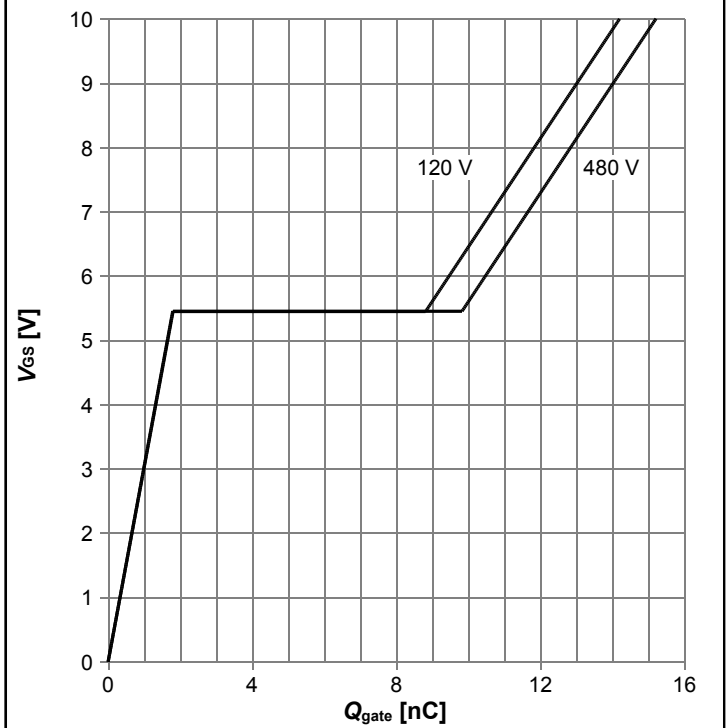
$R_{DS(on)} = f(T_j)$; $I_D = 1.5\text{ A}$; $V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics



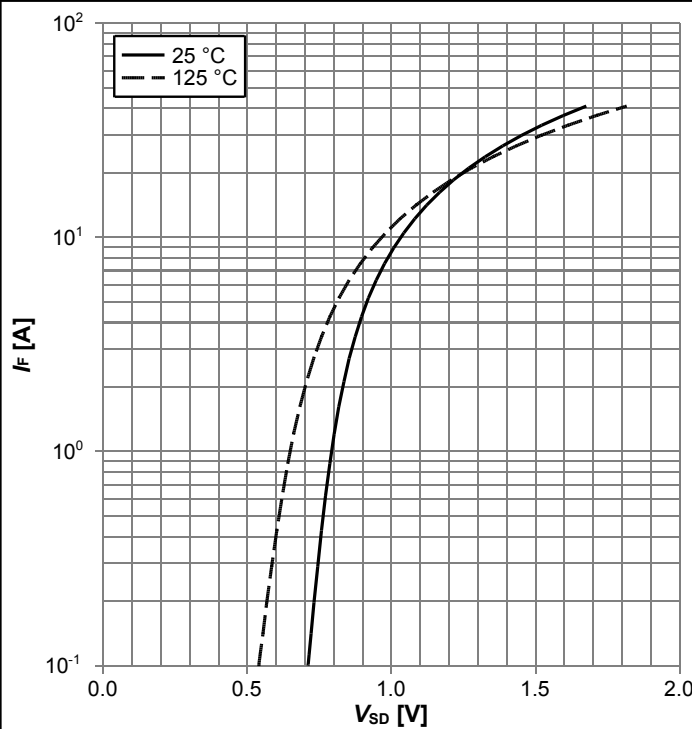
$I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge



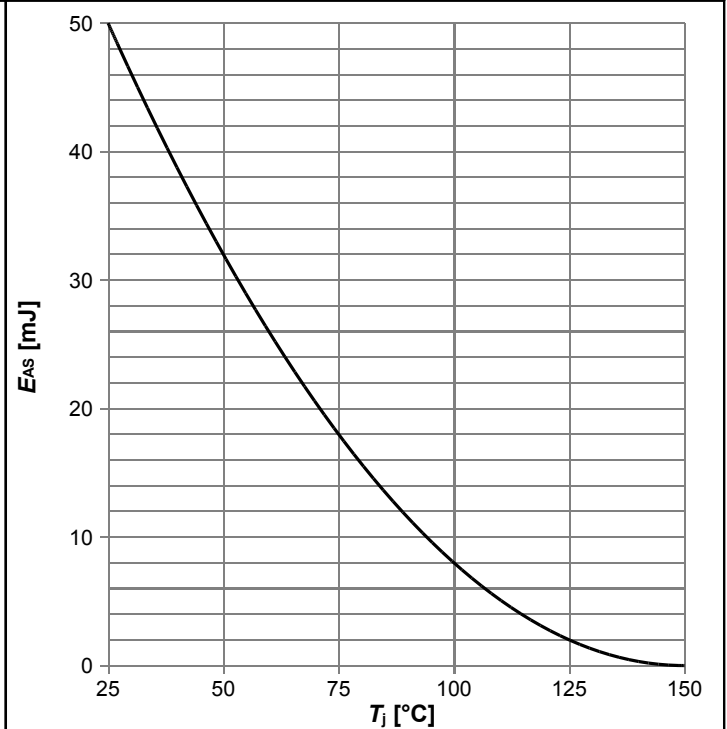
$V_{GS} = f(Q_{gate}); I_D = 2.2 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode



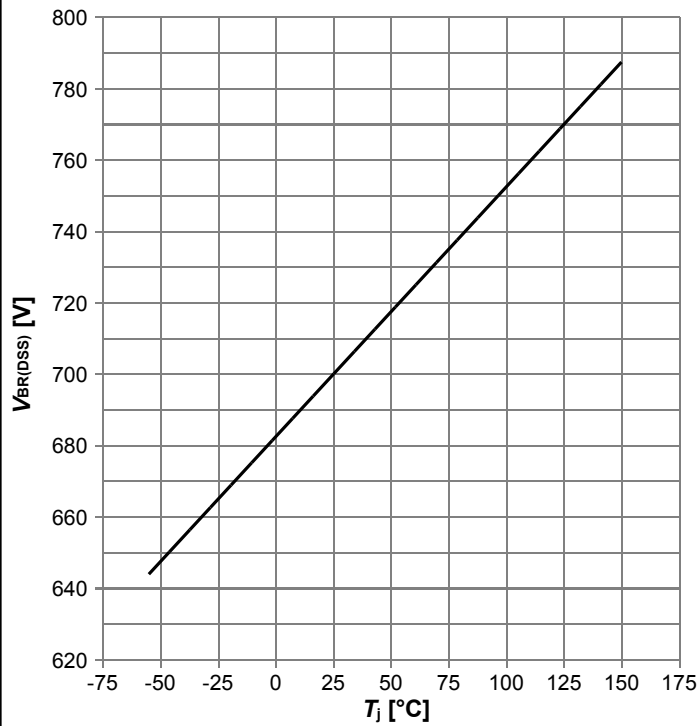
$I_F = f(V_{SD}); \text{parameter: } T_j$

Diagram 12: Avalanche energy



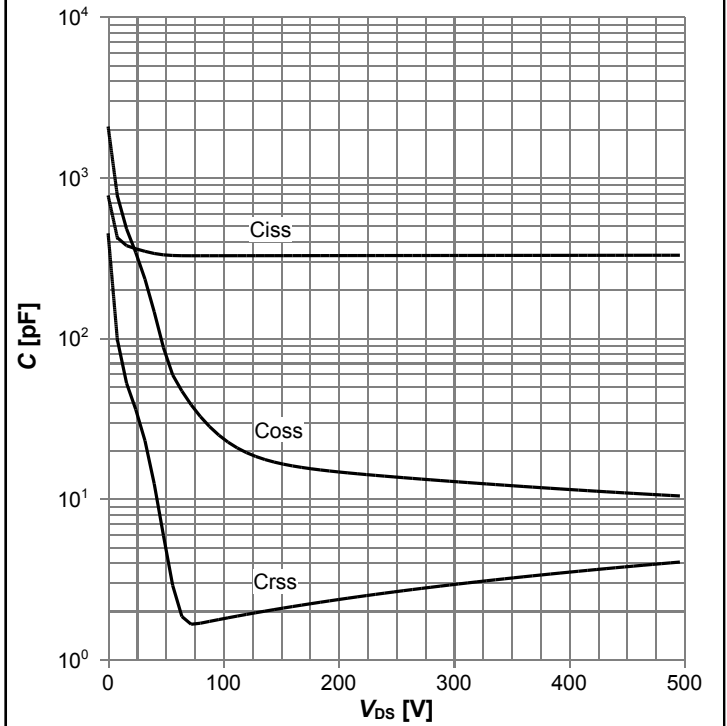
$E_{AS} = f(T_j); I_D = 1.0 \text{ A}; V_{DD} = 50 \text{ V}$

Diagram 13: Drain-source breakdown voltage



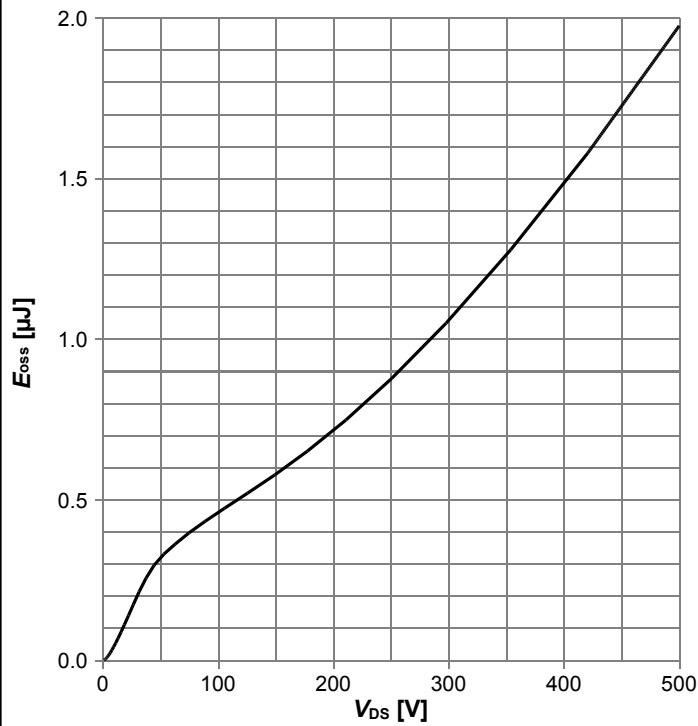
$V_{BR(DSS)}=f(T_j); I_D=1.0 \text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=1 \text{ MHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics

Test circuit for diode characteristics	Diode recovery waveform
<p>$R_{g1} = R_{g2}$</p>	<p>$t_{tr} = t_F + t_S$ $Q_{tr} = Q_F + Q_S$</p>

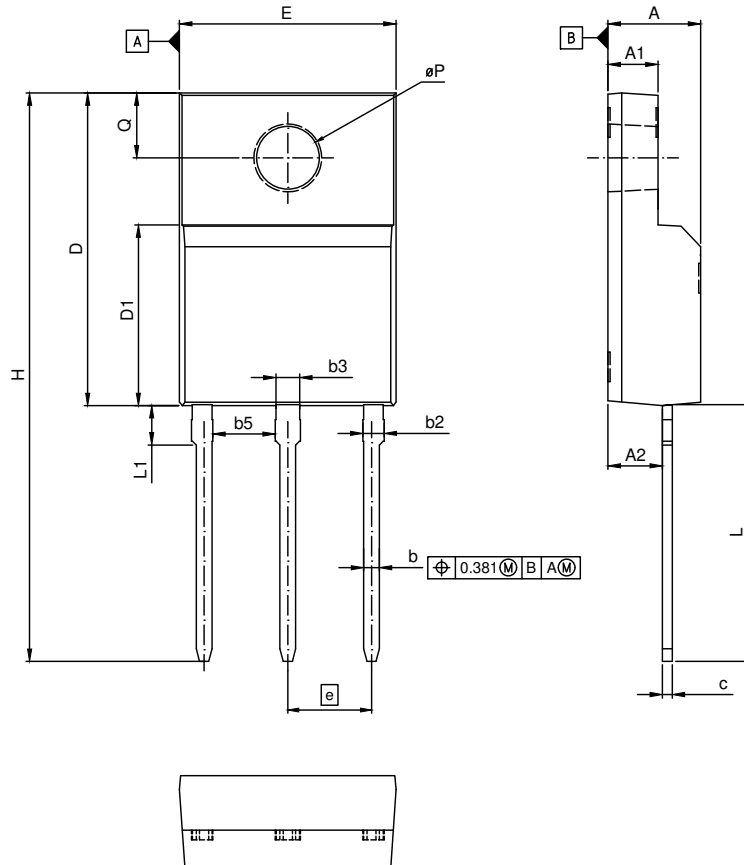
Table 9 Switching times

Switching times test circuit for inductive load	Switching times waveform

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform

6 Package Outlines



DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.50	4.90	0.177	0.193
A1	2.34	2.74	0.092	0.108
A2	2.65	2.95	0.104	0.116
b	0.75	0.90	0.030	0.035
b2	0.98	1.26	0.039	0.050
b3	1.00	1.40	0.039	0.055
b5	3.00	-	0.118	-
c	0.40	0.60	0.016	0.024
D	15.47	16.27	0.609	0.641
D1	9.17		0.361	
E	10.70	11.30	0.421	0.445
e	4.25 (BSC)		0.167 (BSC)	
N	3		3	
H	28.25	29.45	1.112	1.159
L	12.58	13.38	0.495	0.527
L1	1.70	2.30	0.067	0.091
ϕP	3.00	3.30	0.118	0.130
Q	3.10	3.50	0.122	0.138

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Figure 1 Outline PG - TO220 FullPAK WideCreepage, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- IFX CoolMOS™ CE Webpage: www.infineon.com
- IFX CoolMOS™ CE application note: www.infineon.com
- IFX CoolMOS™ CE simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

700V CoolMOS™ CE Power Transistor

IPAW70R950CE

Revision History

IPAW70R950CE

Revision: 2016-09-27, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-09-27	Release of final version

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