2A, Low Input Voltage, Ultra-Low Dropout Linear Regulator with Enable

General Description

The RT2515A is a high performance positive voltage regulator designed for use in applications requiring ultra-low input voltage and ultra-low dropout voltage at up to 2 amperes. It operates with an input voltage as low as 1.4V, with output voltage programmable as low as 0.5V. The RT2515A features ultra low dropout, ideal for applications where output voltage is very close to input voltage. Additionally, the RT2515A has an enable pin to further reduce power dissipation while shutdown. The RT2515A provides excellent regulation over variations in line, load and temperature. The RT2515A is available in the SOP-8 (Exposed Pad) package. The output voltage can be set by an external divider or fixed at 1.2V depending on how the FB pin is configured.

Ordering Information

RT2515A □□

Package Type
SP : SOP-8 (Exposed Pad-Option 2)

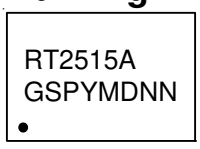
Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



RT2515AGSP : Product Number

YMDNN : Date Code

Features

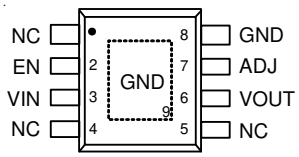
- **Input Voltage as Low as 1.4V**
- **Ultra-Low Dropout Voltage 400mV @ 2A**
- **Adjustable Output Voltage from 0.5V to 3.8V**
- **Over Current Protection**
- **Over Temperature Protection**
- **1μA Input Current in Shutdown Mode**
- **Enable Control**
- **RoHS Compliant and Halogen Free**

Applications

- Telecom/Networking Cards
- Motherboards/Peripheral Cards
- Industrial Applications
- Wireless Infrastructure
- Set Top Box
- Medical Equipment
- Notebook Computers
- Battery Powered Systems

Pin Configurations

(TOP VIEW)



SOP-8 (Exposed Pad)

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Typical Application Circuit

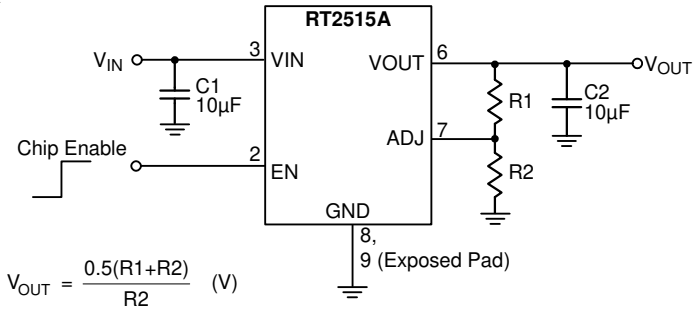


Figure 1. Adjustable Voltage Regulator

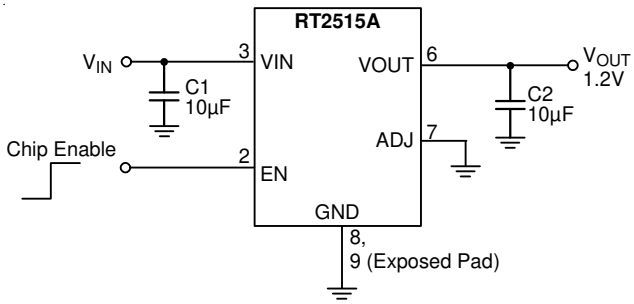
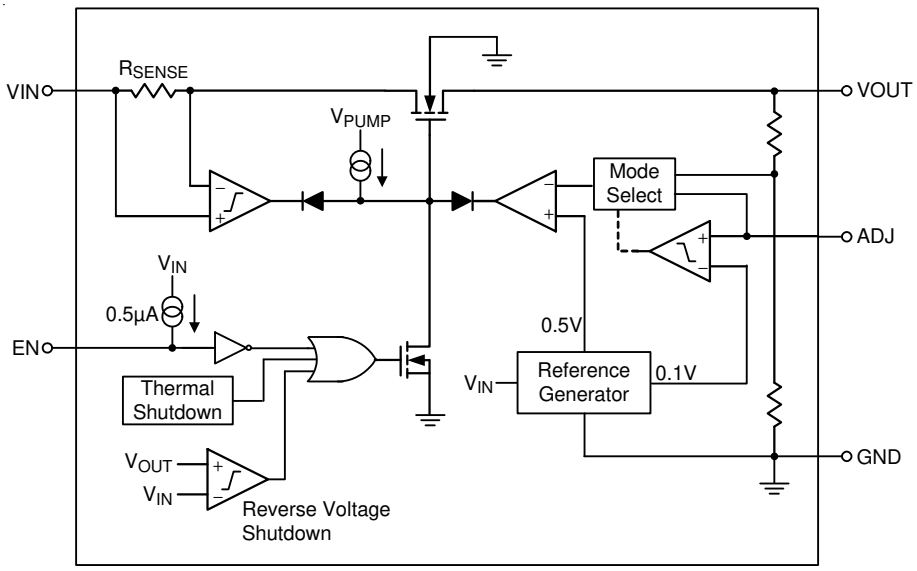


Figure 2. Fixed Voltage Regulator

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 4, 5	NC	No Internal Connection.
2	EN	Chip Enable (Active-High). Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. The device will be enabled if this pin is left open. Connect to VIN if not being used.
3	VIN	Input voltage. For regulation at full load, the input to this pin must be between (V_{OUT} + 0.5V) and 5.5V. Minimum input voltage is 1.4V. A large bulk capacitance should be placed closely to this pin to ensure that the input supply does not sag below 1.4V. Also a minimum of 10µF ceramic capacitor should be placed directly at this pin.
6	VOUT	Output Voltage. A minimum of 10µF capacitor should be placed directly at this pin.
7	ADJ	When this pin is grounded, an internal resistor divider sets the output voltage to 1.2V. If connected to the VOUT pin, the output voltage will be set at 0.5V. If external feedback resistors are used, the output voltage will be determined by the resistor ratio.
8, 9 (Exposed pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



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Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN ---------- –0.3V to 7V
- Other I/O Pin ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 (Exposed Pad) ---------- 2.04W
- Package Thermal Resistance (Note 2)
  SOP-8 (Exposed Pad), θ_{JA} ---------- 49°C/W
  SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VIN ---------- 1.4V to 6V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 1.4V to 6V, I_{OUT} = 10μA to 2A, V_{ADJ} = V_{OUT}, –40°C ≤ T_A ≤ 85°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Current	I_Q	V_{IN} = 3.3V, I_{OUT} = 0A	--	0.7	1.5	mA
Shutdown Current	I_{SHDN}	V_{IN} = 5.5V, V_{EN} = 0V	--	1.5	10	μA
Output Voltage (Fixed Output, V_{ADJ} = 0V)	V_{OUT}	V_{IN} = V_{OUT} + 0.5V, I_{OUT} = 10mA, T_A = 25°C	–2	--	2	%
		V_{IN} = 1.8V, I_{OUT} = 0.8A, T_A = 25°C				
		1.4V ≤ V_{IN} ≤ 5.5V, I_{OUT} = 10mA	–3	--	3	
Line Regulation	ΔV_{LINE}	I_{OUT} = 10mA	--	0.2	0.4	%/V
Load Regulation	ΔV_{LOAD}	I_{OUT} = 10mA to 2A	--	0.5	1.5	%
Dropout Voltage	V_{DROP}	I_{OUT} = 1A, V_{IN} ≥ 1.6V	--	120	200	mV
		I_{OUT} = 1A, 1.4V < V_{IN} < 1.6V	--	--	400	
		I_{OUT} = 1.5A, V_{IN} ≥ 1.6V	--	180	300	
		I_{OUT} = 1.5A, 1.4V < V_{IN} < 1.6V	--	--	500	
		I_{OUT} = 2A, V_{IN} ≥ 1.6V	--	240	400	
		I_{OUT} = 2A, 1.4V < V_{IN} < 1.6V	--	--	600	
Current Limit	I_{LIM}	V_{IN} = 3.3V	2.3	3	4.4	A

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Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Feedback							
ADJ Reference Voltage		V_{ADJ}	V_{IN} = 3.3V, V_{ADJ} = V_{OUT}, I_{OUT} = 10mA, T_A = 25°C	0.495	--	0.505	V
			V_{IN} = 3.3V, V_{ADJ} = V_{OUT}, I_{OUT} = 10mA	0.49	--	0.51	
ADJ Pin Current		I_{ADJ}	V_{ADJ} = 0.5V	--	20	200	nA
ADJ Pin Threshold		V_{TH_ADJ}	V_{IN} = 3.3V	0.05	0.1	0.15	V
Enable							
EN Pin Current		I_{EN}	V_{EN} = 0V, V_{IN} = 5.5V	--	1	10	μA
EN Threshold Voltage	Logic-High	V_{IH}	V_{IN} = 3.3V	1.6	--	--	V
	Logic-Low	V_{IL}	V_{IN} = 3.3V	--	--	0.4	
Over Temperature Protection							
OTP Trip Level				--	160	--	°C
Hysteresis				--	30	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

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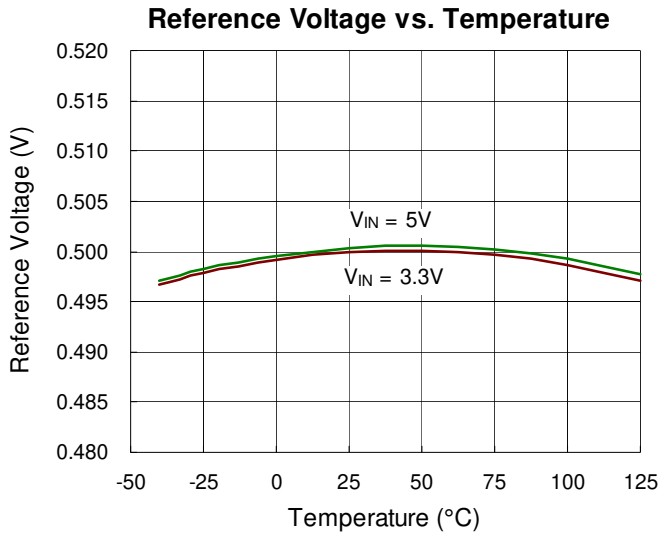
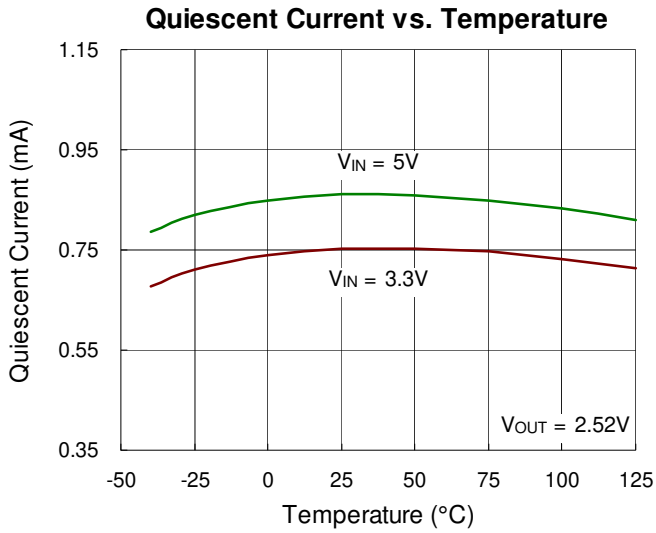
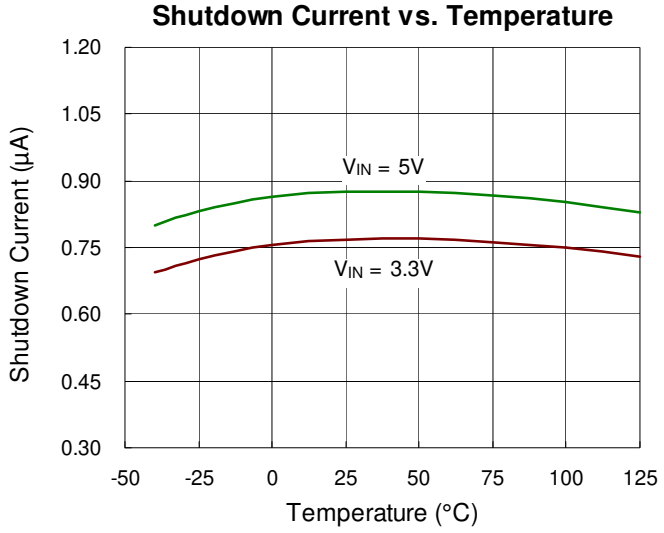
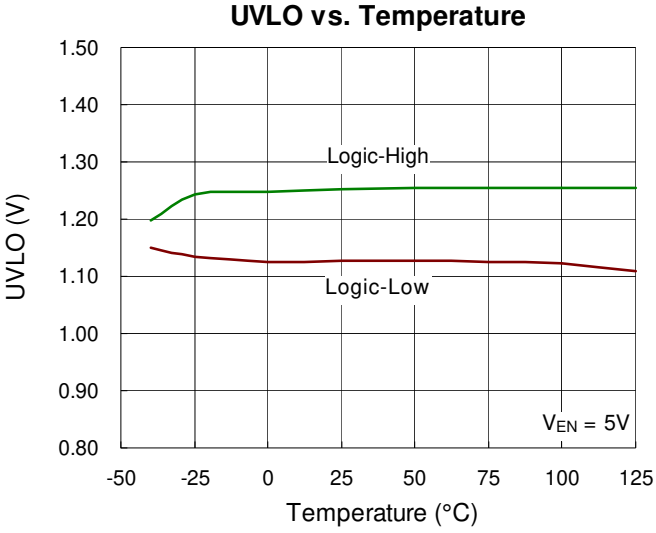
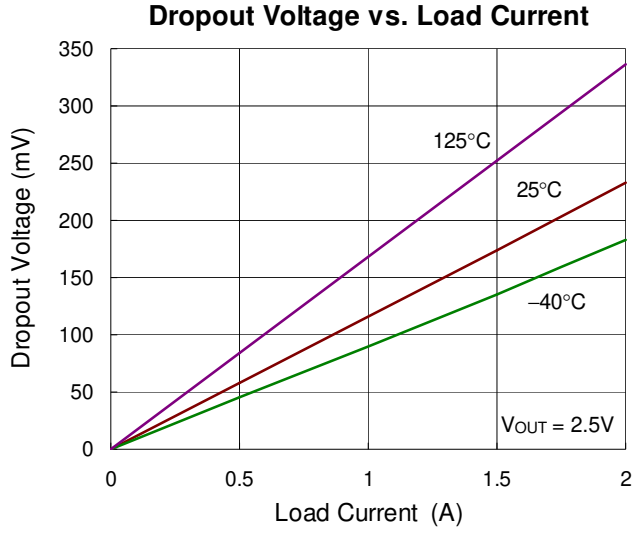
Typical Operating Characteristics

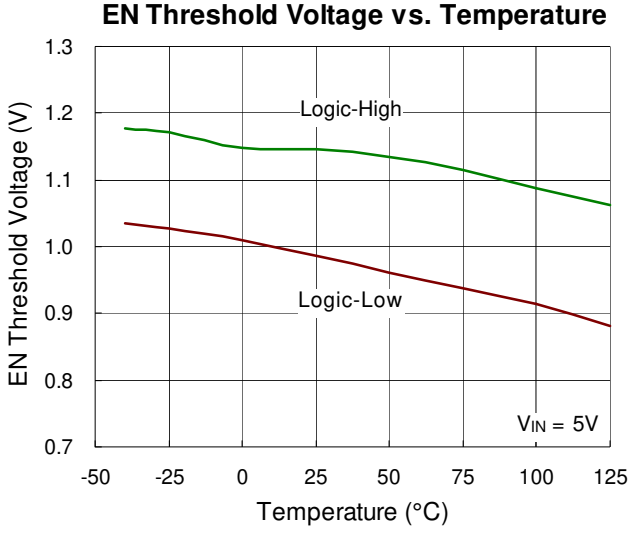












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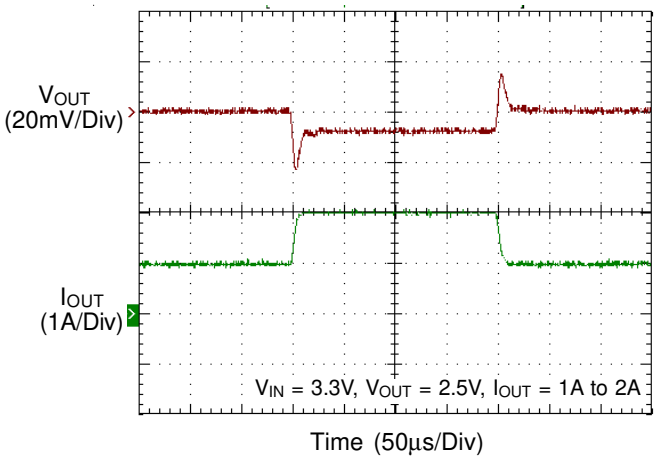
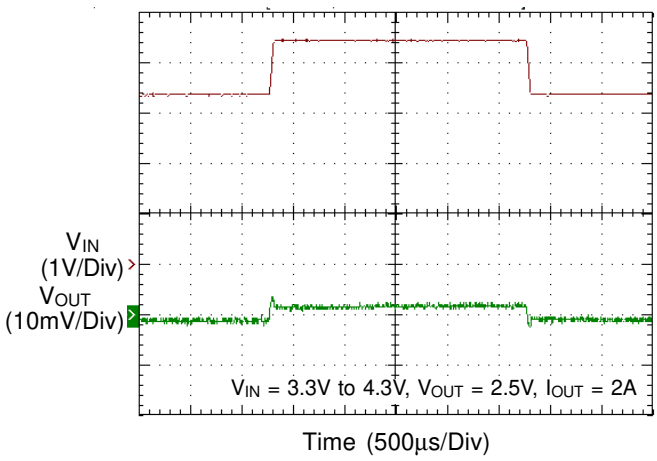
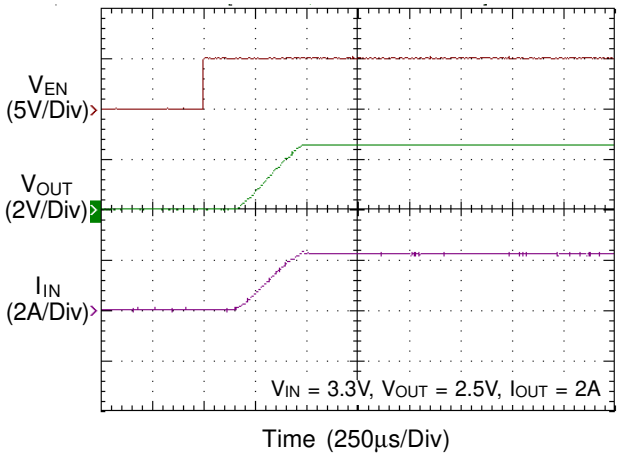
Load Transient Response



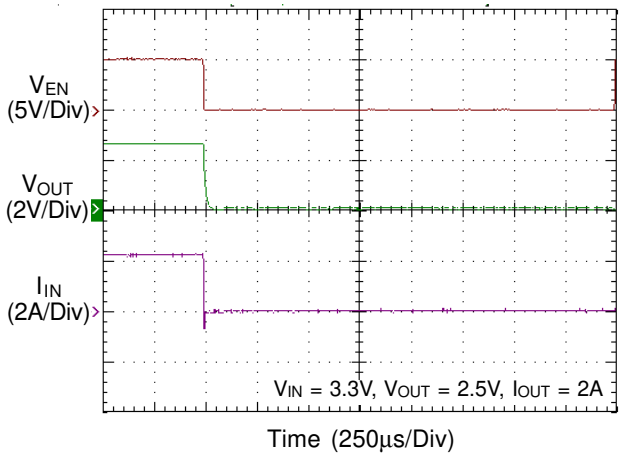
Line Transient Response



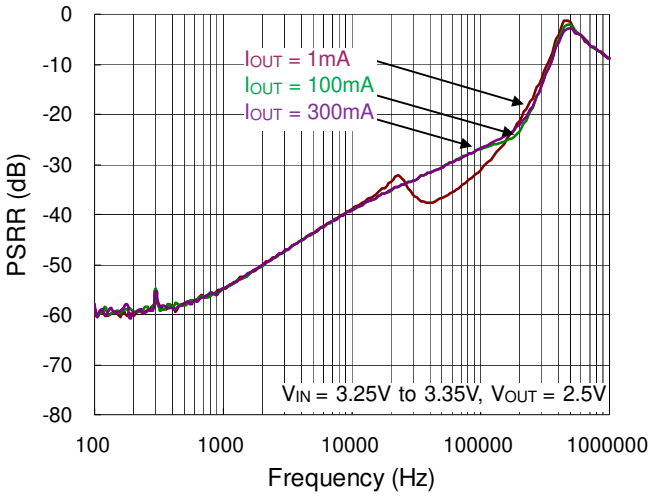
Power On from EN



Power Off from EN



PSRR



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Application Information

The RT2515A is a low voltage, low dropout linear regulator with an external bias supply input capable of supporting an input voltage range from 1.4V to 6V with a fixed output voltage from 1V to 2V in 0.1V increments.

Output Voltage Setting

The RT2515A output voltage is adjustable from 1.4V to 6V via the external resistive voltage divider. The voltage divider resistors can have values of up to 800kΩ because of the very high impedance and low bias current of the sense comparator. The output voltage is set according to the following equation :

$$V_{OUT} = V_{ADJ} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{ADJ} is the reference voltage with a typical value of 0.5V.

Chip Enable Operation

The RT2515A goes into sleep mode when the EN pin is in a logic low condition. In this condition, the pass transistor, error amplifier, and band gap are all turned off, reducing the supply current to only 10μA (max.). The EN pin can be directly tied to VIN to keep the part on.

Current Limit

The RT2515A contains an independent current limit circuitry, which monitors and controls the pass transistor's gate voltage, limiting the output current to 3A (typ.).

C_{IN} and C_{OUT} Selection

Like any low dropout regulator, the external capacitors of the RT2515A must be carefully selected for regulator stability and performance. Using a capacitor of at least 10μF is suitable. The input capacitor must be located at a distance of not more than 0.5 inch from the input pin of the IC. Any good quality ceramic capacitor can be used. However, a capacitor with larger value and lower ESR (Equivalent Series Resistance) is recommended since it will provide better PSRR and line transient response.

The RT2515A is designed specifically to work with low ESR ceramic output capacitor for space saving and performance consideration. Using a ceramic capacitor with capacitance of at least 10μF and ESR larger than 1mΩ on the RT2515A output ensures stability. Nevertheless, the RT2515A can still work well with other types of output capacitors due to its wide range of stable ESR. Figure 3 shows the allowable ESR range as a function of load current for various output capacitance. Output capacitors with larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located at a distance of not more than 0.5 inch from the output pin of the RT2515A.

Region of Stable C_{OUT} ESR vs. Load Current

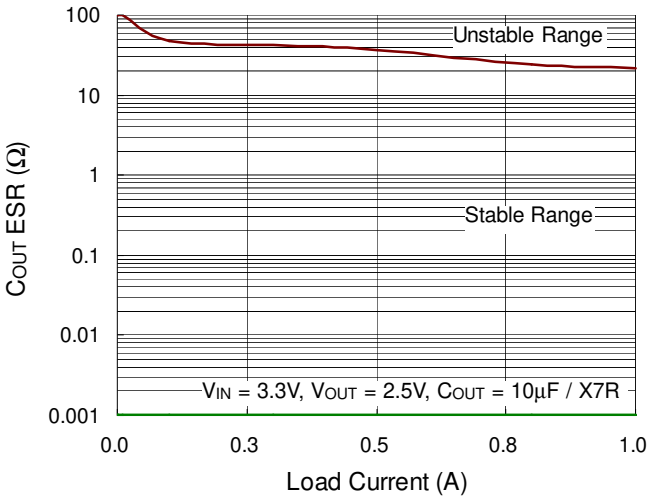

Figure 3

Thermal Considerations

Thermal protection limits power dissipation in RT2515A. When the operation junction temperature exceeds 160°C, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turns on again after the junction temperature cools by 30°C.

RT2515A output voltage will be closed to zero when output short circuit occurs as shown in Figure 4. It can reduce the IC temperature and provides maximum safety to end users when output short circuit occurs.

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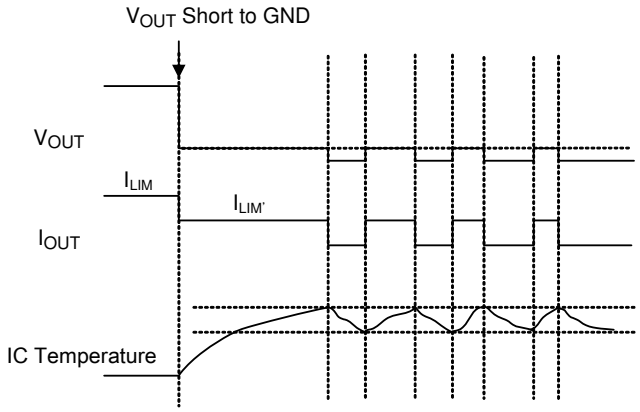

Figure 4. Short Circuit Protection when Output Short Circuit Occurs

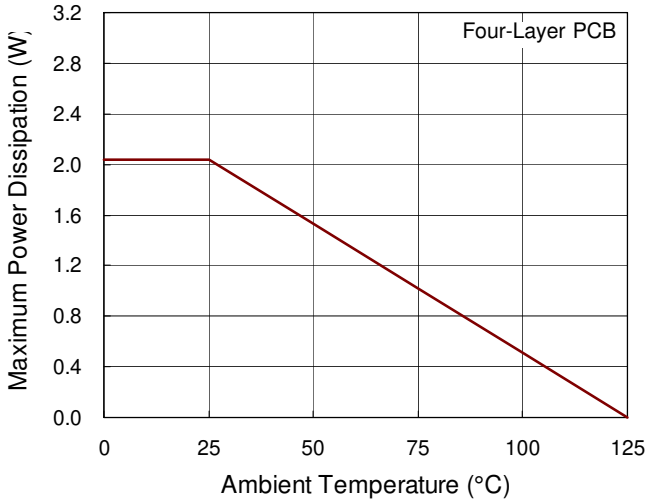

Figure 5. Derating Curve of Maximum Power Dissipation

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 (Exposed Pad) package, the thermal resistance, θ_{JA}, is 49°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)} = (125°C - 25°C) / (49°C/W) = 2.04W$ for

SOP-8 (Exposed Pad) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

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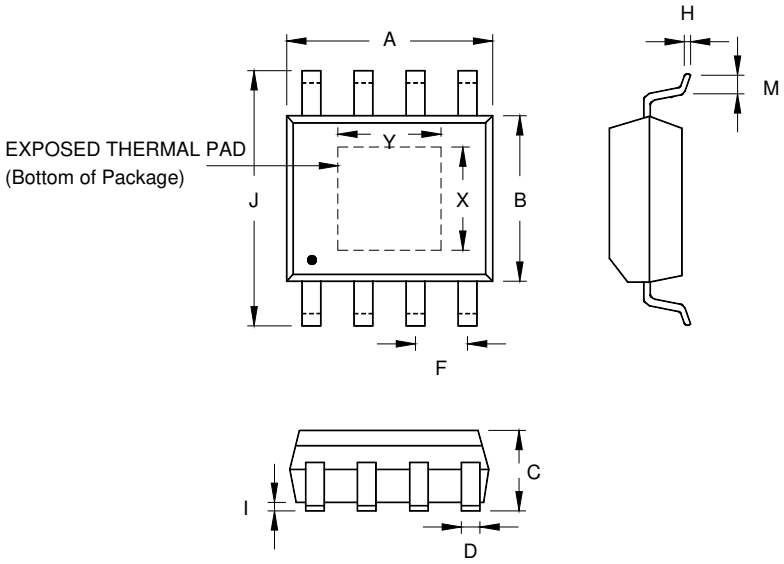
Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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