



# FDMA8884

## Single N-Channel Power Trench<sup>®</sup> MOSFET

30 V, 6.5 A, 23 mΩ



### Features

- Max  $r_{DS(on)}$  = 23 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 6.5\text{ A}$
- Max  $r_{DS(on)}$  = 30 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 6.0\text{ A}$
- High performance trench technology for extremely low  $r_{DS(on)}$
- Fast switching speed
- RoHS Compliant

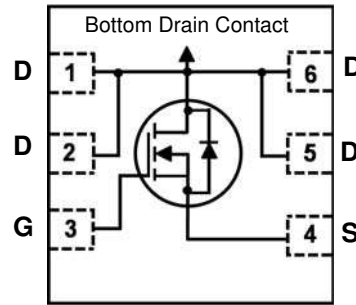
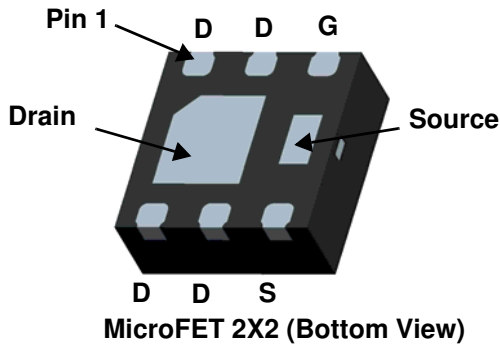


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench<sup>®</sup> process that has been optimized for  $r_{DS(on)}$  switching performance.

### Application

- Primary Switch



### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

| Symbol         | Parameter  | Rated       | Units |
|----------------|--|-------------|-------|
| $V_{DS}$       | Drain to Source Voltage  | 30          | V     |
| $V_{GS}$       | Gate to Source Voltage (Note 3)                                  | ±20         | V     |
| $I_D$          | Drain Current -Continuous (Package limited) $T_C = 25\text{ °C}$ | 8.0         | A     |
|                | -Continuous $T_A = 25\text{ °C}$ (Note 1a)                       | 6.5         |       |
|                | -Pulsed  | 25          |       |
| $P_D$          | Power Dissipation (Note 1a)                                      | 1.9         | W     |
|                | Power Dissipation (Note 1b)                                      | 0.7         |       |
| $T_J, T_{STG}$ | Operating and Storage Junction Temperature Range                 | -55 to +150 | °C    |

### Thermal Characteristics

|                 |   |     |      |
|-----------------|---|-----|------|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 65  | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1b) | 180 |      |

### Package Marking and Ordering Information

| Device Marking | Device   | Package      | Reel Size | Tape Width | Quantity   |
|----------------|----------|--------------|-----------|------------|------------|
| 884            | FDMA8884 | MicroFET 2x2 | 7"        | 8 mm       | 3000 units |

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
|--------|-----------|-----------------|-----|-----|-----|-------|

### Off Characteristics

|                                      |   |   |    |    |     |                      |
|--------------------------------------|---|---|----|----|-----|----------------------|
| $BV_{DSS}$                           | Drain to Source Breakdown Voltage         | $I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$                       | 30 |    |     | V                    |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$ |    | 15 |     | mV/ $^\circ\text{C}$ |
| $I_{DSS}$                            | Zero Gate Voltage Drain Current           | $V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$                               |    |    | 1   | $\mu\text{A}$        |
| $I_{GSS}$                            | Gate to Source Leakage Current, Forward   | $V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$                               |    |    | 100 | nA                   |

### On Characteristics

|  |  |   |     |     |     |                      |
|--|--|---|-----|-----|-----|----------------------|
| $V_{GS(th)}$                           | Gate to Source Threshold Voltage                         | $V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$                             | 1.2 | 1.8 | 3.0 | V                    |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$   |     | -5  |     | mV/ $^\circ\text{C}$ |
| $r_{DS(on)}$                           | Static Drain to Source On Resistance                     | $V_{GS} = 10\text{ V}, I_D = 6.5\text{ A}$                                  |     | 19  | 23  | m $\Omega$           |
|  |  | $V_{GS} = 4.5\text{ V}, I_D = 6.0\text{ A}$                                 |     | 25  | 30  |                      |
|  |  | $V_{GS} = 10\text{ V}, I_D = 6.5\text{ A}, T_J = 125\text{ }^\circ\text{C}$ |     | 25  | 30  |                      |
| $g_{FS}$                               | Forward Transconductance                                 | $V_{DD} = 5\text{ V}, I_D = 6.5\text{ A}$                                   |     | 26  |     | S                    |

### Dynamic Characteristics

|           |                              |   |  |     |     |          |
|-----------|------------------------------|---|--|-----|-----|----------|
| $C_{iss}$ | Input Capacitance            | $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ |  | 339 | 450 | pF       |
| $C_{oss}$ | Output Capacitance           |   |  | 132 | 175 | pF       |
| $C_{rss}$ | Reverse Transfer Capacitance |   |  | 18  | 28  | pF       |
| $R_g$     | Gate Resistance              |   |  | 1.1 |     | $\Omega$ |

### Switching Characteristics

|              |                               |   |                                      |  |     |     |
|--------------|-------------------------------|---|--------------------------------------|--|-----|-----|
| $t_{d(on)}$  | Turn-On Delay Time            | $V_{DD} = 15\text{ V}, I_D = 6.5\text{ A}, V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$ |                                      | 5  | 10  | ns  |
| $t_r$        | Rise Time                     |   |                                      | 1  | 10  | ns  |
| $t_{d(off)}$ | Turn-Off Delay Time           |   |                                      | 11   | 20  | ns  |
| $t_f$        | Fall Time                     |   |                                      | 1  | 10  | ns  |
| $Q_{g(TOT)}$ | Total Gate Charge             |   | $V_{GS} = 0\text{ V to }10\text{ V}$ | $V_{DD} = 15\text{ V}, I_D = 6.5\text{ A}$ | 5.4 | 7.5 |
|              | Total Gate Charge             | $V_{GS} = 0\text{ V to }4.5\text{ V}$   | 2.7                                  |  | 3.7 | nC  |
| $Q_{gs}$     | Total Gate Charge             |   | 1.0                                  |  |     | nC  |
| $Q_{gd}$     | Gate to Drain "Miller" Charge |   | 0.9                                  |  |     | nC  |

### Drain-Source Diode Characteristics

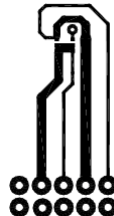
|          |                                       |  |  |      |     |    |
|----------|---------------------------------------|--|--|------|-----|----|
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS} = 0\text{ V}, I_S = 6.5\text{ A}$ (Note 2)     |  | 0.86 | 1.2 | V  |
| $t_{rr}$ | Reverse Recovery Time                 | $I_F = 6.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ |  | 16   | 28  | ns |
| $Q_{rr}$ | Reverse Recovery Charge               |  |  | 4    | 10  | nC |

#### NOTES:

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $65\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper.

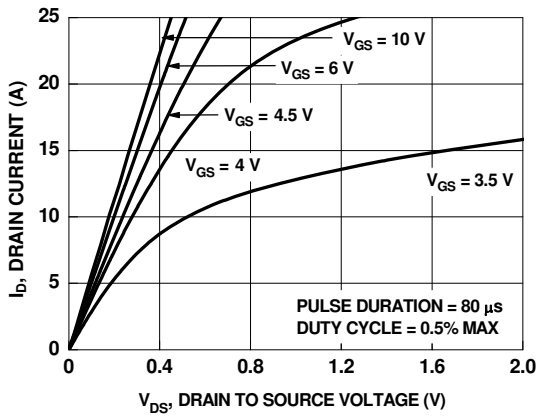


b.  $180\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

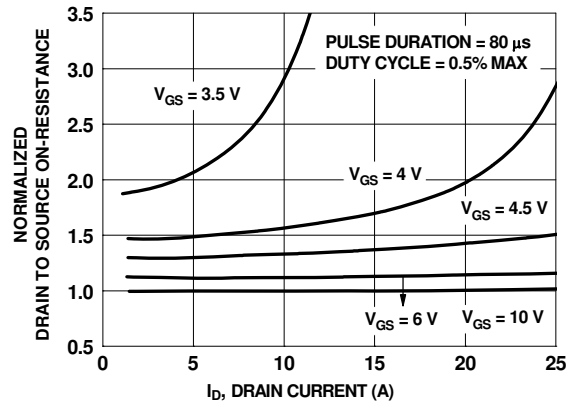
2. Pulse Test: Pulse Width <  $300\text{ }\mu\text{s}$ , Duty cycle < 2.0 %.

3. As an N-ch device, the negative  $V_{GS}$  rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

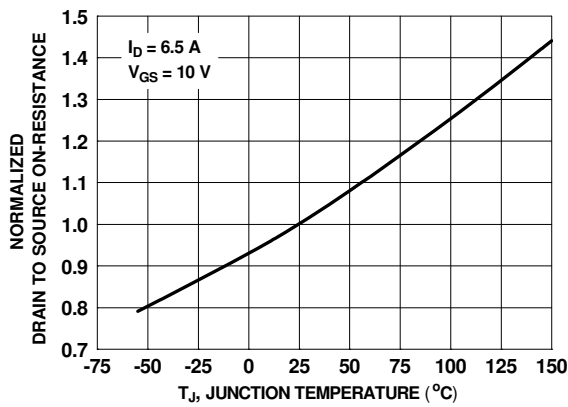
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



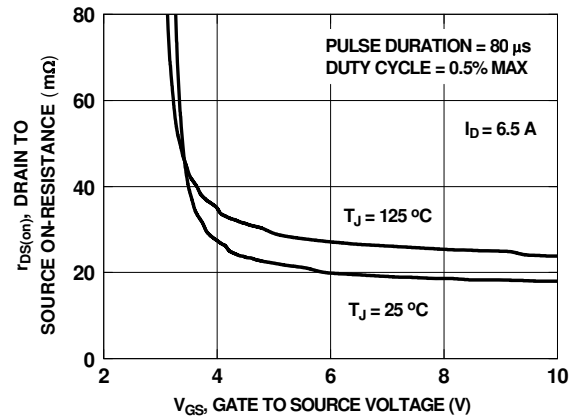
**Figure 1. On Region Characteristics**



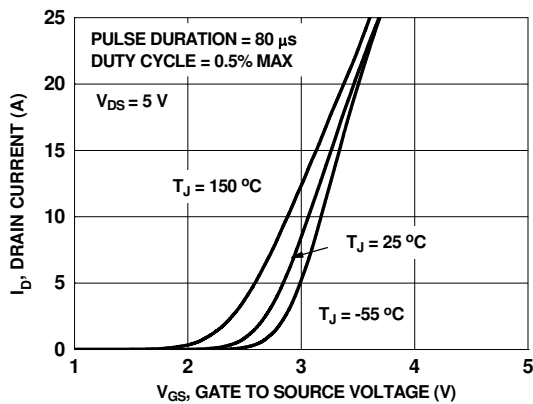
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



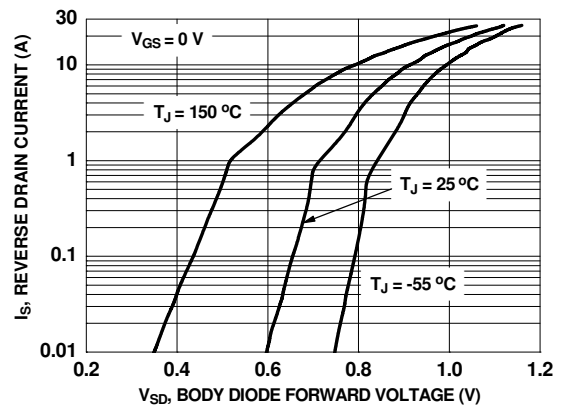
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

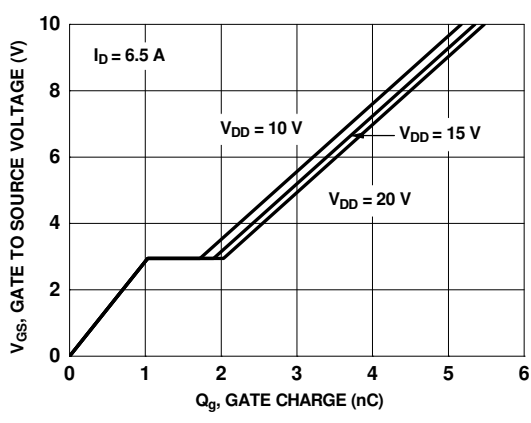


**Figure 5. Transfer Characteristics**

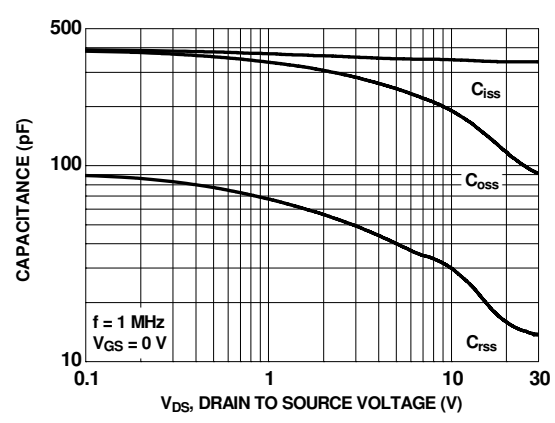


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

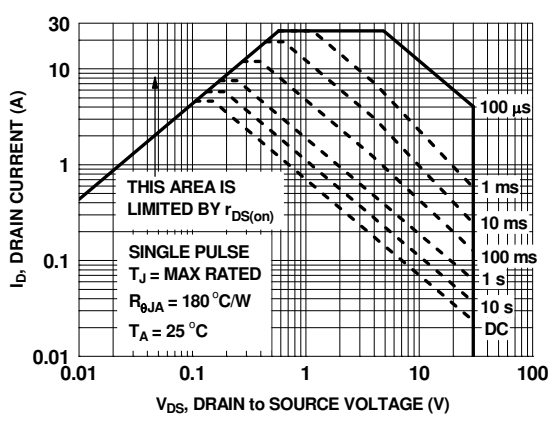
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



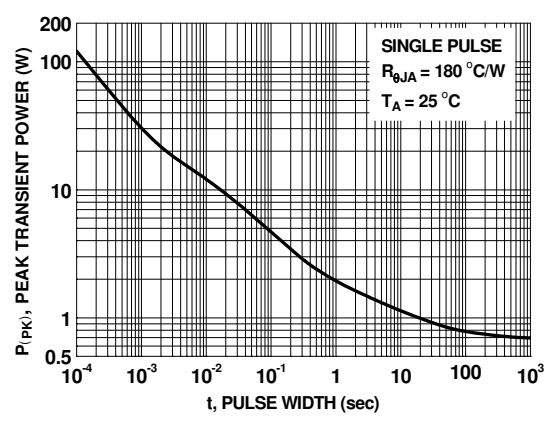
**Figure 7. Gate Charge Characteristics**



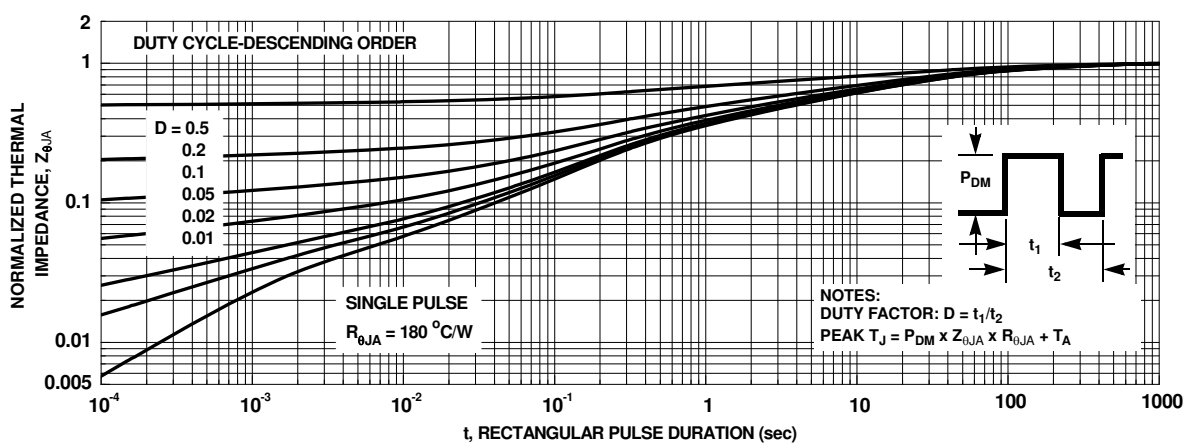
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Forward Bias Safe Operating Area**



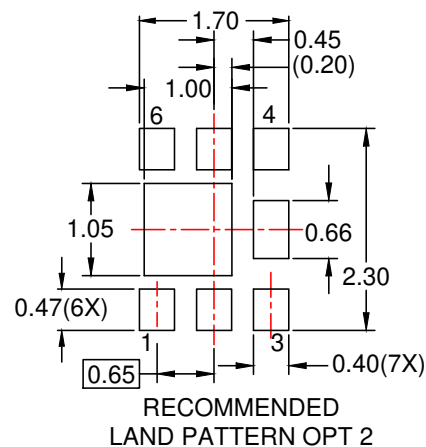
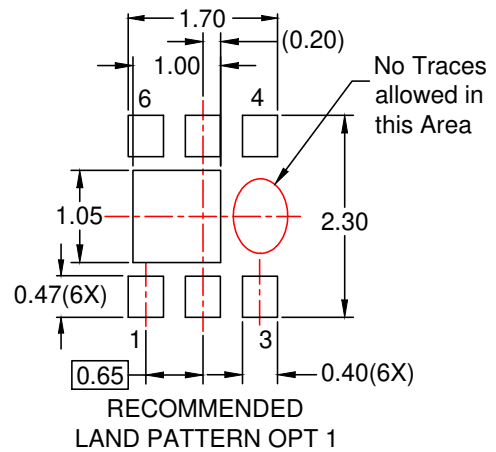
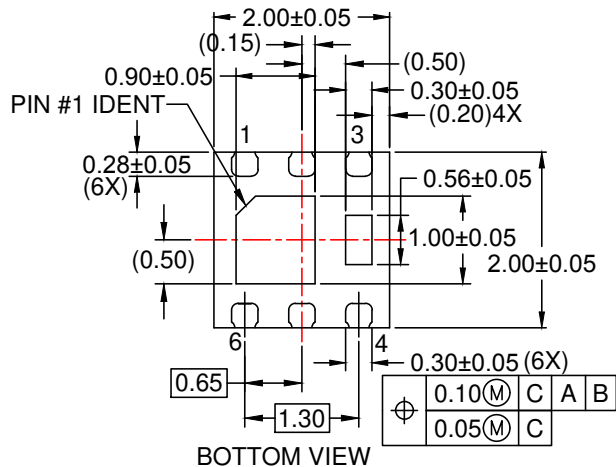
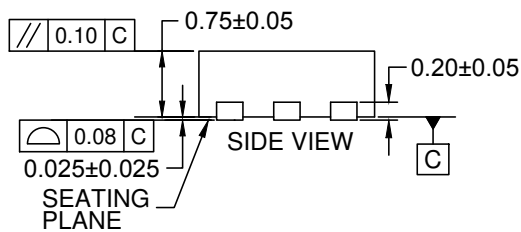
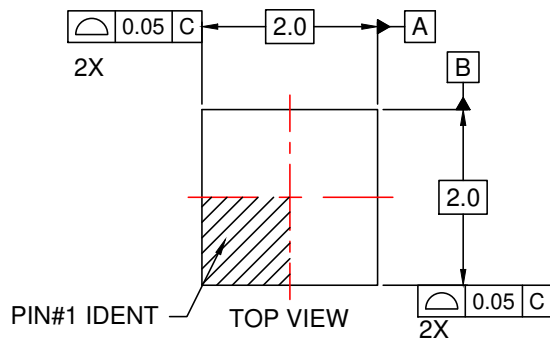
**Figure 10. Single Pulse Maximum Power Dissipation**



**Figure 11. Junction-to-Ambient Transient Thermal Response Curve**

**Figure 12.**

## Dimensional Outline and Pad Layout



### NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP06Lrev4.








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| BitSiC™  | Global Power Resource <sup>SM</sup>             | Programmable Active Droop™  | TinyBuck®  |
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