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Designing with QorIQ P1020, P1021 and P1022 Processors

FTF-NET-F0430

Zhongcai Zhou
Applications Engineer

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Session Objectives

- This session will :
  - Provide overview and highlight the new features introduced with the QorIQ P1020,P1021 and P1022 processor family.
  - Help you to choose the correct processor for your next application

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Agenda

- Introduction
- QorIQ P1020/21/22 processor overview
- Markets and applications
- QorIQ P1020/21/22 common subsystem
- QorIQ P1021 only subsystem
- QorIQ P1022 only subsystem
- QorIQ development boards
- Summary

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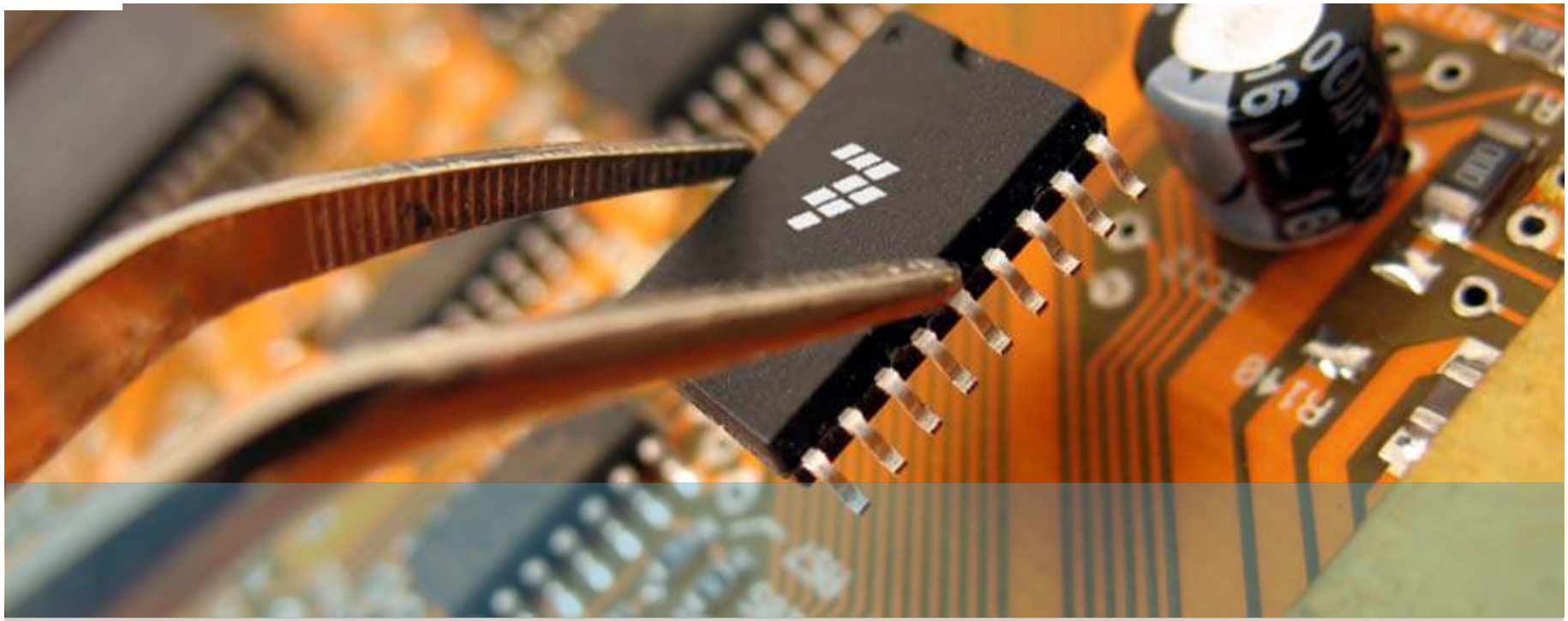

QorIQ P1020/21/22 Processors Overview

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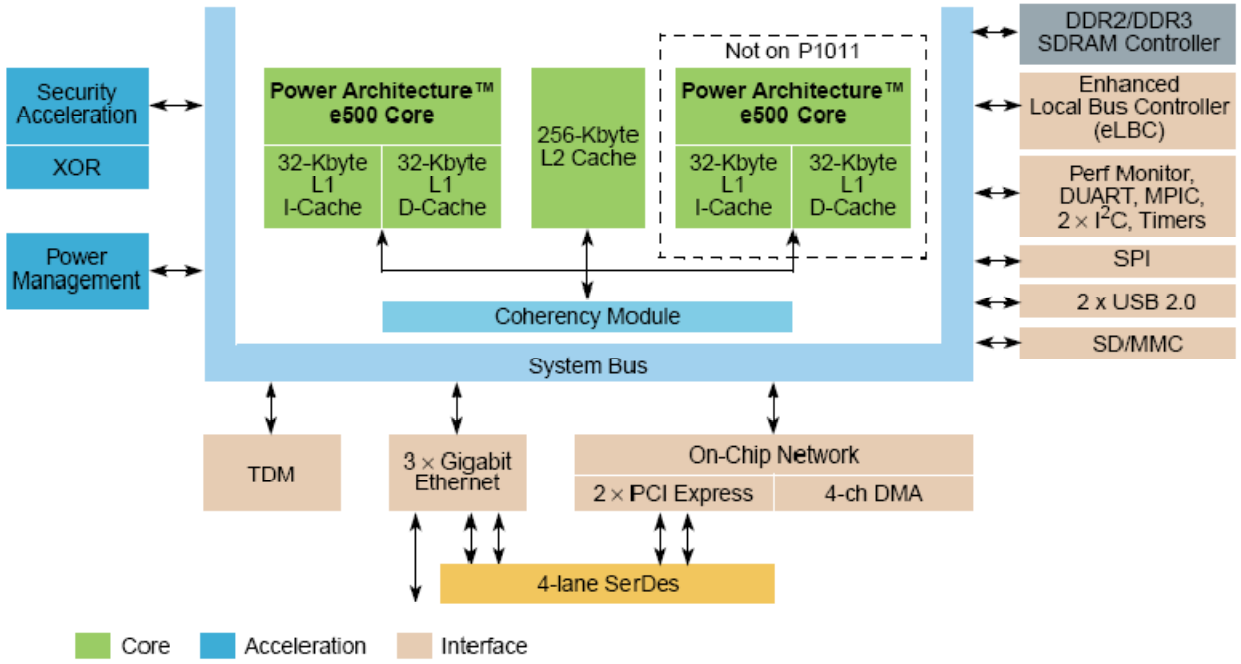
QorIQ P1020 Processor Overview

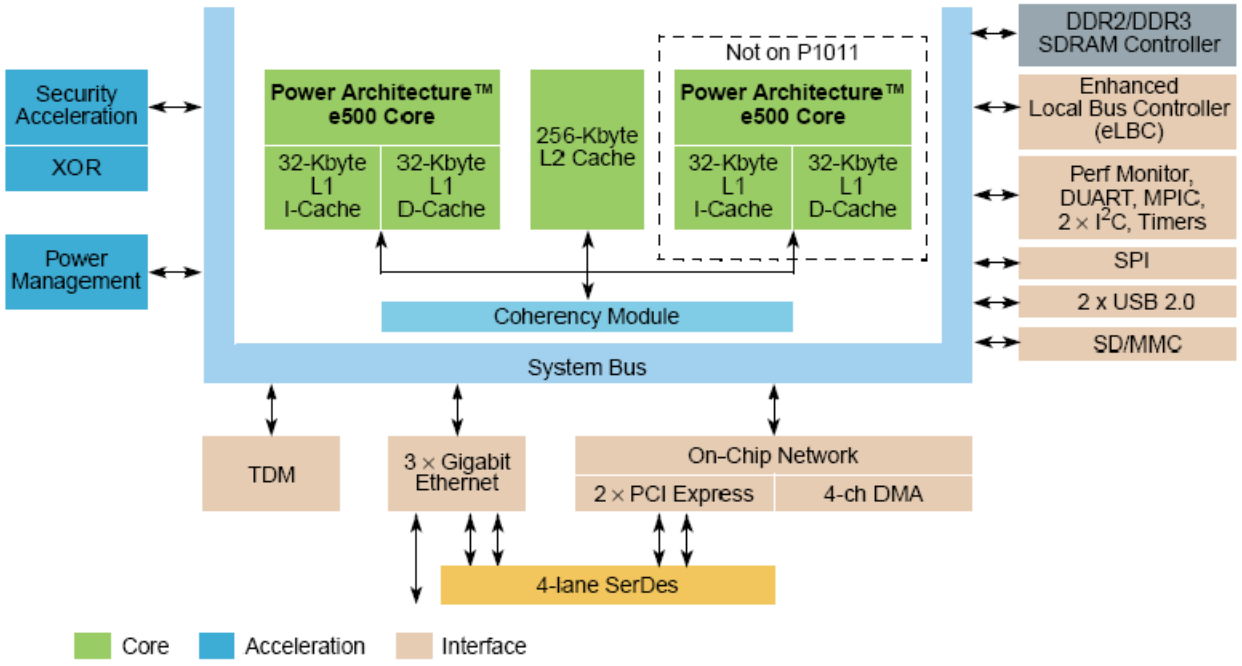
- Dual e500 cores, built on Power Architecture® technology
  - 533 – 800 MHz
  - 256KB Frontside L2 cache w/ECC, HW cache coherent
  - 36-bit physical addressing, DP-FPU



QorIQ P1020 Processor Overview (cont.)

System Unit

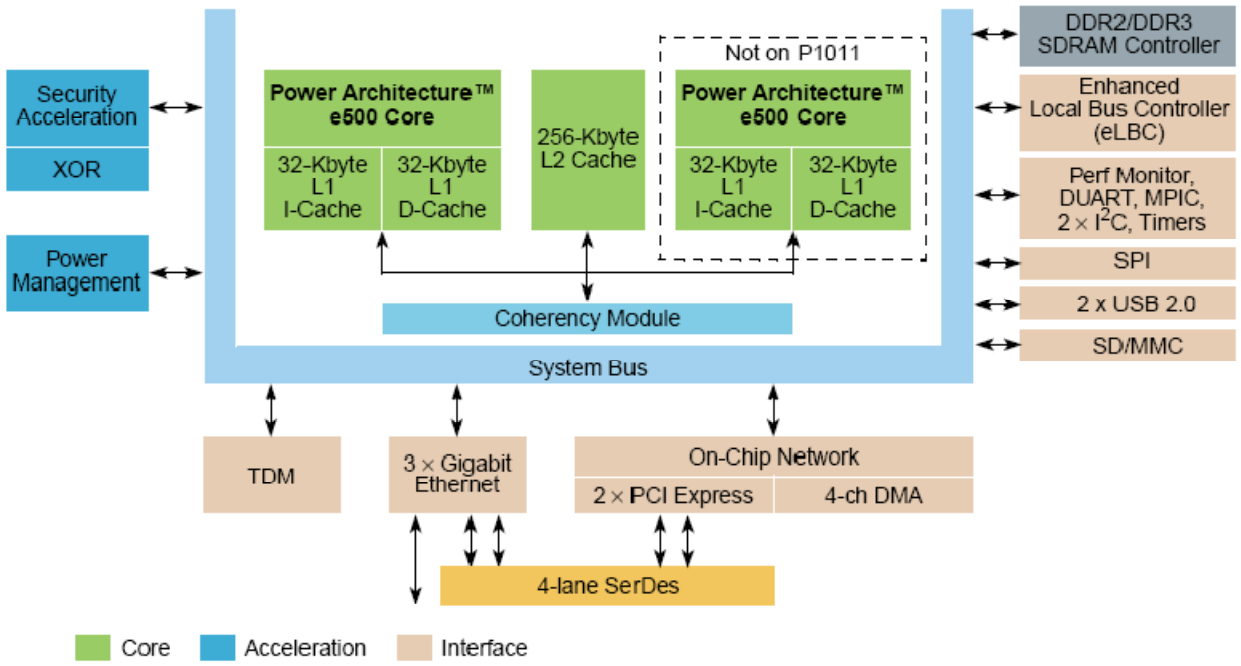
- 32-bit DDR2/DDR3 with ECC
- Integrated SEC 3.3.2 Security Engine
- Open-PIC Interrupt Controller, Perf Mon, 2x I²C, Timers, 16 GPIO's, DUART
- 16-bit Enhanced Local Bus supports booting from NAND Flash
- Two USB 2.0 controllers Host/Device support
- SPI controller supporting booting from SPI serial flash memory
- SD/MMC card controller supporting booting from flash memory cards
- TDM interface



- Three 10/100/1000 Ethernet Controllers (eTSEC) w/ Jumbo Frame support, SGMII interface
- Two PCI Express® 1.0a controllers operating at 2.5 GHz
- Power Management

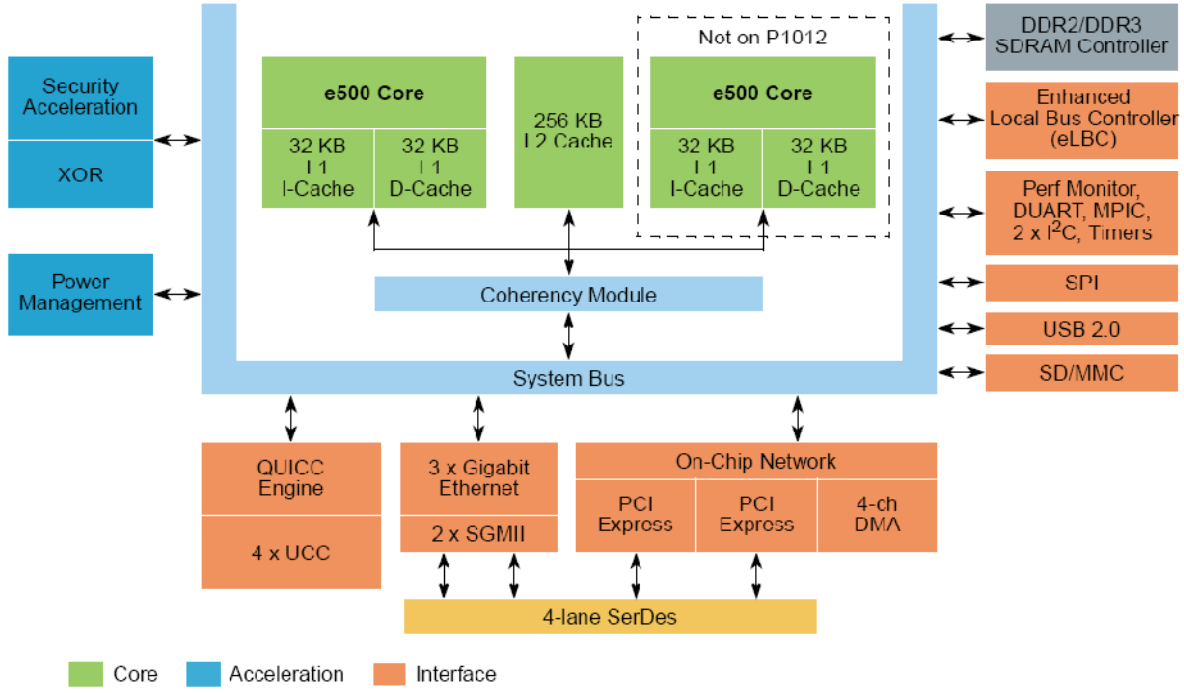
QorIQ P1020 Processor Overview (cont.)

- Process & Package
  - 45nm SOI, 0C to 125C Tj with -40C to 125C Tj option
  - 689-pin TePBGAII



QorIQ P1021 Processor Overview

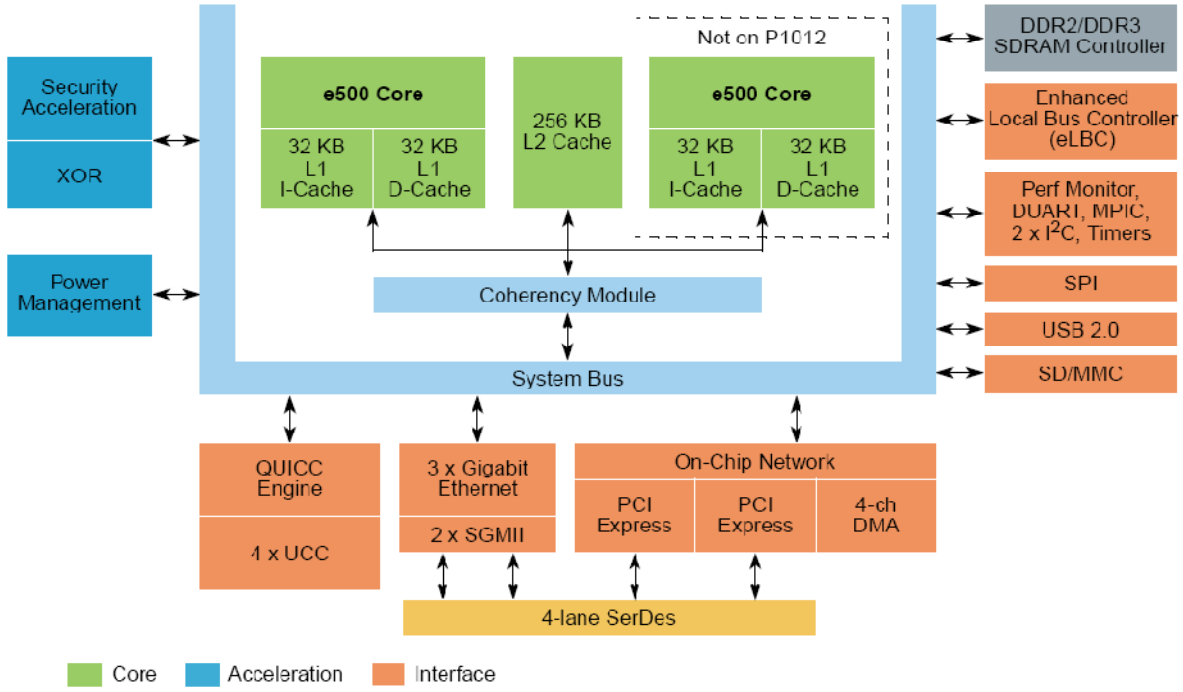
- Dual e500 cores, built on Power Architecture® technology
  - 533 – 800 MHz
  - 256KB Frontside L2 cache w/ECC, HW cache coherent



QorIQ P1021 Processor Overview (cont.)

System Unit

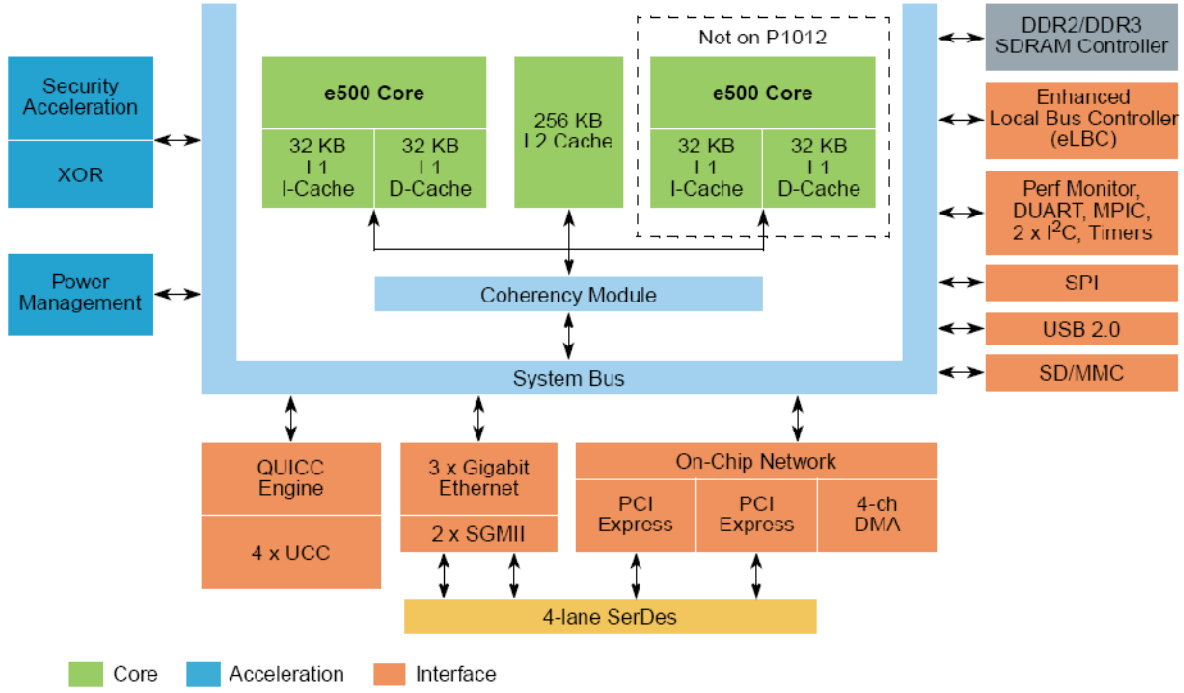
- 32-bit DDR2/DDR3 SDRAM memory controller with ECC support
- Three 10/100/1000 Mbps enhanced three-speed Ethernet controllers
- QUICC Engine block
  - 32-bit RISC controller for flexible support of the communications peripherals
- High-speed interfaces
  - Four SerDes lanes running at 2.5 GHz (multiplexed across controllers)
  - Up to two PCI Express® interfaces (two x1 or one x1/x2/x4)
- High-speed USB controller (USB 2.0)
- Enhanced secure digital host controller (SD/MMC)



- Integrated security engine (SEC3.3.2)
  - Crypto algorithm support includes 3DES, AES, MD5/SHA, RSA/ECC, and FIPS deterministic RNG
- Programmable interrupt controller (PIC) compliant with Open-PIC standard
- Four-channel DMA controller

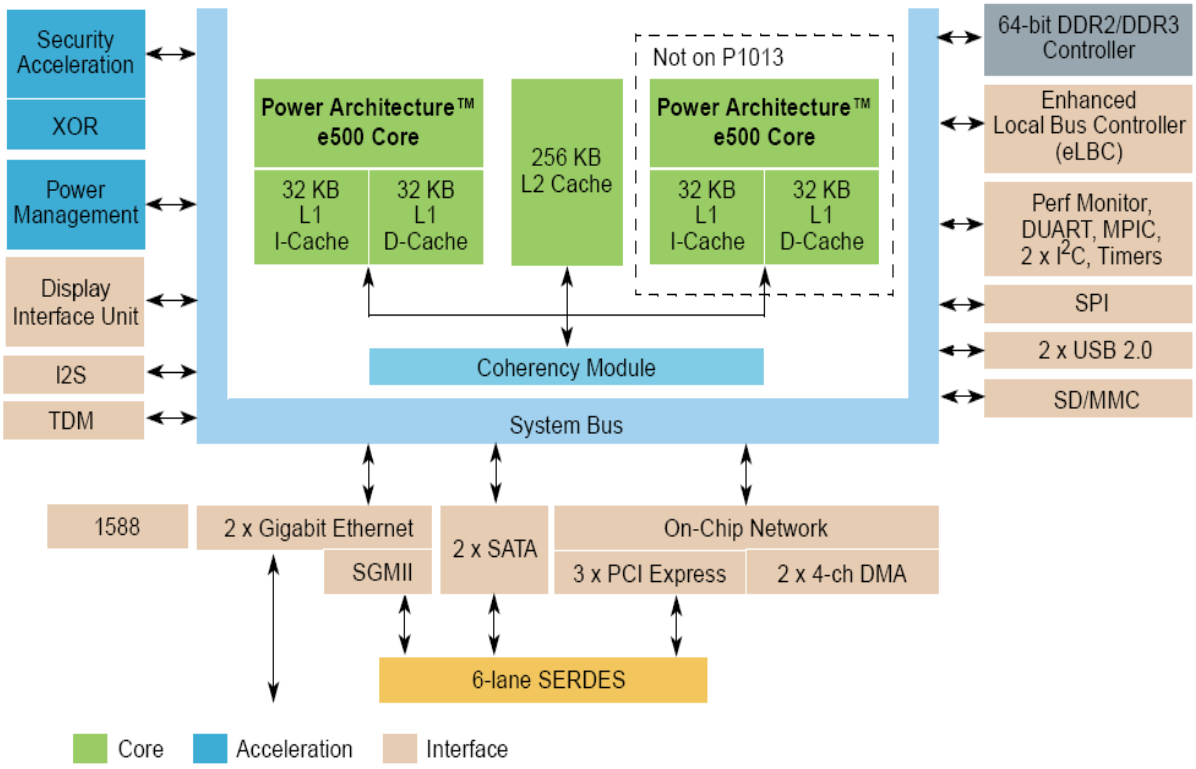
QorIQ P1021 Processor Overview (cont.)

- Process & Package
  - 45nm SOI, 0C to 125C Tj with -40C to 125C Tj option
  - 689-pin TePBGAII



QorIQ P1022 Processor Overview

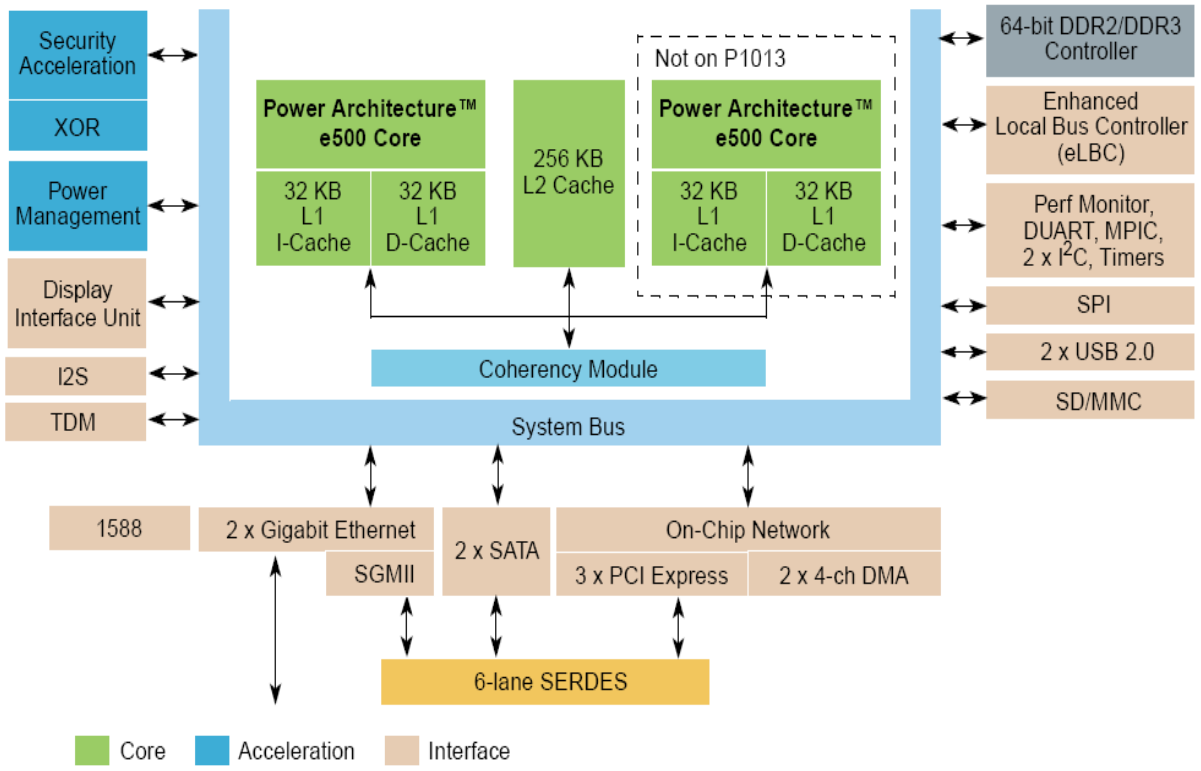
- Dual e500 cores, built on Power Architecture® technology
  - 600 – 1066 MHz
  - 256KB Frontside L2 cache w/ECC, HW cache coherent
  - 36-bit physical addressing, DP-FPU



QorIQ P1022 Processor Overview (cont.)

System Unit

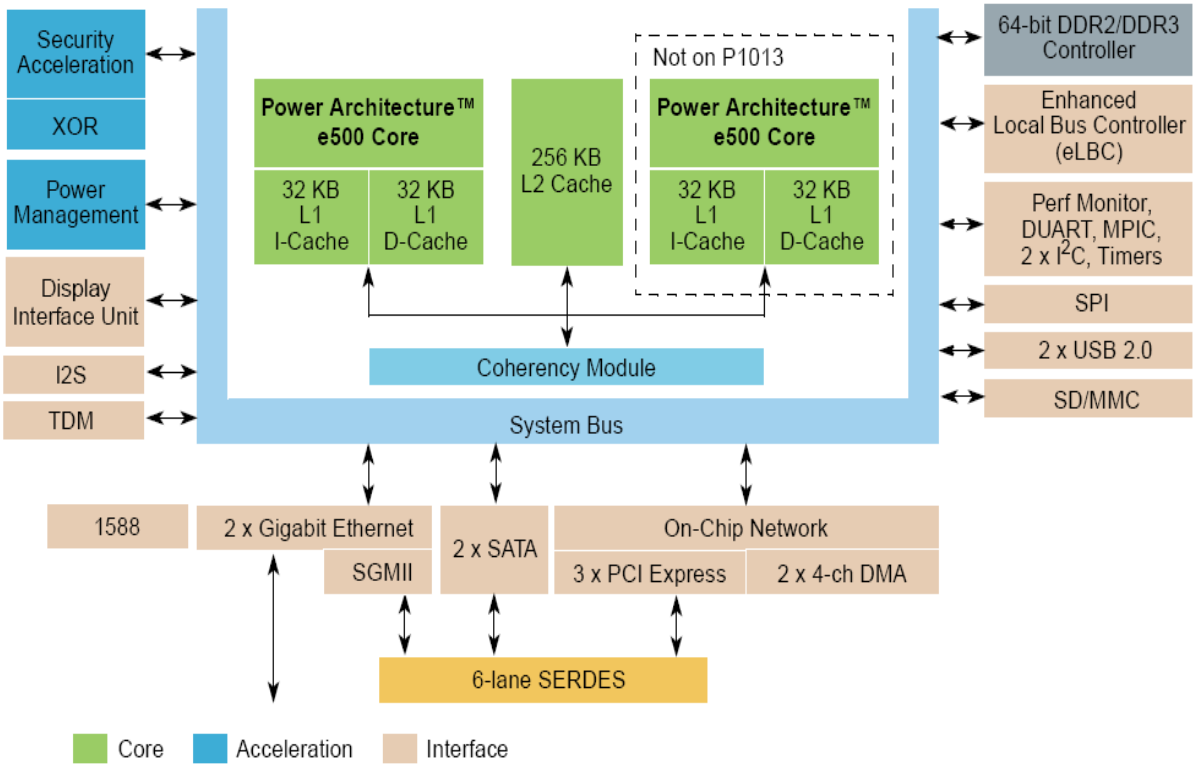
- 64-bit DDR2/DDR3 SDRAM memory controller with ECC support
- Two 10/100/1000 Mbps enhanced three-speed Ethernet controllers
- High-speed interfaces
  - Six SerDes lanes running up to 2.5 GHz (multiplexed across controllers)
  - One x4 and two x1 PCI Express® interfaces
  - Two serial ATA (SATA) interfaces)
  - Two SGMII interfaces
- Audio Visual interfaces
  - LCD interface supporting a display of 1280 × 1024P at 60 Hz, 24 bits per pixel
- Two high-speed USB controllers (USB 2.0)
- Enhanced secure digital host controller (SD/MMC)



- Integrated security engine (SEC) with XOR acceleration
- Programmable interrupt controller (PIC) compliant with Open-PIC standard
- Dual four-channel DMA controllers
- TDM interface supporting up to 128 channels

QorIQ P1022 Processor Overview (cont.)

- Process & Package
  - 45nm SOI, 0C to 125C Tj with -40C to 125C Tj option
  - 689-pin TePBGAII



QorIQ P1 Series Comparison

	P1020	P1021	P1022
CPU	Dual e500 Up to 800MHz 32K I/D	Dual e500 Up to 800MHz 32K I/D	Dual e500 Up to 1067MHz 32K I/D
L2 Cache	256KB	256KB	256KB
DDR I/F Type/Width	DDR2/3 32-bit	DDR2/3 32-bit	DDR2/3 32/64-bit
10/100/1000 Ethernet (with IEEE® 1588 v2)	3 w/(2) SGMII	3 w/(2) SGMII	2 w/(2) SGMII
TDM	Yes	-	Yes
PCI Express® 1.0a	2 controllers w/ 4 SerDes	2 controllers w/ 4 SerDes	3 controllers w/ 6 SerDes
USB2.0	2	1	2
Memory Card	SD/MMC	SD/MMC	SD/MMC
Other interfaces	SPI, 2xI²C, DUART	SPI, 2xI²C, DUART	SPI, 2xI²C, DUART
Accelerators	SEC3.3.2	SEC3.3.2	SEC3.3.2
QUICC Engine	-	Yes	-
SATA	-	-	2
DIU	-	-	1
Audio (SSI)	-	-	1
Package	689-pin TePBGAII	689-pin TePBGAII	689-pin TePBGAII

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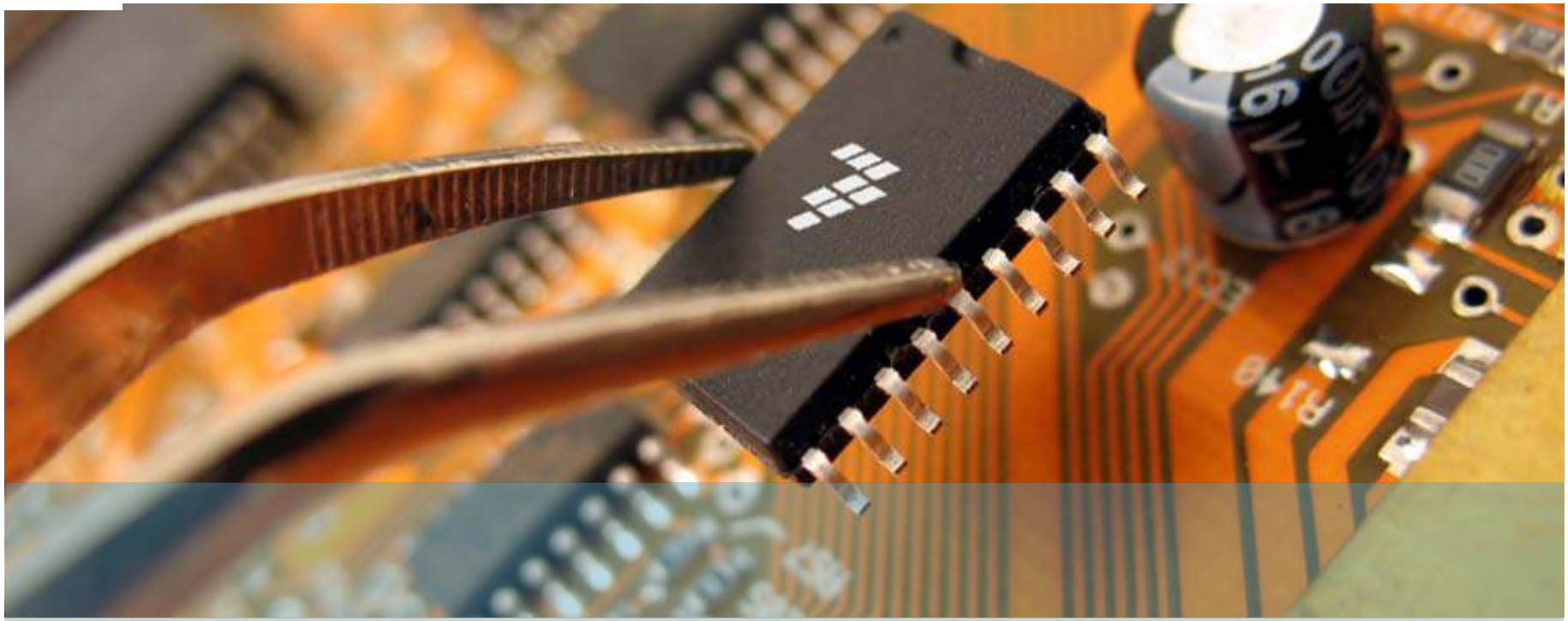

Markets and Applications

QorIQ P1020, P1021 and P1022 Processors

Target Applications

- Networking (switches and routers)
  - Line card controller
  - Mid-range line card control plane
  - Low-end line card combined control and data plane
  - Shelf controller
  - Business gateway
  - Multiservice router
  - Wireless access points
- Telecom
  - AMC card
  - Controller on ATCA carrier card
  - Channel and control card for NodeB, BTS, WCDMA, 4G LTE, WiMAX
  - General-purpose compute blade
- Industrial
  - Robotics
  - Test/measurement networking/telecom
  - Multifunction printer
  - Single-board computers
  - Industrial applications

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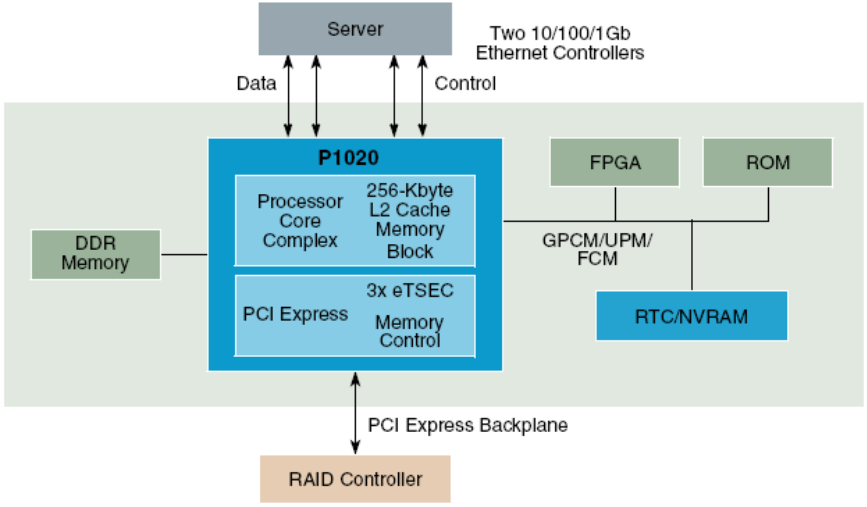
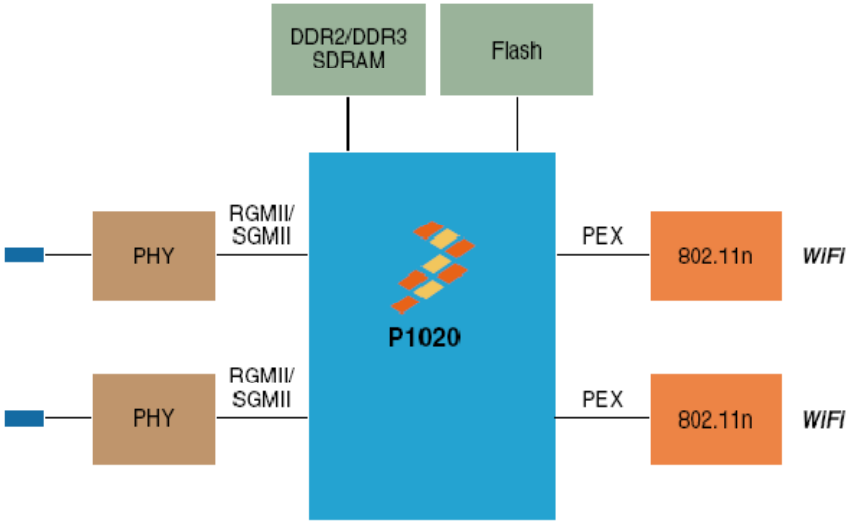
QorIQ P1020 Processor Target Application – NC/WLAN

- High-end network card used in a system area network that is enabled by PCI Express® interface

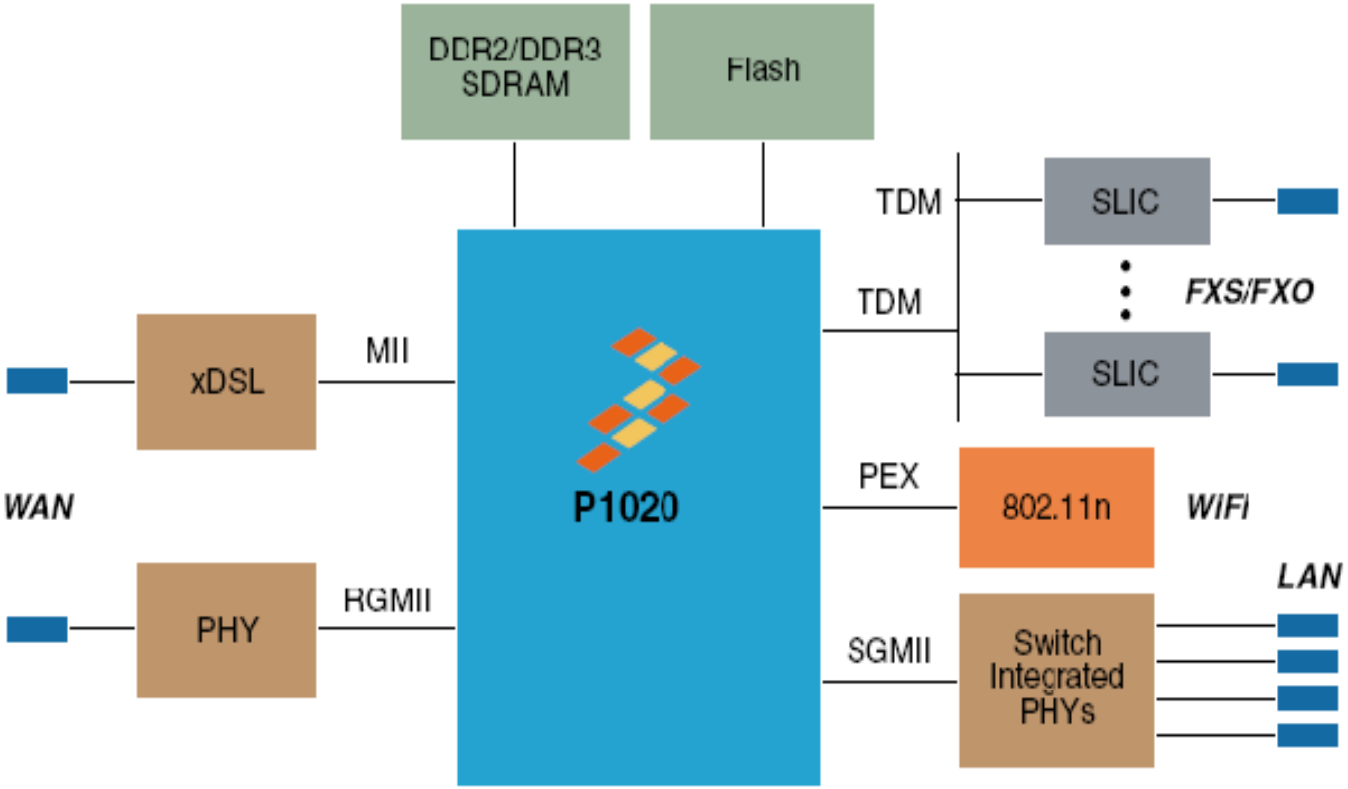


- WLAN access point application where the CPU provides the complete data and control path processing needs for multiple MAC/radio interfaces



QorIQ P1021 Processor Target Application – SMB

- This solution enables complete secure data, voice and wireless communications services in a single easy-to-manage platform
- Multi-service router or business gateway targeting small-to-medium business customer premise equipment



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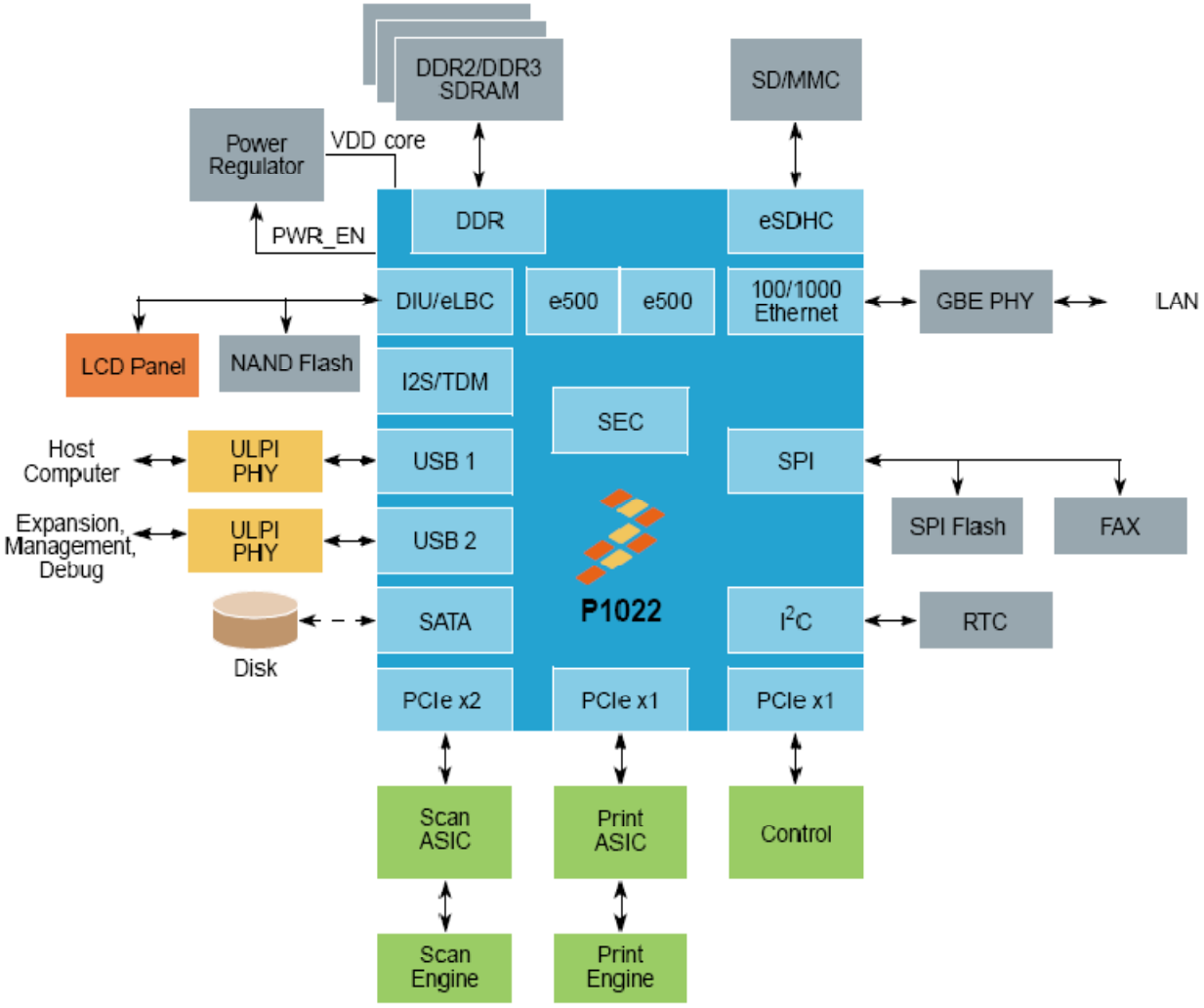
QorIQ P1022 Processor Target Application – Multifunction Printer

- In a multifunction printer (MFP), the device interfaces to external ASICs, which perform scan, print and control functions on the PCI Express® interface. However, print functions such as PDL (page description language) parsing, rasterizing the page, resize, color format conversion and half-toning are expected to be performed by the software running on the cores.



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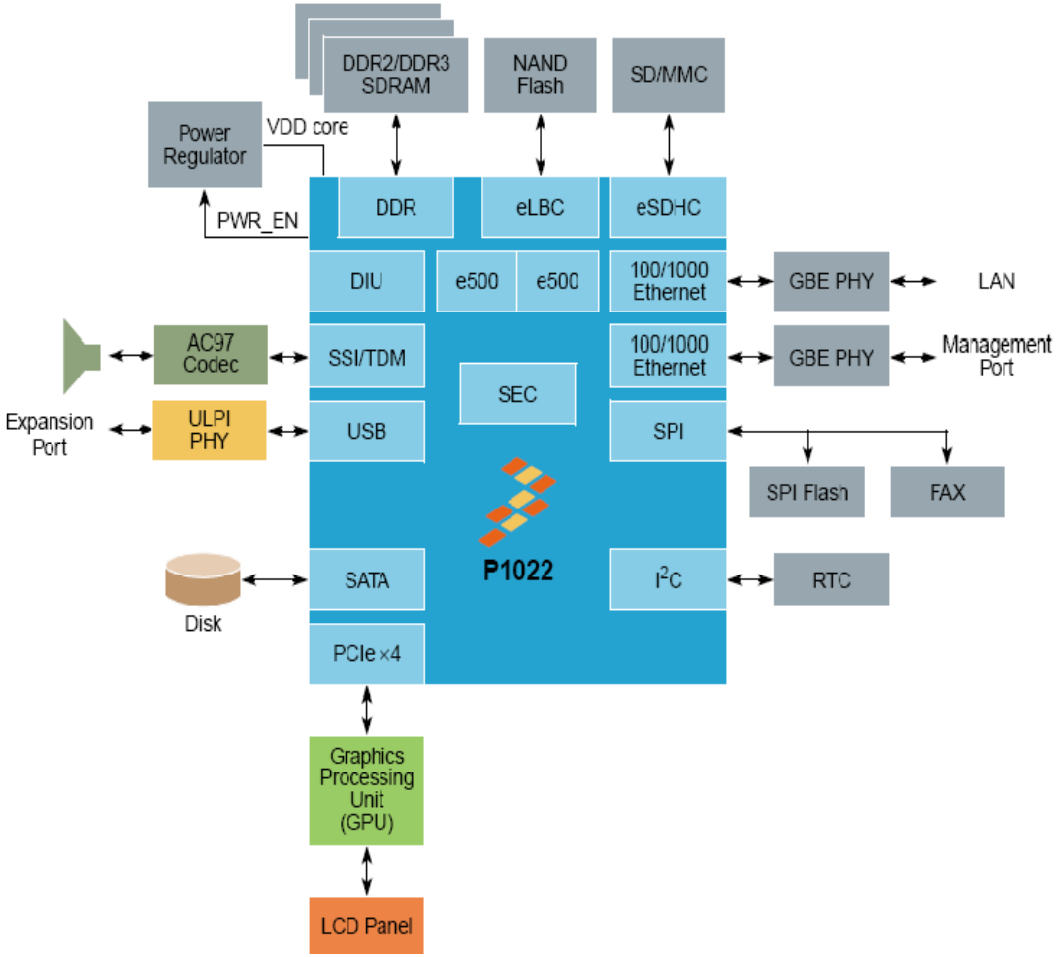
QorIQ P1022 Processor Target Applications – Digital Signage

- Compressed video streams and overlay graphics information are streamed into a graphics processing unit (GPU) connected to one of the PCI Express® ports. The GPU decodes the video stream and composes the raster with the overlay graphics to display the composed picture on the LCD panel.
- The audio decoding is performed on the P1022 CPU cores. The decoded audio samples are fed to an off-chip audio codec through the on-chip I²S interface, which converts the digital audio samples to analog signals, amplifies them, and feeds the audio signals to the speakers.
- An HDD can be connected to the SATA interface to house the encoded AV stream. Moreover, the P1022 processor supports a 64-bit DDR interface and can boot from NOR, NAND, SPI and SD/MMC interfaces.



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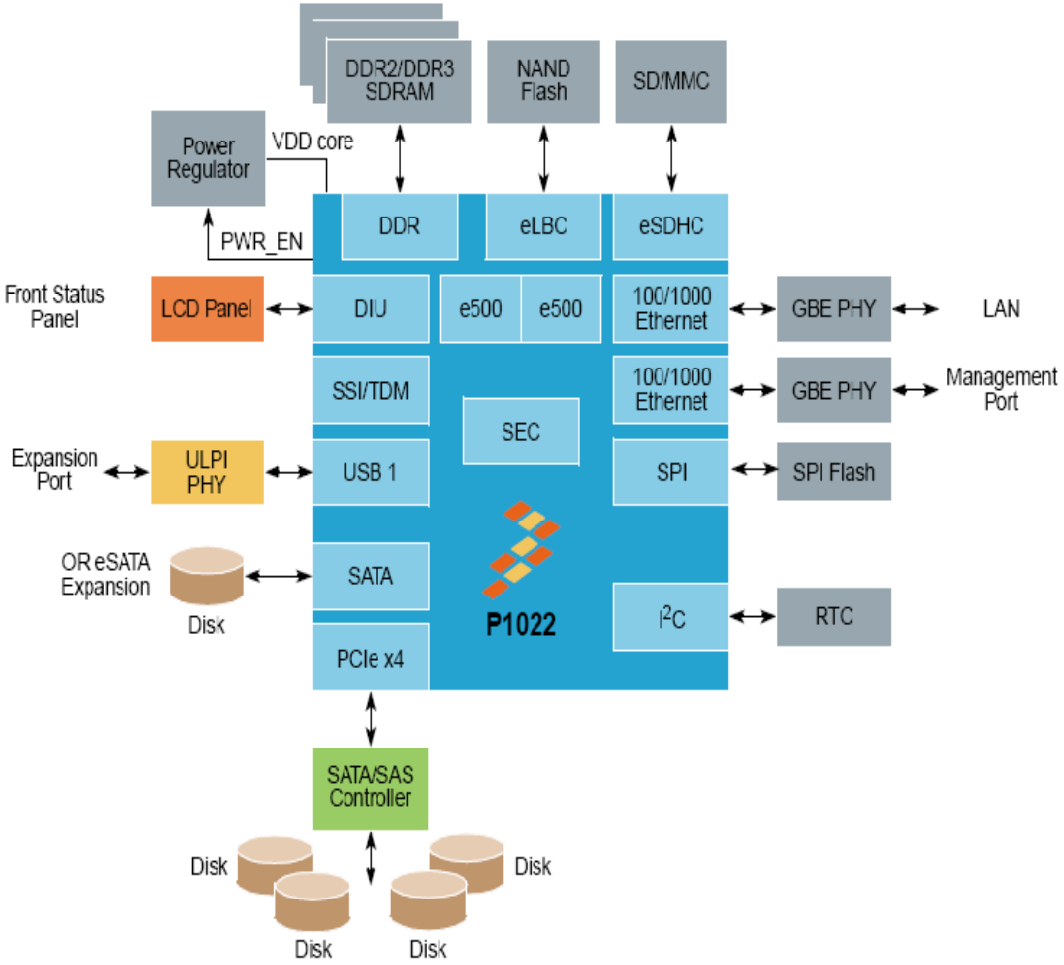
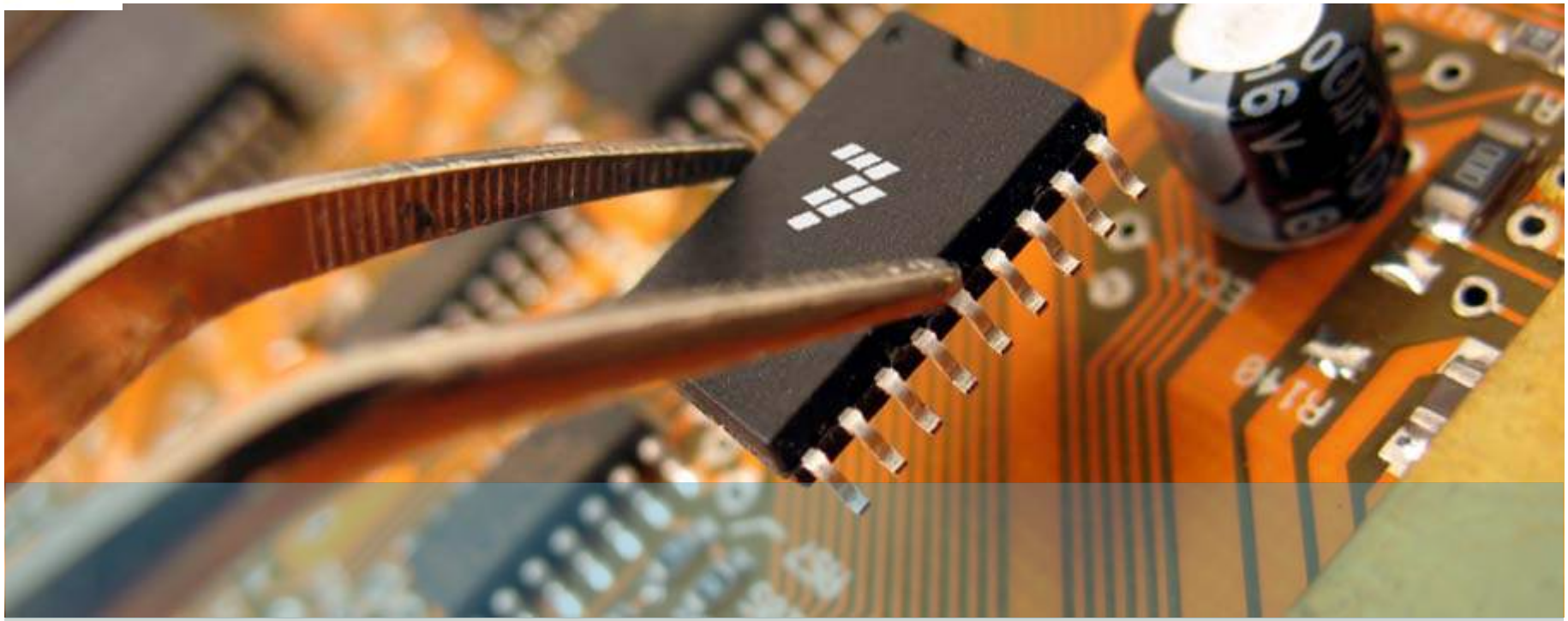
QorIQ P1022 Processor Target Applications – NAS/NVR

- Network Attached Storage (NAS) or a Network Video Recorder (NVR application built around the P1022 processor can support two file systems, either with the same operating system or different operating systems running on each core.
- The RAID stack runs on either one or both of the cores, depending on the application.





QorIQ P1020/21/22 Processor Common Subsystems

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Initialization and Boot

- P1020/21/22 core can be configured to fetch boot code from one of the following I/O interfaces:
  - Local Bus (8/16/32b port size)
  - PCI Express®
  - DDR SDRAM
  - Internal Boot ROM
- Internal Boot ROM allows customer boot code to be loaded to DRAM from SPI or SD flash memory
- As a PCI agent or PCI Express® endpoint, P1020/21/22 can also be initialized from an external host before local boot code is executed.
- I^2C Boot Sequencer can optionally perform register or memory initialization by loading data and addresses from I^2C EEPROM before P1020/21/22 is released for initial boot code fetch.

P1020/21/22 Boot Modes	
Enhanced Local Bus Controller boot	Booting the system using either Parallel NAND flash, Parallel NOR flash, Parallel NVRAM and battery-backed RAM
	x8, x16, and x32 boot device(s) via the parallel address/data bus
	Support checking/verifying ECC for NAND flash boot blocks during the boot process
PCIe Boot	Boot vector fetch can be routed to the PCI Express interfaces if external boot ROM is located on any of those interfaces
SPI Boot	Device Boot from SPI Flash and 16-bit/24-bit address SPI EEPROM (Master mode only)
SD Boot	Supports boot from both SDC and MMC cards
I^2C Boot	Support for optionally loading configuration data from serial ROM at reset via the I^2C interface, which can be used to initialize configuration registers and/or memory
	Support for extended I^2C addressing mode
	Support for checking/verifying ECC during the boot process

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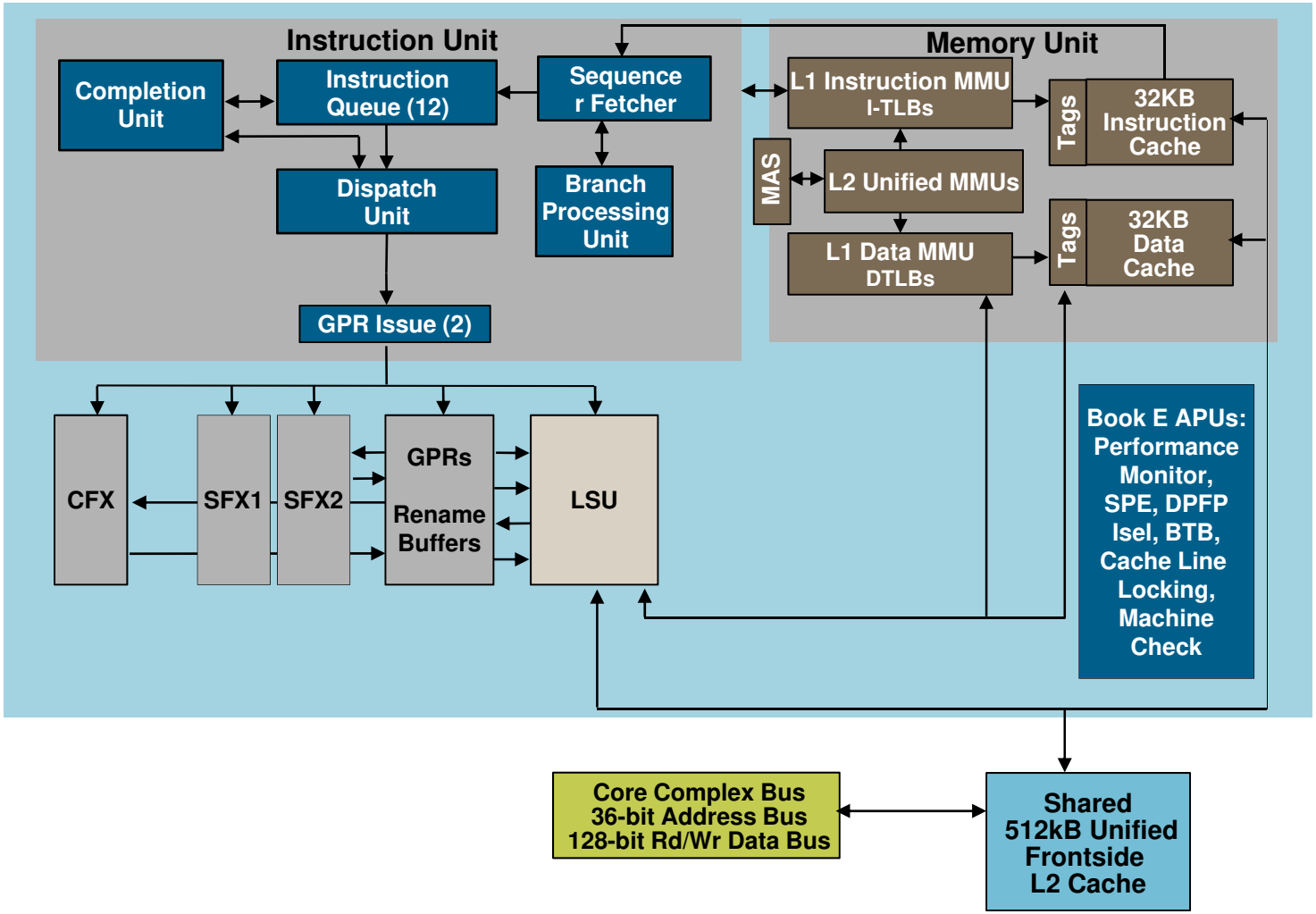
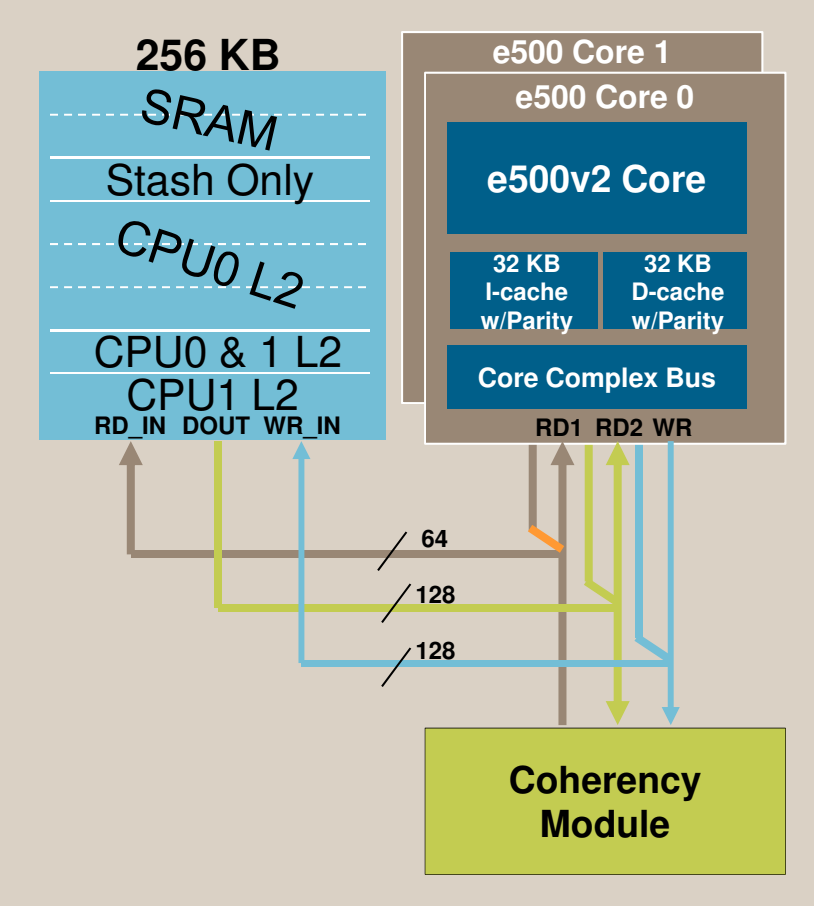
e500v2 Core Architecture



- Up to 1.2 GHz
- L1: 32KB, 8-way set associative, parity
- L2: Front Side: 8-way set associative, ECC
- Cache line locking supported
- MESI cache coherence
- Peak IPC 2 Instructions plus 1 branch
- Out of Order Execution
- Multiple Book E APUs
- 16 TLB SuperPages
- 512-entry 4K Pages
- 36-bit Physical Address

L2 Cache Controller

- Shared 256 KB unified frontside L2 cache w/8-way associativity (each way: 64 KB)
- Assignment Granularity:
  One, two, four, or all eight “ways” of the cache can be assigned as the following:
  - SRAM
  - Stash-Only
  - CPU0 L2 Only
  - CPU1 L2 Only
  - Both CPU0 and CPU1 L2
- Stash-Only regions can now be defined
  - Prevents stash data from polluting processor data and vice-versa
  - One, two or four “ways” of the cache can be dedicated as Stash-Only
- Stash Allocate Disable mode added
  - Allows update of all resident cache lines without allocation of new lines



Example

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eTSEC: Enhanced Triple-Speed Ethernet Controller

Code compatible with PowerQUICC III TSEC

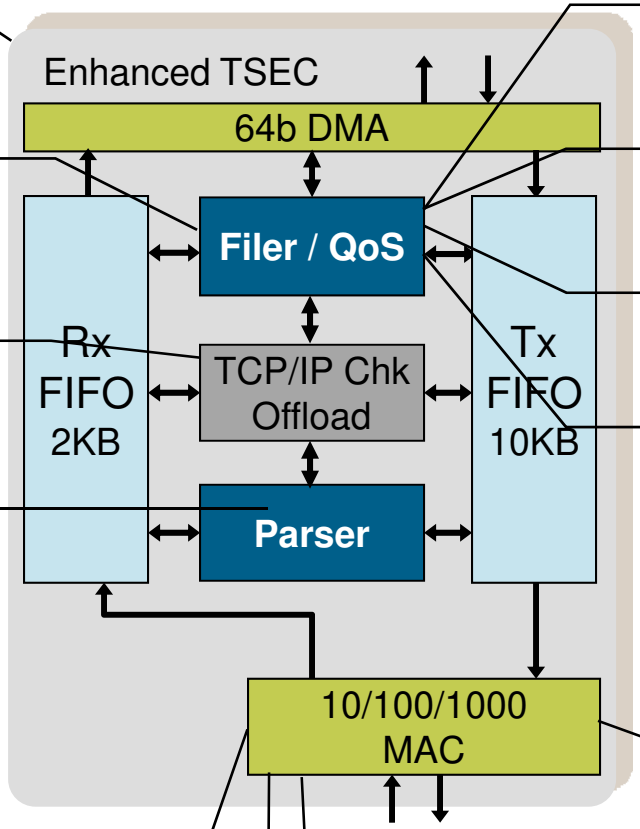
Support for weighted round robin and strict priority queueing

TCP/IP checksum offload for RX and TX

IPv6 and Magic Packet support

Support VeTSEC

RMII, RGMII Interface Support



SGMII Interface Support

IEEE® 1588 Hardware Support

QoS support for 8 Rx and 8 Tx H/W queues

Programmable IP header alignment

Customizable per-packet rejection

Customizable per-packet filtering/filing to 64 logical receive queues.
Examples: 802.1p, IP TOS, Diffserv classification, TCP/UDP ports, etc.

Layer 2 features:
- VLAN insertion and deletion per frame
- 16 exact-match MAC addresses
- Increased hash table address matching

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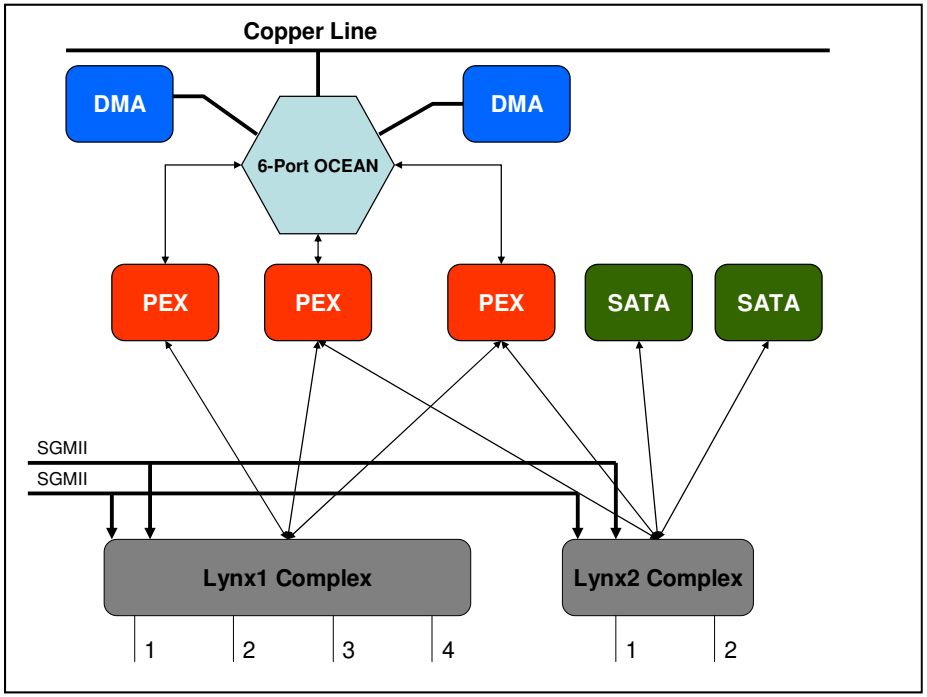
eTSEC Controller (cont.)

P1020/21		
eTSEC1	eTSEC2	eTSEC3
RGMII	SGMII	RGMII
None	None	SGMII

P1022	
eTSEC1	eTSEC2
SGMII	SGMII
RMII/RGMII	RMII/RGMII

Protocol	X4 Lanes P1022			
	E	F	A	B
	SGMII	SGMII	x1 PEX	x1 PEX
	SGMII	SGMII	x2 PEX	
	SGMII	x1 PEX	x1 PEX	x1 PEX
	x2 PEX		x1 PEX	x1 PEX
	x2 PEX		x2 PEX	
	x4 PEX			

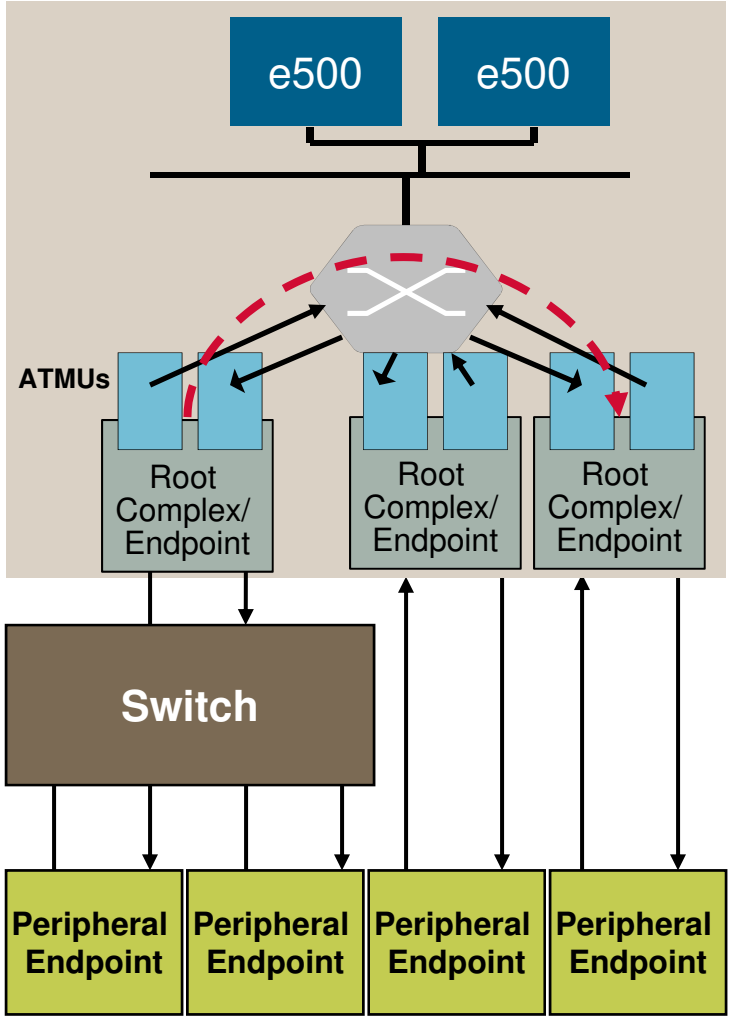


Protocol	X2 Lanes P1022	
	A	B
	x1 PEX	x1 PEX
	x2 PEX	
	x1 SATA	x1 SATA
	SGMII	SGMII

Protocol	X4 Lanes P1020/21			
	E	F	A	B
	off	off	x1 PEX	off
	x4 PEX			
	SGMII	SGMII	x1 PEX	x1 PEX
	SGMII	SGMII	x2 PEX	

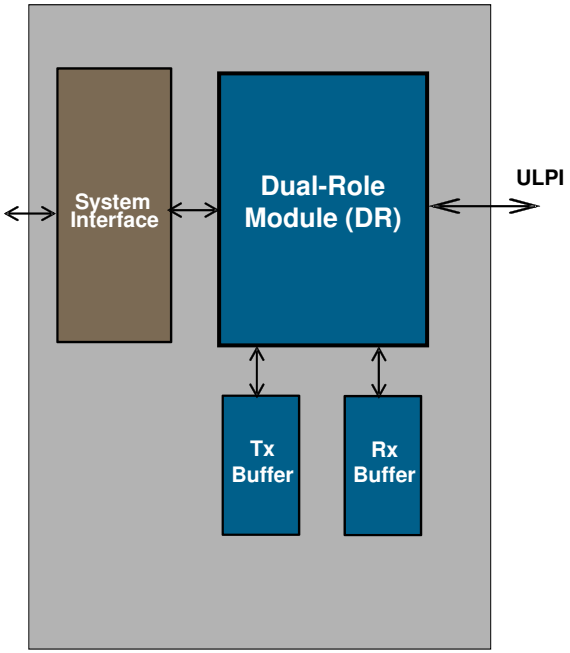
PCI Express® Interface

- PCI Express 1.0a compatible
- Supports x1, x2, and x4 link widths @ 2.5 Gbaud, 2.0 Gb/s
  - Auto-detection of number of connected lanes
- Selectable as root complex or endpoint at initialization
- 32- and 64-bit addressing into PCI Express address space
- Root complex inbound support for MSI and INTx
- Endpoint support for outbound MSI
- Reads/writes carried across ports, but not a switch
- 256 byte maximum payload size
- One virtual channel
- Strong and relaxed ordering rules
- 8 non-posted, 6 posted transactions
- 3 inbound + 1 configuration window
  - Translates upper 52b of PCI addr to upper 24b of local addr
  - Window sizes of 4 KB to 64 GB
  - Settings: read/write type, prefetchable, and target
  - 1 MB Config window maps to CCSR region
- 4 outbound + 1 default window
  - Translates upper 24b of local addr to upper 52b of PCI addr
  - Select I/O or memory for reads and writes
  - Window sizes of 4 KB to 64 GB



USB Controller

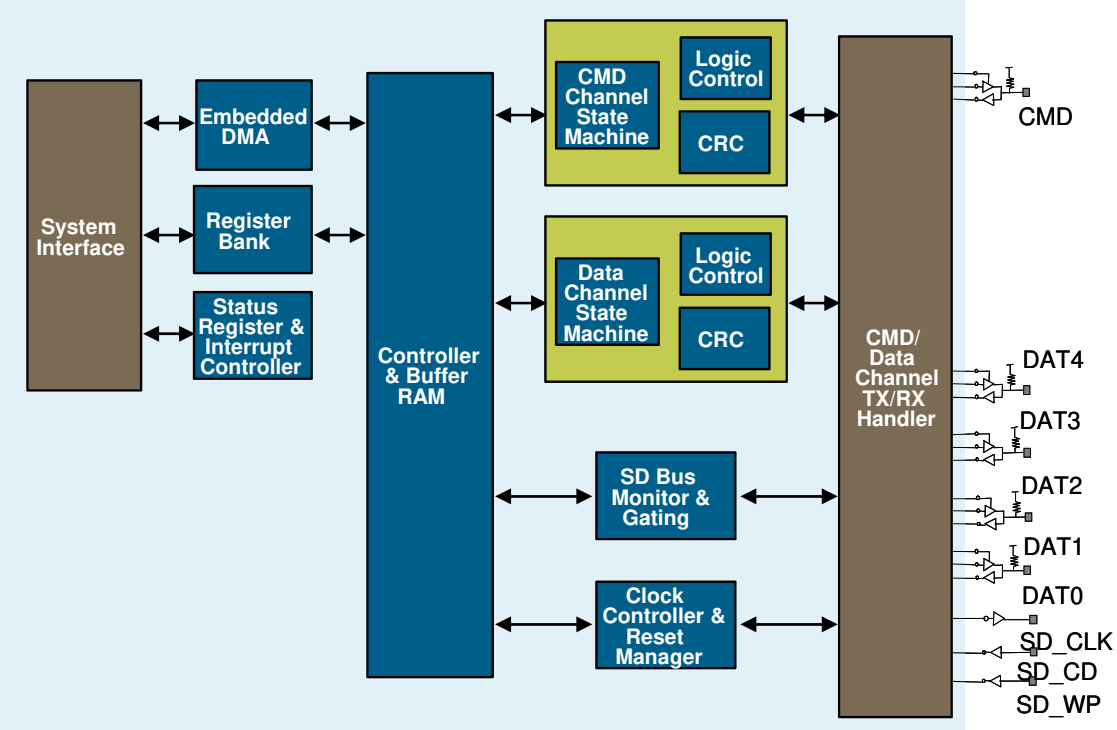
- Complies with USB specification rev 2.0
  - High Speed (HS) = 480 Mbit/s
  - Full Speed (FS) = 12 Mbit/s
  - Low Speed (LS)= 1.5 Mbit/s
- EHCI Compliant
- Hi-Speed, Full-speed and Low-speed
- USB dual role controller
  - Device controller
    - Six programmable USB bi-directional endpoints
  - Host controller
    - USB root hub with one downstream facing port
    - EHCI compatible
- Supports external USB PHYs
  - ULPI (UTMI+ Low Pin Interface)
  - Full Speed Serial



USB Controller

eSDHC Controller

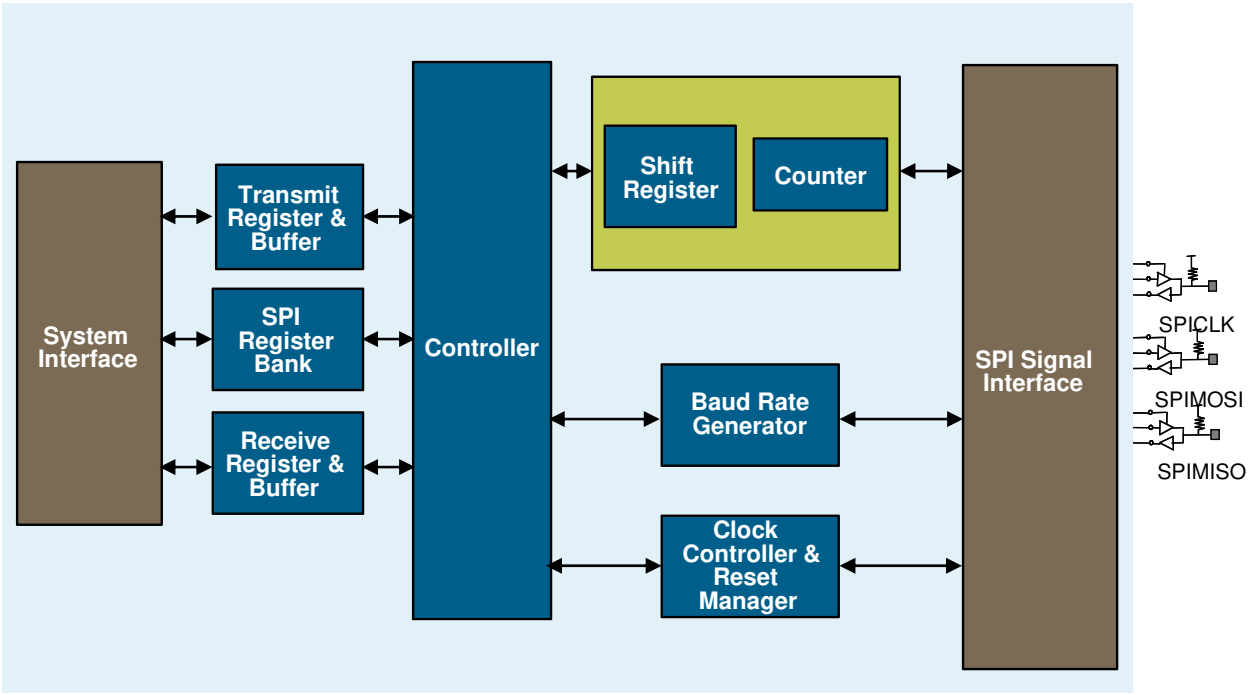
- Works with SD/MMC cards
- Supports SD 1-bit/4-bit cards,
  - SD Memory Card Specification version 2.0, support High Capacity SD Memory Card
  - SD Host Controller Std Spec, Ver 2.0
- Supports MMC 1-bit/4-/8-bitcards
  - Compatible with the MMC System Specification version 4.0
- Supports Single Block, Multi Block read and write
- Supports Auto CMD12 for multi-block transfer
- Host can initiate non-data transfer command while data transfer is in progress
- Supports SDIO Read Wait and Suspend/Resume operations



Esdhc Controller

eSPI Controller supports:

- Full- and half-duplex operation
- eSPI master and RapidS full clock cycle operation support
- 32 Byte TX and 32 Byte RX Buffers
- 16 and 24 bit Addressing
- Supports a range from 4-bit to 16-bit data characters
- Supports back-to-back character transmission and reception
- Supports single master SPI mode
- Independent programmable baud rate generator
- Programmable clock phase and polarity
- 4 Chip Selects
- Local loopback for testing



SPI Controller

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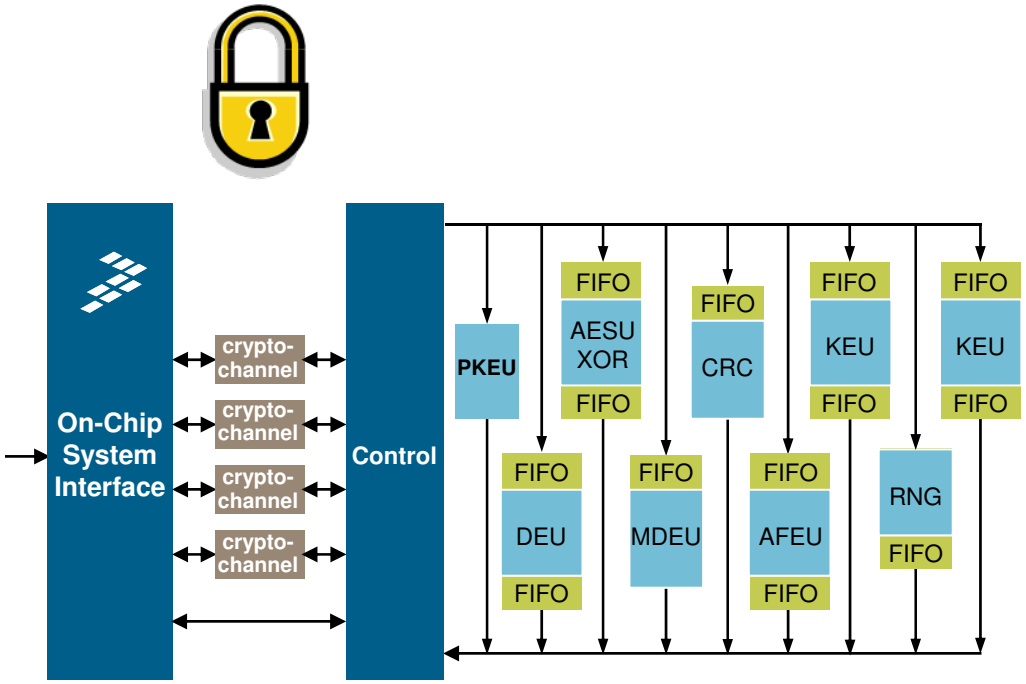
Security Engine – SEC 3.3.2

- Public Key Execution Unit supports:
  - RSA and Diffie-Hellman (to 4096b)
  - Elliptic curve cryptography (1023b)
  - Supports Run Time Equalization
- DES Execution Unit
  - DES, 3DES (2K, 3K)
  - ECB, CBC, OFB modes
- AES Execution Unit
  - Key lengths of 128, 192, and 256b
  - ECB, CBC, CTR, CCM, GCM, CMAC, OFB, CFB, and XTS
- Message Digest Execution Unit
  - SHA-1 160-bit digest
  - SHA-2 256-bit digest
  - SHA-384/512
  - MD5 128-bit digest
  - HMAC with all algorithms
- Snow 3G Execution Unit (STEU)
  - Implements Snow 3GPP
- CRC Execution Unit
  - CRC32, CRC32C
- XOR acceleration
- Random Number Generator
- Multi-OS friendly



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Enhanced Local Bus Controller (eLBC)

- Multiplexed 32/28/26-bit address and 16-bit data operating up to 83 MHz
- Four chip selects support four external slaves
- Odd/even parity checking
- Write protection capability
- Parity byte-select
- General-purpose chip-select machine (GPCM)
  - Compatible with SRAM, EPROM, FEPROM, and peripherals
  - Global (boot) chip-select available at system reset
  - Boot chip-select support for 8- and 16-bit devices
  - Minimum 3-clock access to external devices
  - Two byte-write-enable signals (LWE[0:1])
  - Output enable signal (LOE)
  - External access termination signal (LGTA)

Enhanced Local Bus Controller (eLBC) – cont'd

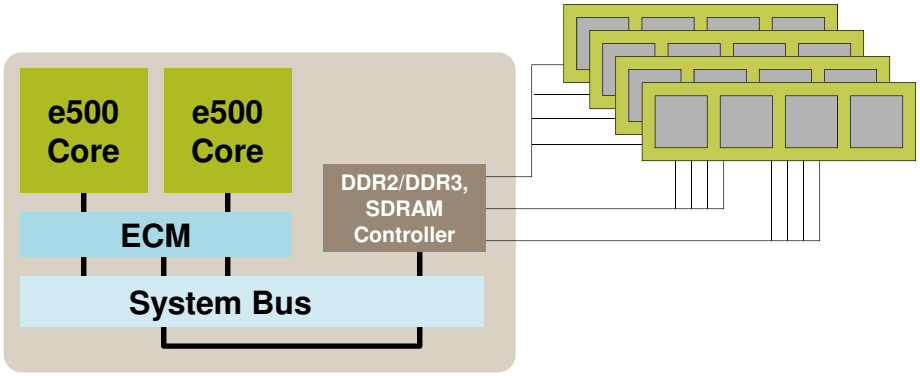
- Three user-programmable machines (UPMs)
  - Can be programmed to support to ZBT and NoBL SRAMs, NAND and NOR Flash and Compact Flash
  - Programmable-array-based machine controls external signal timing with a granularity of up to one-quarter of an external bus clock period
  - User-specified control-signal patterns can be initiated by software
  - Support for 8- and 16-bit devices

Enhanced Local Bus Controller (eLBC) – cont'd

- NAND Flash Control Machine (FCM)
  - Support for small page (512 data bytes + 16 spare bytes) and large page (2,048 data bytes + 64 spare bytes) parallel NAND flash E2PROM devices
  - Support for hardware-based ECC checking and generation
  - Global (boot) chip-select available at system reset, with 4 Kbytes boot block buffer for execute-in-place boot loading
  - Boot chip-select support for 8-bit devices
  - Dual 2-Kbyte/eight 512-byte buffers allow simultaneous data transfer during flash reads and programming
  - Interrupt-driven block transfer for reads and writes
  - Support for user-programmable command and data transfer sequences of up to eight steps
  - Support for proprietary flash interfaces through generic command and address registers
  - Block write locking to ensure system security and integrity
  - Support for checking/verifying ECC for NAND flash boot blocks

Memory Controller

- DDR2 and DDR3
- 64-bit (72 bits with ECC)
- 32-bit (40 bit with ECC)
- 4 chip selects
- Support for up to 4 Gb devices, x8, x16, x32 configurations
- Up to 4 GB DIMMs per bank
- Up to 16 GB
- Supports self-refresh mode
- Battery backup
- Initialization bypass
- Chip-select interleaving
- Automatic DRAM initialization
- Error injection



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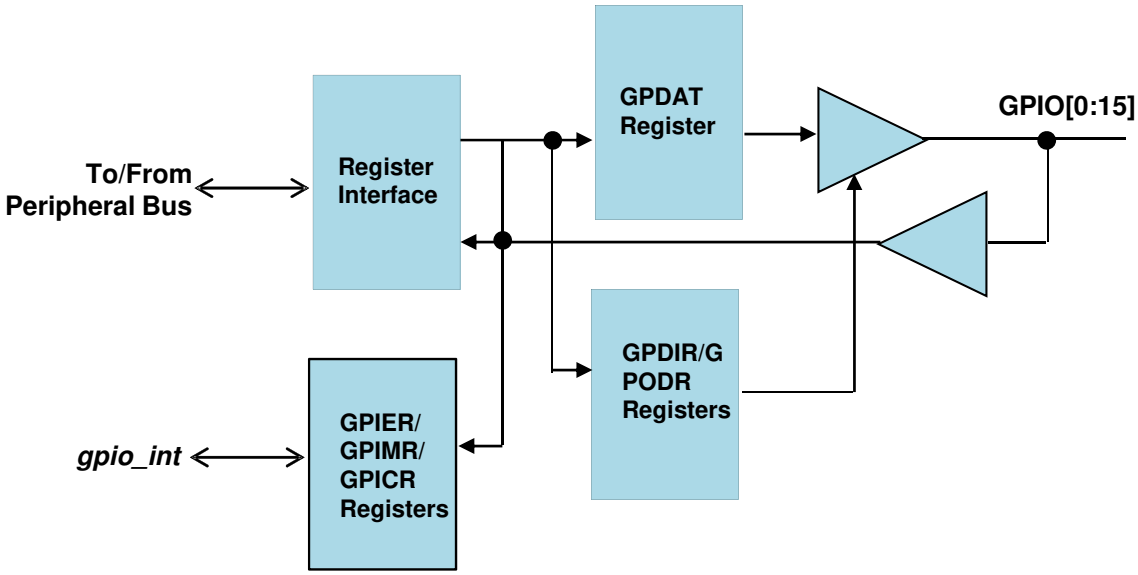
GPIO Function

- The GPIO features:
  - 16 input/output ports
  - All GPIO signals are configured as inputs when the device comes out of reset and also when HRESET is asserted.
  - Open-drain capability on all ports
  - All ports can optionally generate an interrupt



GPIO Block Diagram

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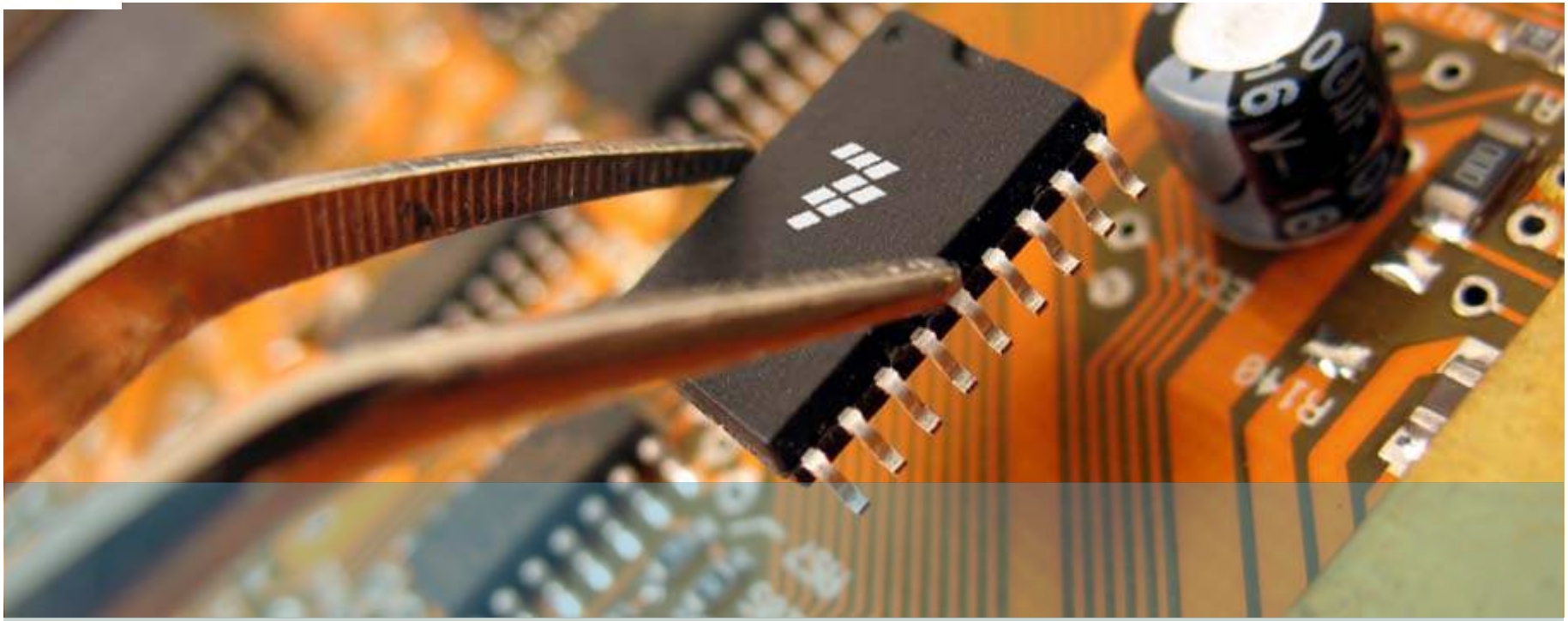
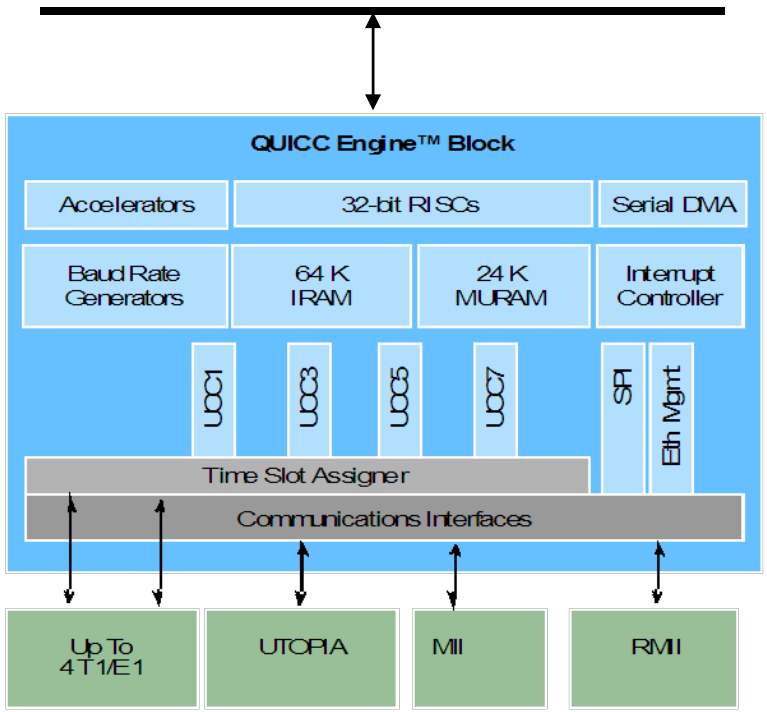


QorIQ P1021 Processor Subsystem

QUICC Engine Subsystem

- One 32-bit RISC controller for flexible support of the communications peripherals
- Serial DMA channel for receive and transmit on all serial channels
- Four universal communication controllers (UCCs) supporting the following protocols and interfaces (not all of them simultaneously):
  - Two 10/100 Mbps Ethernet/IEEE Std. 802.3 Interfaces, using RMII
  - ATM protocol through UTOPIA
  - HDLC and Transparent controllers up to 70 Mbps full-duplex; HDLC bus up to 10 Mbps
  - UART and asynchronous HDLC BISYNC up to 2 Mbps
  - QUICC multi-channel controller (QMC) for 128 TDM channels
- One UTOPIA L2 interface supporting 31 multi-PHY addresses
- One serial peripheral interfaces (SPI)
- Four TDM interfaces, with T1/E1/J1/E3 or DS-3 serial interfaces



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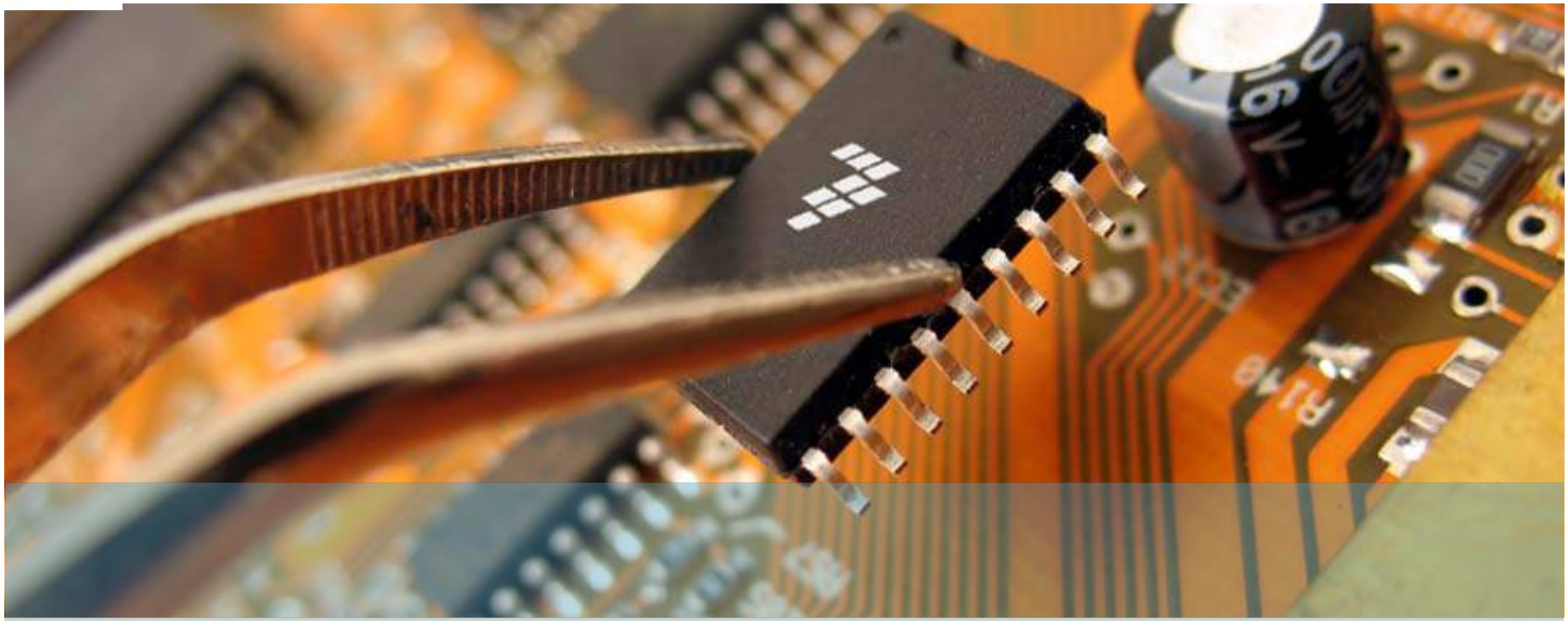
Protocols Supported Through QUICC Engine Subsystem

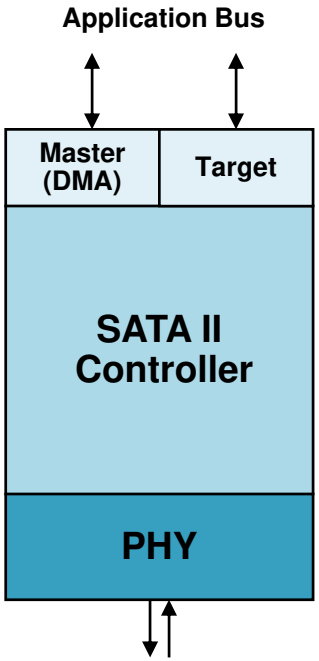
- ATM SAR up to 155Mbps (OC-12) full duplex, with ATM traffic shaping (ATF TM4.1) for up to 256 ATM connections
- ATM AAL1 structured and unstructured circuit emulation service (CES 2.0)
- IMA and ATM transmission convergence sublayer
- ATM OAM handling features compatible with ITU-TI.610
- PPP, multi-link (ML-PPP), multi-class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686, 3153
- IP termination support for IPv4 and IPv6 packets including TOS, TTL and header checksum processing
- Support for ATM statistics and Ethernet RMON/MIB statistics.
- 128 channels of HDLC/Transparent or 64 channels of SS7
- Up to 4 TDM ports
- IEEE® 1588 V2 support
- RAM based microcode



QorIQ P1022 Processor Subsystems

Dual SATA II Controller

- Supports Host SATA I per Rev 1.0a of the spec
  - OOB
  - Port Multipliers
  - ATAPI 6+
  - Spread Spectrum clocking on Receive
- Support for SATA II Extensions
  - Asynchronous Notification
  - Hot Plug including Asynchronous Signal Recovery
  - Link Power Management
  - Native Command Queuing
  - Staggered Spin-up and
  - Port Multiplier support
- Support for SATA I and II data rates
  - 1.5 & 3.0 Gbaud
- Standard ATA Master-only Emulation
- Includes ATA Shadow Registers
- Implements SATA superset registers
  - SError, SControl, SStatus
- Interrupt driven
- Power management support
- Error handling and diagnostic features
  - Far end/Near end loopback
  - Failed CRC error reporting
  - Increased ALIGN insertion rates
  - Scrambling and CONT override



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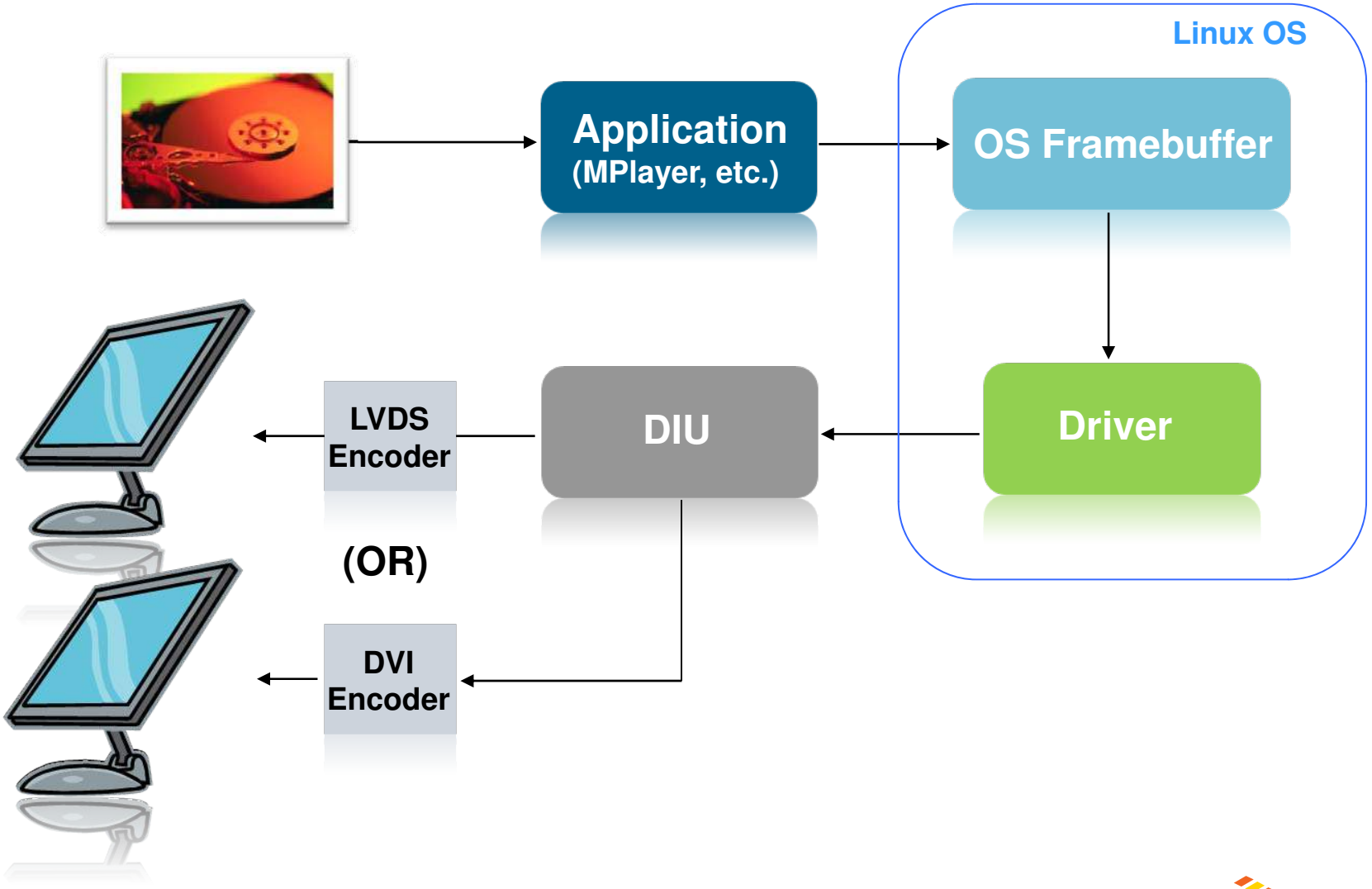
Display Interface Unit Software/Hardware Interaction



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Display Interface Unit Capabilities

Display Type	Resolution	Max Refresh Rate	Max Planes
SXGA	1280 x 1024	Up to 60 Hz	Only 1
XGA	1024 x 768	Up to 72 Hz	Up to 3
WVGA	854 x 480	Up to 72 Hz	Up to 3
SVGA	800 x 600	Up to 72 Hz	Up to 3
VGA	640 x 480	Up to 72 Hz	Up to 3
QVGA	320 x 240	Up to 72 Hz	Up to 3

- Parallel TTL Display Interfaces
- Red/Green/Blue (RGB) and 256-level grayscale input pixel format
  - 24 bits/pixel (bpp)
- Programmable bit order definition
  - Up to 8 bits per component
- Hardware cursor
  - 32 x 32 pixels, 16 bits/pixel
- Up to 256 levels α-blending
- Chroma Keying selectable by range
- Independent programmable Gamma adjustments for each color component
- Memory write-back mode to store intermediate results, virtually extending the number of graphics planes
- 5 Operating Modes

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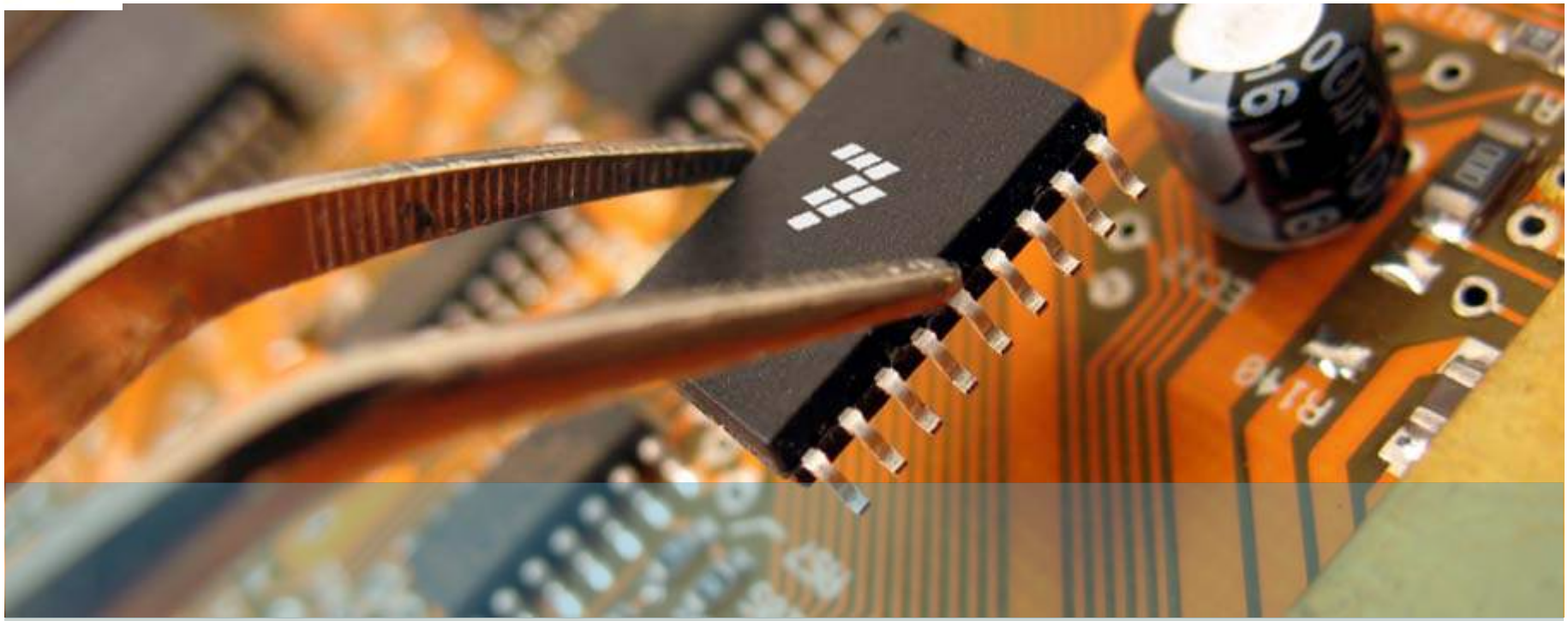
Audio I/O: Synchronous Serial Interface (SSI)

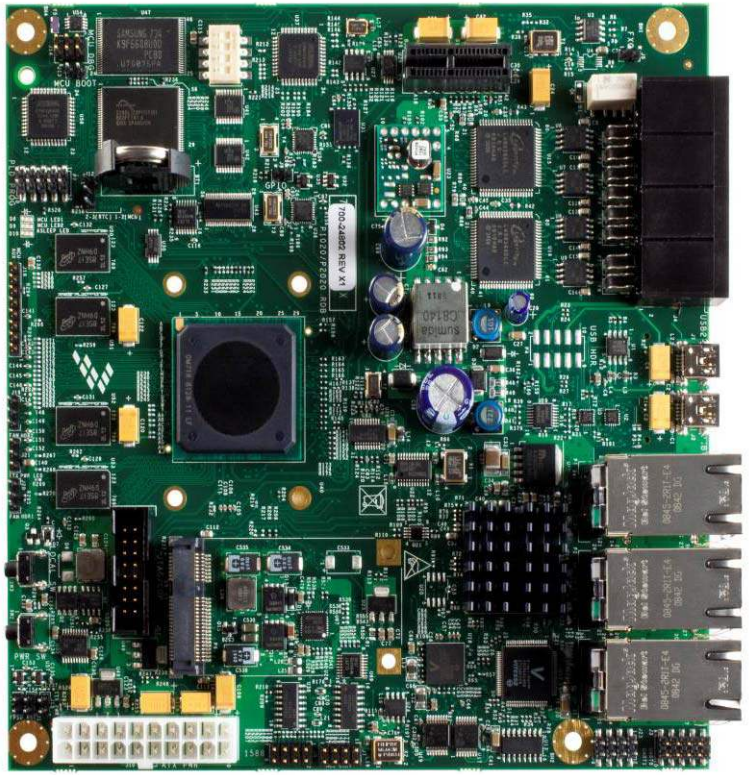
- SSI is a full-duplex, serial port that can communicate with:
  - Popular industry audio CODECs that implement the inter-IC sound bus
    - I^2S standard
    - Intel AC97standard
  - Standard CODer-DECoders (CODEC)
  - Digital Signal Processors (DSP)
  - Microprocessors
  - Peripherals



QorIQ Development Boards

QorIQ P1020 Development Board

- Customer Reference Design Board “RDB” that supports both P1020 and P2020 Silicon
  - P1020 at 800 MHz
  - 32 Bits DDR2 at 667 MHz data rate for P1020
  - Triple Gigabit Ethernet supporting RGMII and SGMII
  - PCI Express® x2 interfaces
  - USB 2.0 for High/Full speed
  - NOR/NAND flash memory
  - SD/MMC connector
  - TDM Interface with SLIC/SLAC
- Freescale Software
  - Linux® OS, U-boot, and CodeWarrior tools support
- Collateral
  - RDB Platform Reference Manual
  - Quick Start Guide



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QorIQ P1021 Development Board

- Customer Modular Design System Board “MDS”
  - P1021 at 800 MHz
  - 32 Bits DDR3 at 800MHz date rate
  - Triple Gigabit Ethernet supporting GMII and SGMII
  - PCI Express® x2 interfaces
  - USB 2.0 for High/Full speed
  - NOR/NAND flash memory
  - SD/MMC connector
  - TDM Interface with SLIC/SLAC
  - QUICC Engine Interface:
    - UTOPIA
    - T1/E1 Framers
    - Two 10/100 MII Ethernet I/F
- Freescale S/W
  - Linux® OS, U-boot, and CodeWarrior tools support
  - CodeWarrior utilities drivers support (Bare-board drivers)
- Collaterals
  - MDS Platform Reference Manual
  - Quick Start Guide

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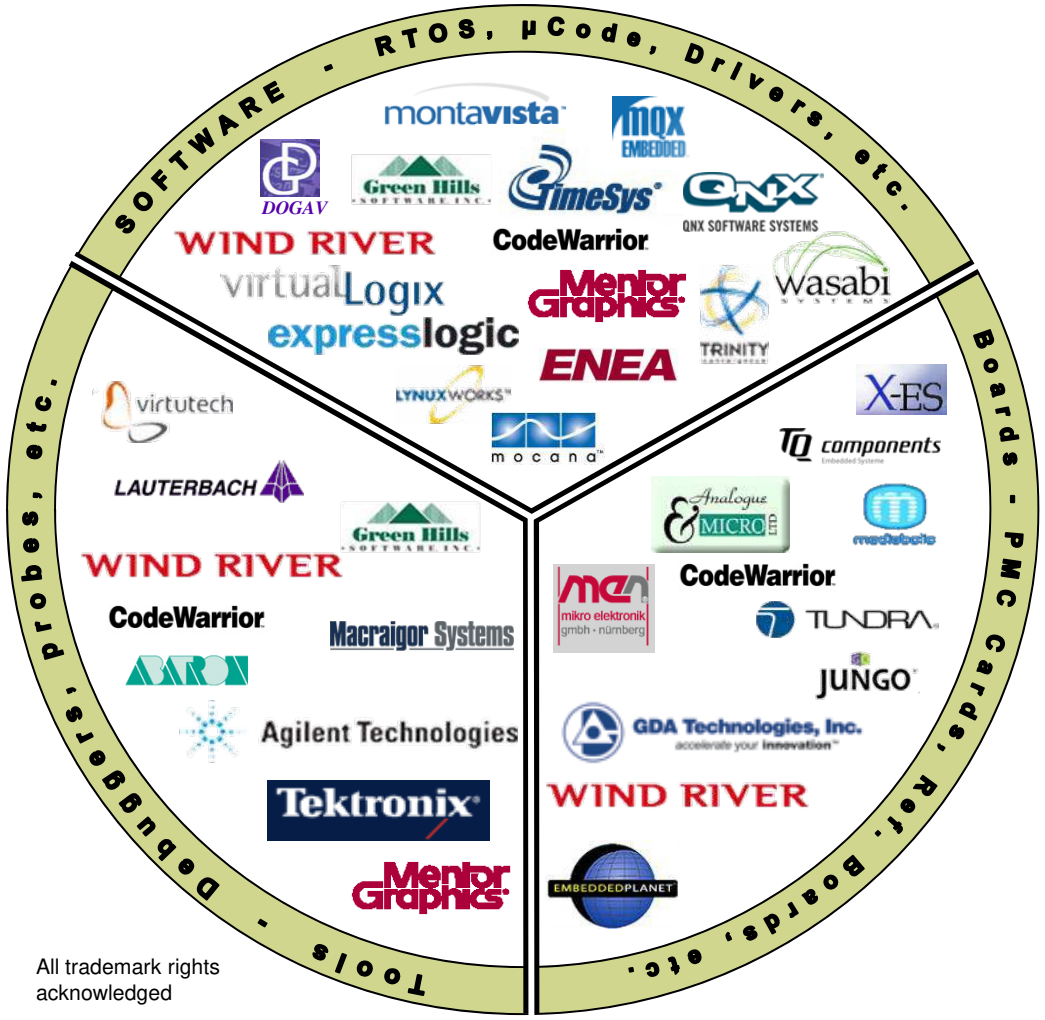
Leading Embedded Ecosystem



All trademark rights acknowledged

- Pre-silicon
  - Functional simulation
  - I/O simulation
  - Power simulation
- Software
  - Operating systems
  - Application stacks
  - Protocol acceleration
  - Development services
- Board offerings
  - Custom off the shelf
  - Standard product
  - Various form factors
  - Integration design services
- Development
  - Integrated development environments
  - Debuggers
  - Compilers
  - Probes

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Summary

Features	Benefits
Best in class ecosystem	Faster time to market
Migration path	Improved performance/watt/$ migrating from PowerQUICC II, PowerQUICC II Pro, and PowerQUICC III
High performance e500 2.4MIPS/MHz Power Architecture® core	High efficiency and frequency cores means fewer cores to get the job done
Best-in-class power	Enables fanless, “green” and low cost designs, improves reliability
Integrated Ethernet, TDM, USB, SD Flash controller, IEEE1588®, PCI Express, QUICC Engine, SATA	Flexibility to address a wide range of applications and reduced system cost
6x performance range in a single package	Common hardware platform to enable wide range of system performance
Dual and single cores	Move to dual core at your own pace without hardware changes

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