5-V PECL-to-TTL Translator

FEATURES

- **3ns (TYP) Propagation Delay**
- **Operating Range: V_{CC} = 4.2 V to 5.7 V with GND = 0 V**
- **24-mA TTL Output**
- **Deterministic Output Value for Open Input Conditions or When Inputs < 1.3 V**
- **Built-In Temperature Compensation**
- **Drop-In Compatible to the MC10ELT21, MC100ELT21**

APPLICATIONS

- **Data and Clock Transmission Over Backplane**
- **Signaling Level Conversion for Clock or Data**

DESCRIPTION

The SN65ELT21 is a differential PECL-to-TTL translator. It operates on +5-V supply and ground only. The device includes circuitry to maintain Q to a low logic level when inputs are in an open condition or < 1.3 V.

The V_{BB} pin is a reference voltage output for the device. When the device is used in single-ended mode, the unused input should be tied to V_{BB}. This reference voltage can also be used to bias the input when it is ac coupled. When it is used, place a 0.01µF decoupling capacitor between V_{CC} and V_{BB}. Also limit the sink/source current to < 0.5 mA to V_{BB}. Leave V_{BB} open when it is not used.

The SN65ELT21 is housed in an industry standard SOIC-8 package and is also available in an optional TSSOP-8 package.

PIN ASSIGNMENT

D or DGK PACKAGE
(TOP VIEW)

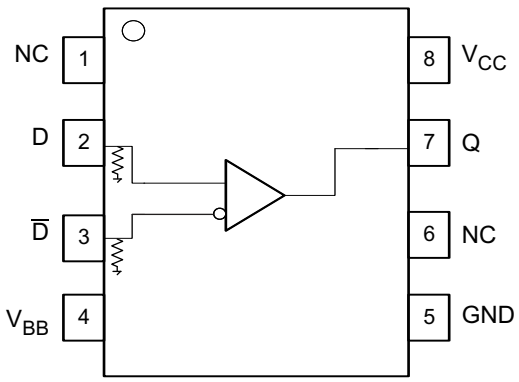


Table 1. Pin Descriptions

PIN	FUNCTION
D, $\overline{D}$	PECL data inputs
Q	TTL output
V_{CC}	Positive supply
V_{EE}	Negative supply
V_{BB}	Reference voltage output

ORDERING INFORMATION(1)(2)

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65ELT21D	ELT21	SOIC	NiPdAu
SN65ELT21DGK	SIII	SOIC-TSSOP	NiPdAu

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Leaded device options are not initially available; contact a sales representative for further details.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

PARAMETER	CONDITIONS	VALUE	UNIT
Absolute PECL mode supply voltage	V_{CC} (GND = 0 V)	6	V
Sink/source current, V_{BB}		±0.5	mA
PECL input voltage	GND = 0 V, $V_I \le V_{CC}$	6	V
Operating temperature range		–40 to 85	°C
Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	POWER RATING T_A < 25°C (mW)	THERMAL RESISTANCE, JUNCTION-TO-AMBIENT NO AIRFLOW	DERATING FACTOR T_A > 25°C (mW/°C)	POWER RATING T_A = 85°C (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
SOIC-TSSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
θ_{JB}	Junction-to-board thermal resistance	SOIC		79		°C/W
		SOIC-TSSOP		120		
θ_{JC}	Junction-to-case thermal resistance	SOIC		98		°C/W
		SOIC-TSSOP		74		

KEY ATTRIBUTES

CHARACTERISTICS		VALUE
Internal input pull-down resistor		50 kΩ
Moisture sensitivity level		Level 1
Flame ability rating (oxygen index: 28 to 34)		UL 94 V-0 at 0.125 in
Electrostatic discharge	Human body model	2 kV
	Charged-device model	1.5 kV
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test		

PECL DC CHARACTERISTICS

At V_{CC} = 5.0 V, GND = 0.0 V (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	T_A = –40°C			T_A = 25°C			T_A = 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage, single-ended		3835		4120	3835		4120	3835		4120	mV
V_{IL}	Low-level input voltage, single-ended		3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output reference voltage		3.62	3.69	3.74	3.62	3.69	3.74	3.62	3.69	3.74	V
V_{IHCMR}	High-level input voltage, common-mode range, differential	See (3)	2.2		5.0	2.2		5.0	2.2		5.0	V
I_{IH}	High-level input current				150			150			150	µA
I_{IL}	Low-level input current		0.5			0.5			0.5			µA

(1) The device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Input parameters vary 1:1 with V_{CC}. V_{CC} can vary +0.7 V / –0.8 V.
(3) $V_{IHCMR(min)}$ varies 1:1 with GND, $V_{IHCMR(max)}$ varies 1:1 with V_{CC}.

TTL DC CHARACTERISTICS

At V_{CC} = 4.2 V to 5.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCH}	Power supply current				20	mA
I_{CCL}	Power supply current				20	mA
V_{OH}	High-level output voltage	I_{OH} = –3.0 mA	2.4		See (2)	V
V_{OL}	Low-level output voltage	I_{OL} = 24 mA			0.5	V
I_{OS}	Output short circuit current		–150		–60	mA

(1) The device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) $V_{OH(max)\ level}$ is V_{CC} – 0.7.

AC CHARACTERISTICS

At V_{CC} = 4.2 V to 5.7 V, GND = 0.0 V (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	T_A = –40°C			T_A = 25°C			T_A = 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Maximum switching frequency	At Vol < 0.5V (See Figure 4)		200			200			200		MHz
t_{PLH}/t_{PHL}	Propagation delay times	At 1.5 V	2		4.5	2		4.5	2		4.5	ns
t_{JITTER}	Random clock jitter (RMS)			5	20		5	20		5	20	ps
V_{PP}	Input swing	See (3)	200		1000	200		1000	200		1000	mV
t_r/t_f	Output rise/fall times	Q (10%–90%)		750			780			910		ps

(1) The device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) R_L = 500 Ω to GND and C_L = 20 pF to GND. See Figure 1.
(3) $V_{PP(min)}$ is minimum input swing for which ac parameters are assured.

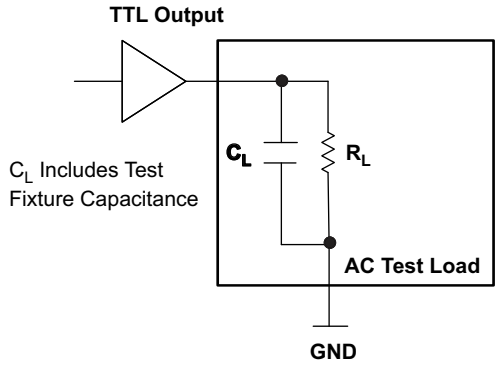


Figure 1. TTL Output AC Test Loading Condition

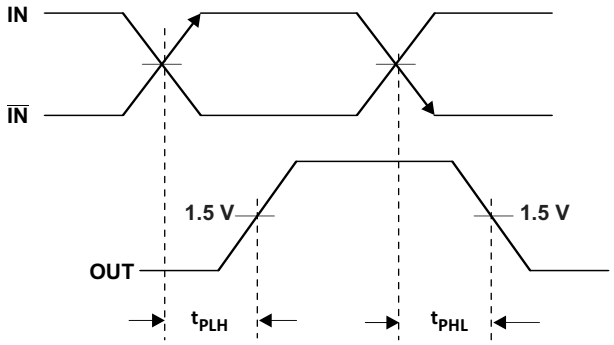


Figure 2. Output Propagation Delay

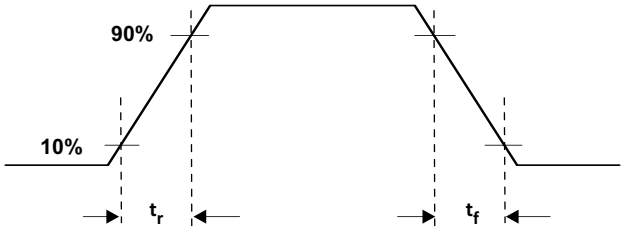


Figure 3. Output Rise and Fall Times

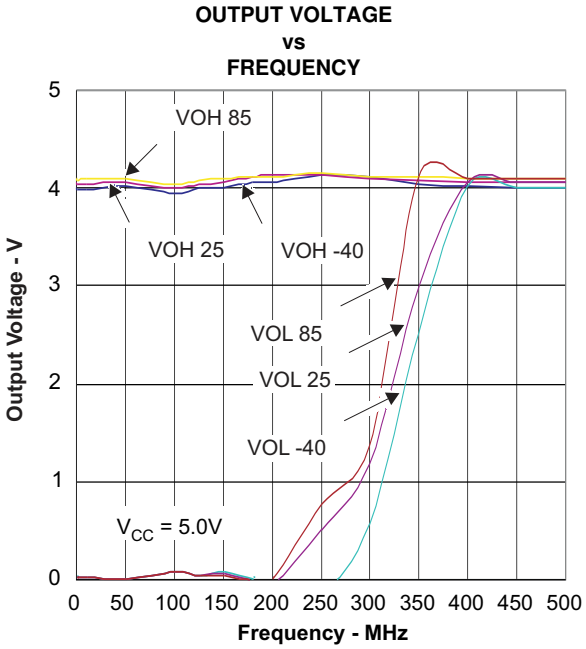

OUTPUT VOLTAGE
vs
FREQUENCY
Output Voltage - V
Frequency - MHz
VOH 85
VOH 25
VOH -40
VOL 85
VOL 25
VOL -40
V_{CC} = 5.0V
0
1
2
3
4
5
0
50
100
150
200
250
300
350
400
450
500

Figure 4.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65ELT21D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ELT21	Samples
SN65ELT21DGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIII	Samples
SN65ELT21DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIII	Samples
SN65ELT21DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ELT21	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

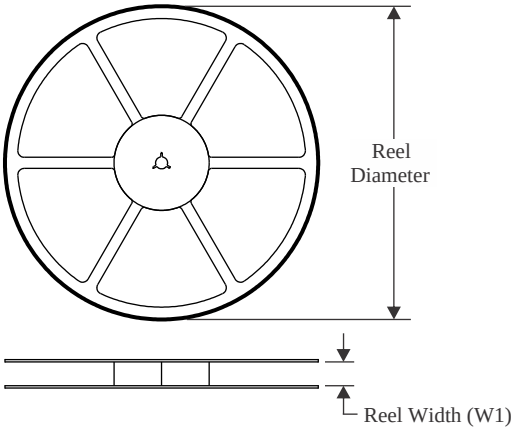
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

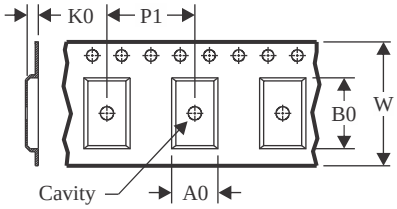
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

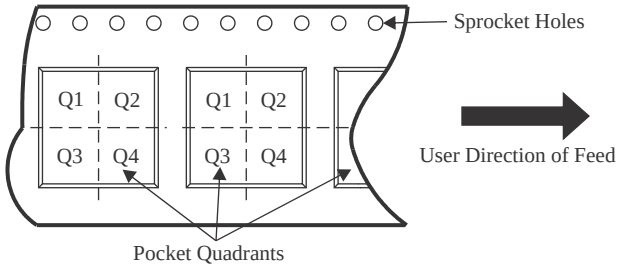


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

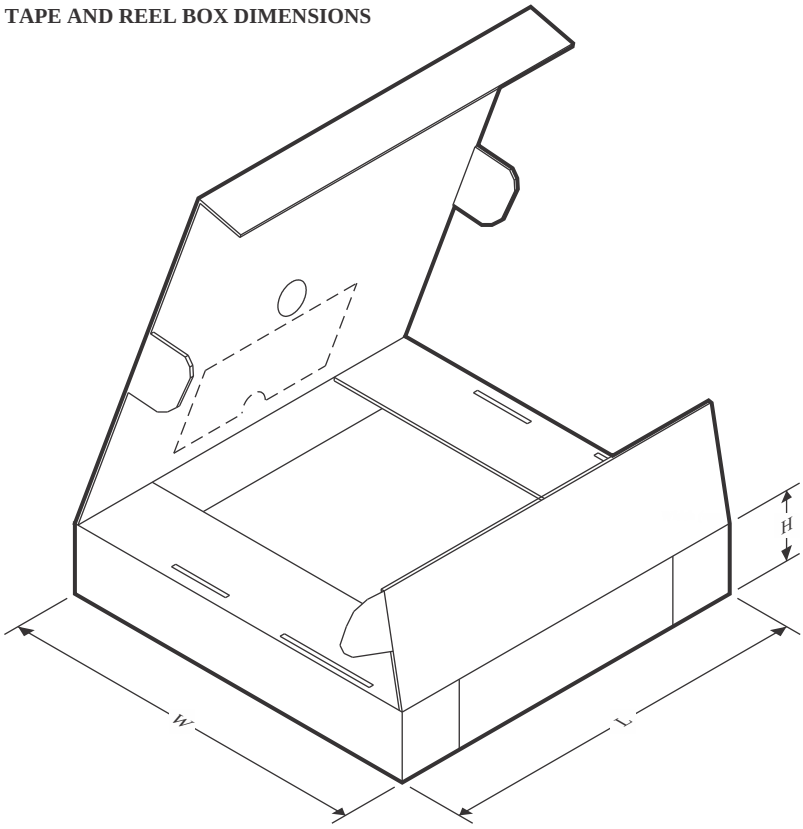
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ELT21DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65ELT21DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

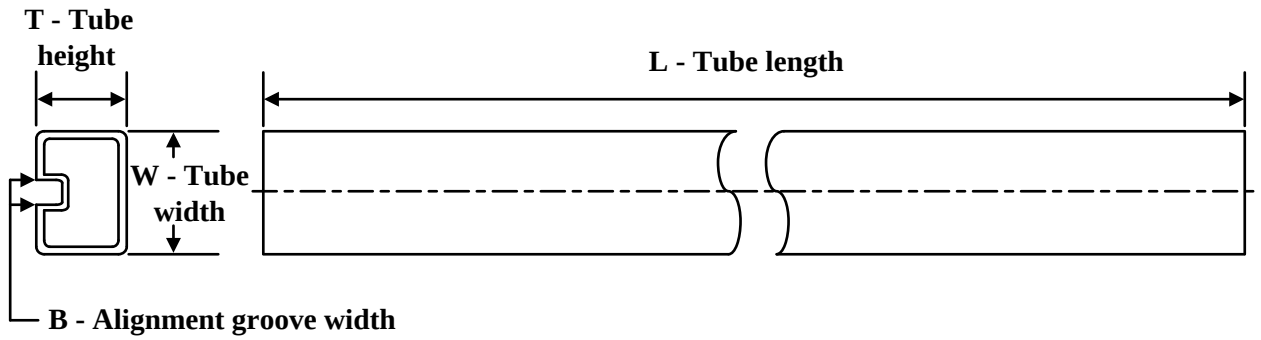
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ELT21DGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
SN65ELT21DR	SOIC	D	8	2500	356.0	356.0	35.0

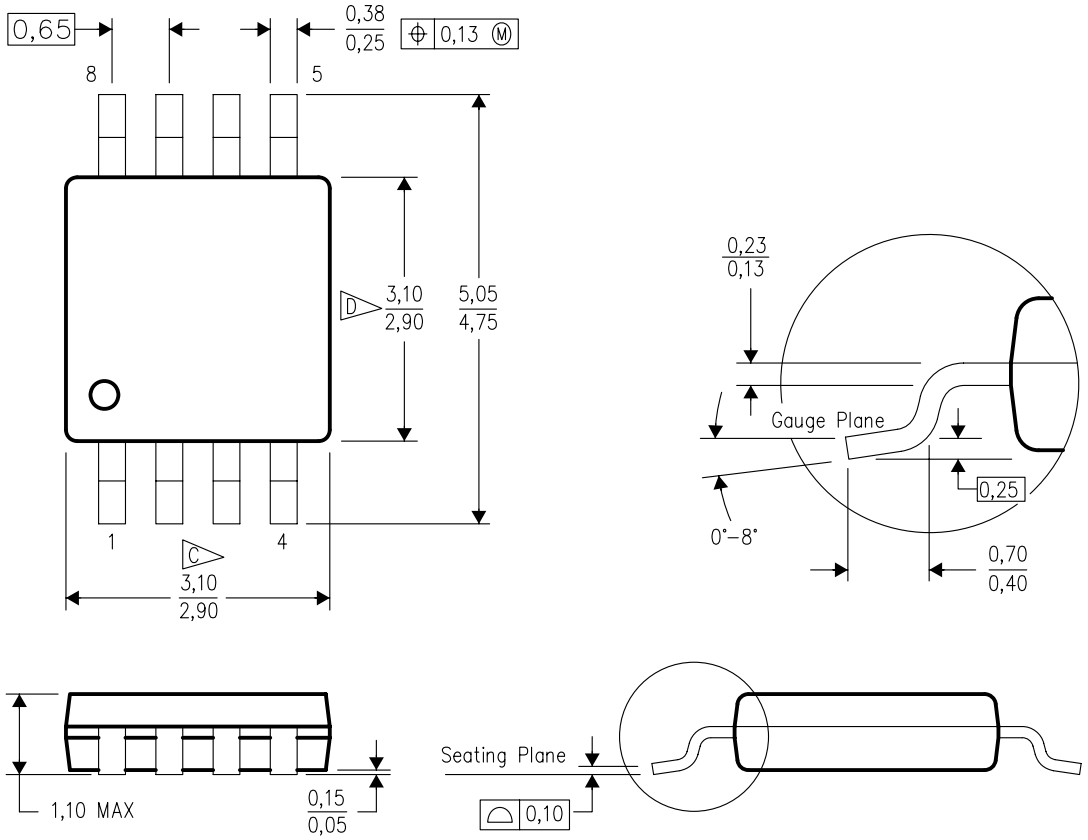
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65ELT21D	D	SOIC	8	75	506.6	8	3940	4.32
SN65ELT21DGK	DGK	VSSOP	8	80	330.2	6.6	3005	1.88

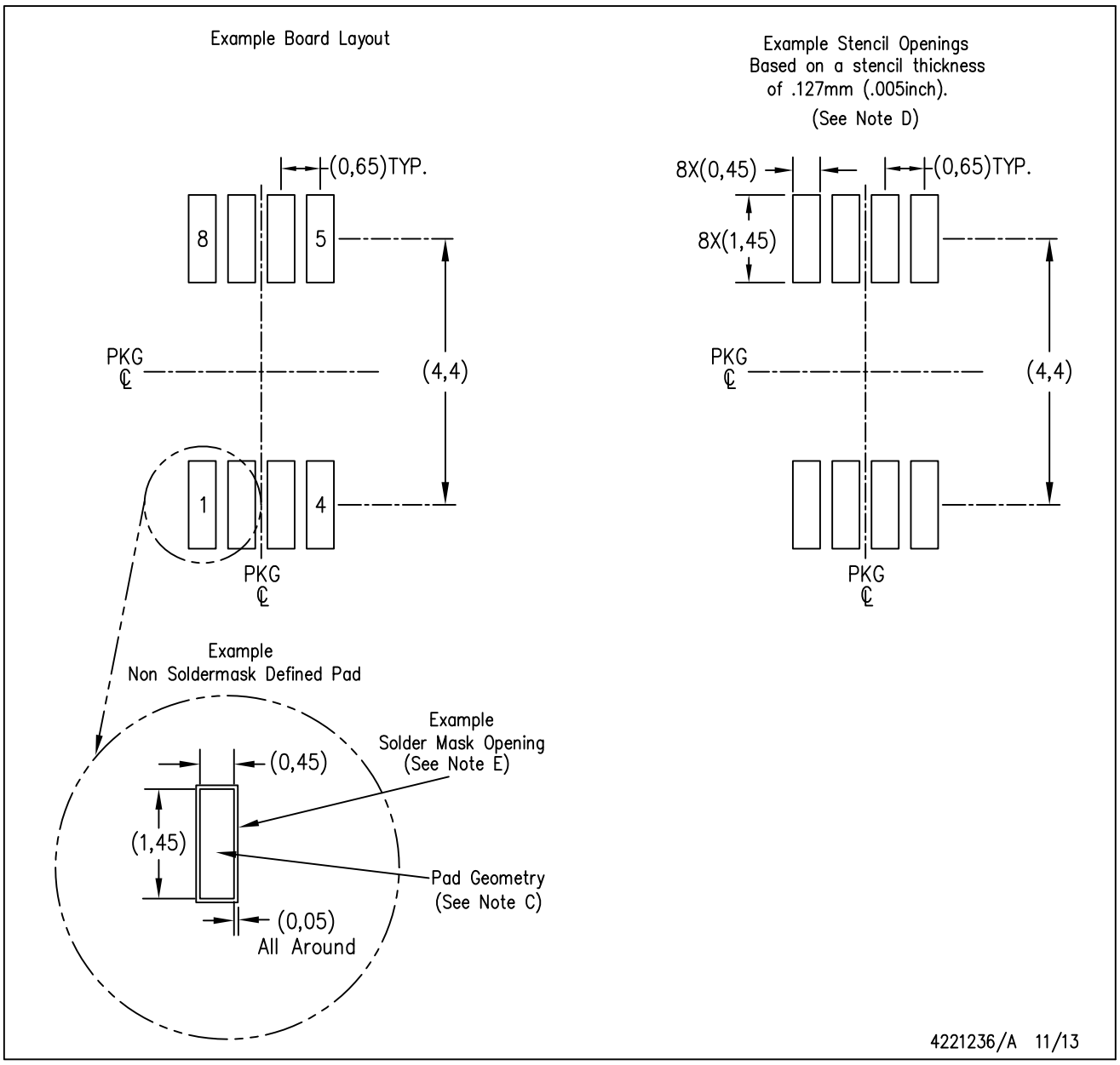
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



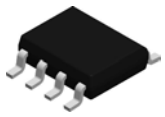
4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

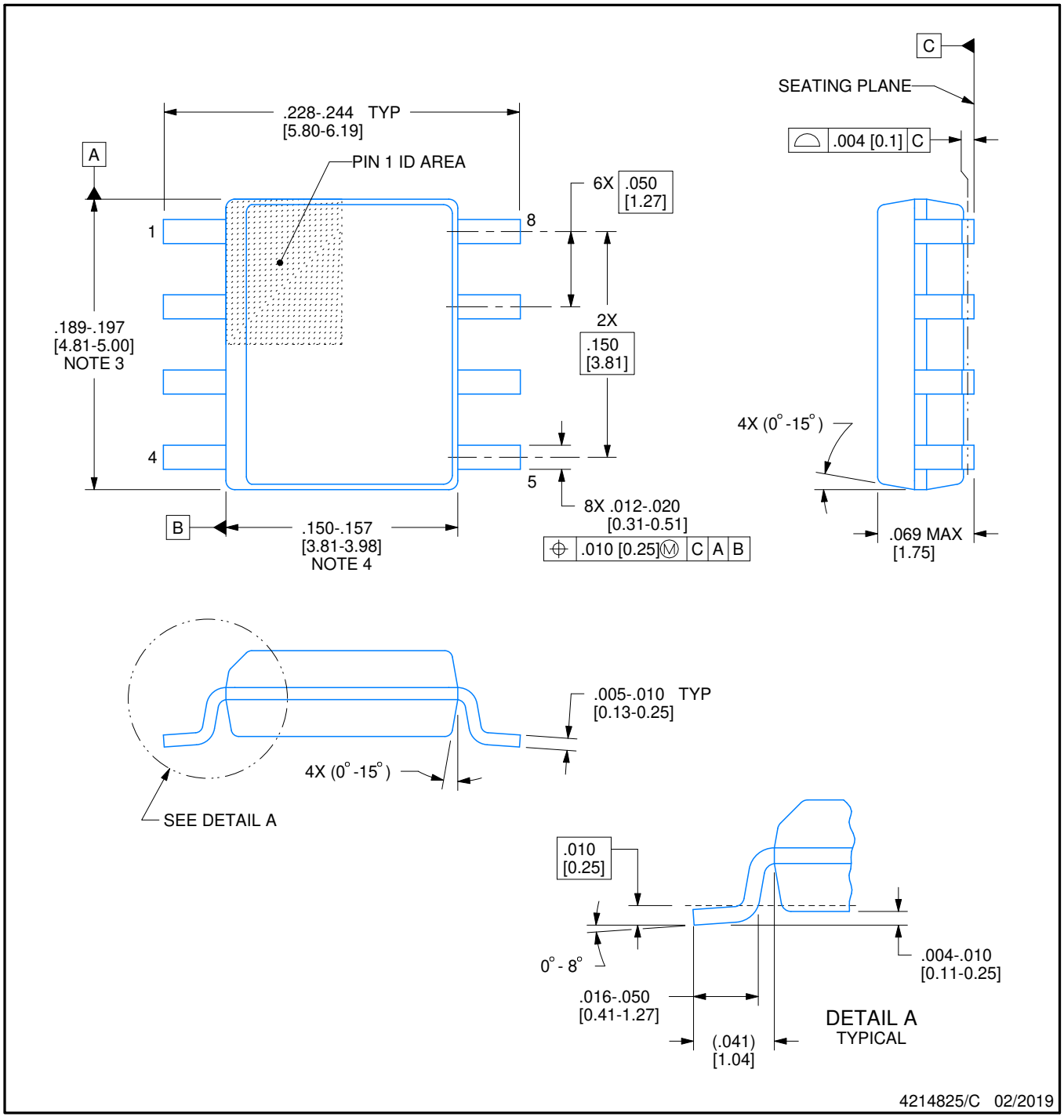


PACKAGE OUTLINE

D0008A

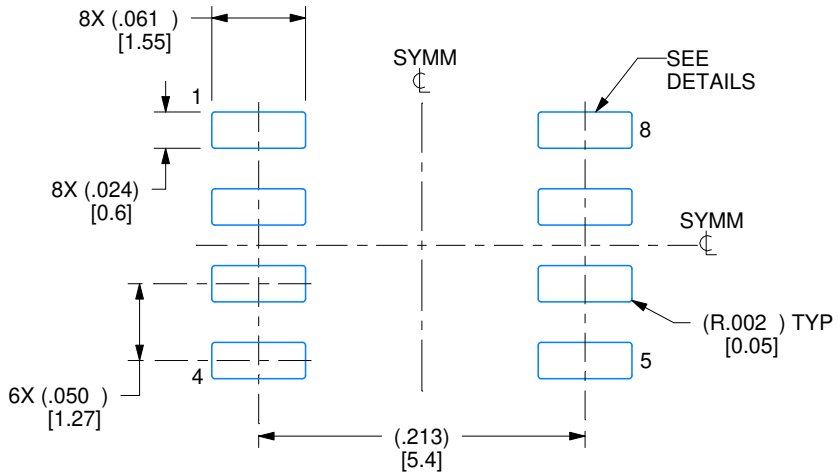
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

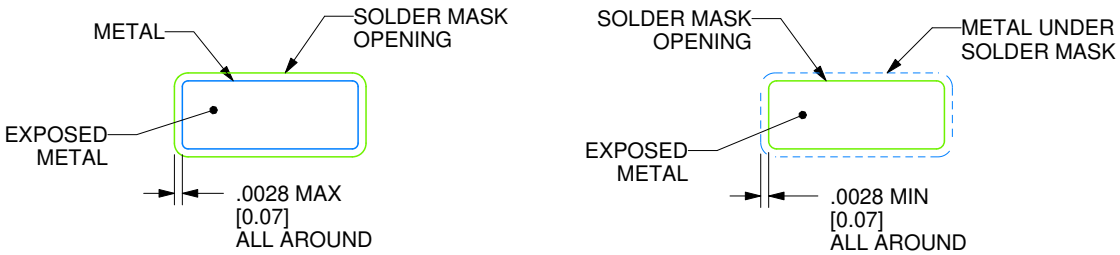


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

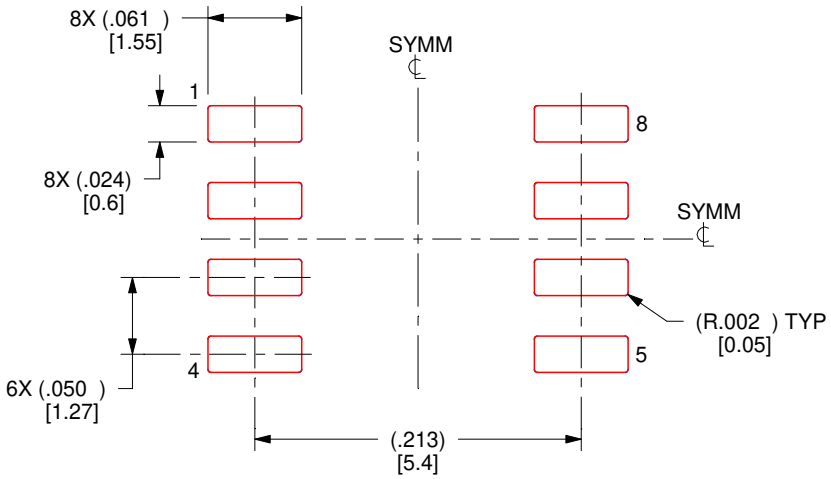
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265