

# Four Channel Squib Driver IC

The Four Channel Squib Driver IC is a complete squib diagnostic and deployment interface for use in automotive air bag modules. Extensive diagnostics and system control features are incorporated to provide fail-safe operation. The device contains a serial peripheral interface (SPI) compatible 8-bit interface to allow microprocessor control.

The device has the capability to be used in a standard four channel squib driver IC or in a cross-coupled state with the high and low side squib drivers located on separate squib driver ICs. Both the high and low side output drivers are protected against temporary shorts to battery or ground. The current limit threshold is set by an external resistor. This device is powered by SMARTMOS technology.

## Features

- Four channel high side and low side 2.0 A FET switches
- Externally adjustable FET current limiting
- Adjustable current limit range: 0.8 to 2.0 A
- Individual channel current limit detection with timing duration measurement, communicated via the SPI
- 8-Bit SPI for diagnostics and FET switch activation
- Diagnostics for high side safing sensor status
- Resistance and voltage diagnostics for squibs
- Squib driver IC capability to be used for cross-coupled driver firing application (allows high and low side FET switches to be located on separate squib driver ICs)

**33797**

**SQUIB DRIVER**



## Applications

- Automotive air bag deployment
- Automatic seat belt retention
- Computer controlled model rocketry igniters
- Remote firing of pyrotechnic and firework displays
- Computer controlled firing of blasting caps for mining and construction
- Military or police weapon systems

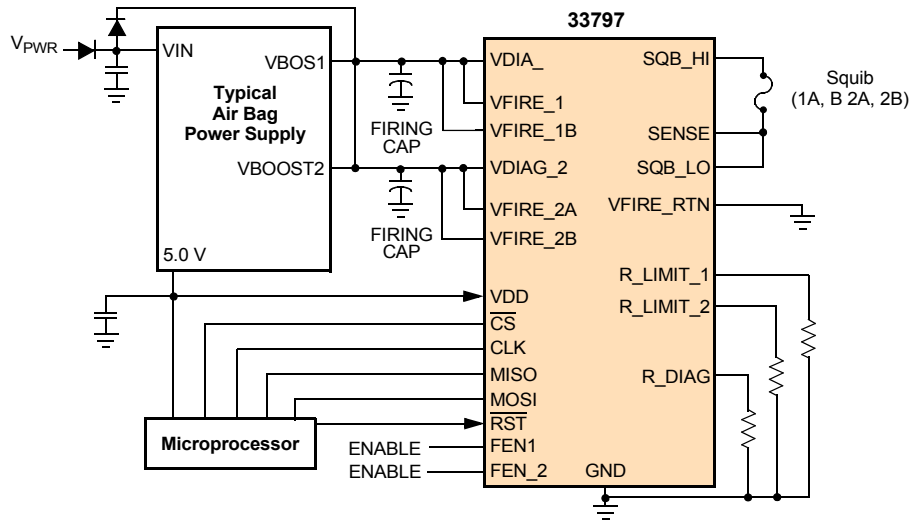


Figure 1. 33797 Simplified Application Diagram

# 1 Orderable Parts

**Table 1. Orderable Part Variations**

Part Number	Temperature (T <sub>A</sub> )	Package
MC33797BPEW	-40 to 85 °C	32 SOICW

Notes

1. To order parts in Tape & Reel, add the R2 suffix to the part number.

### INTERNAL BLOCK DIAGRAM

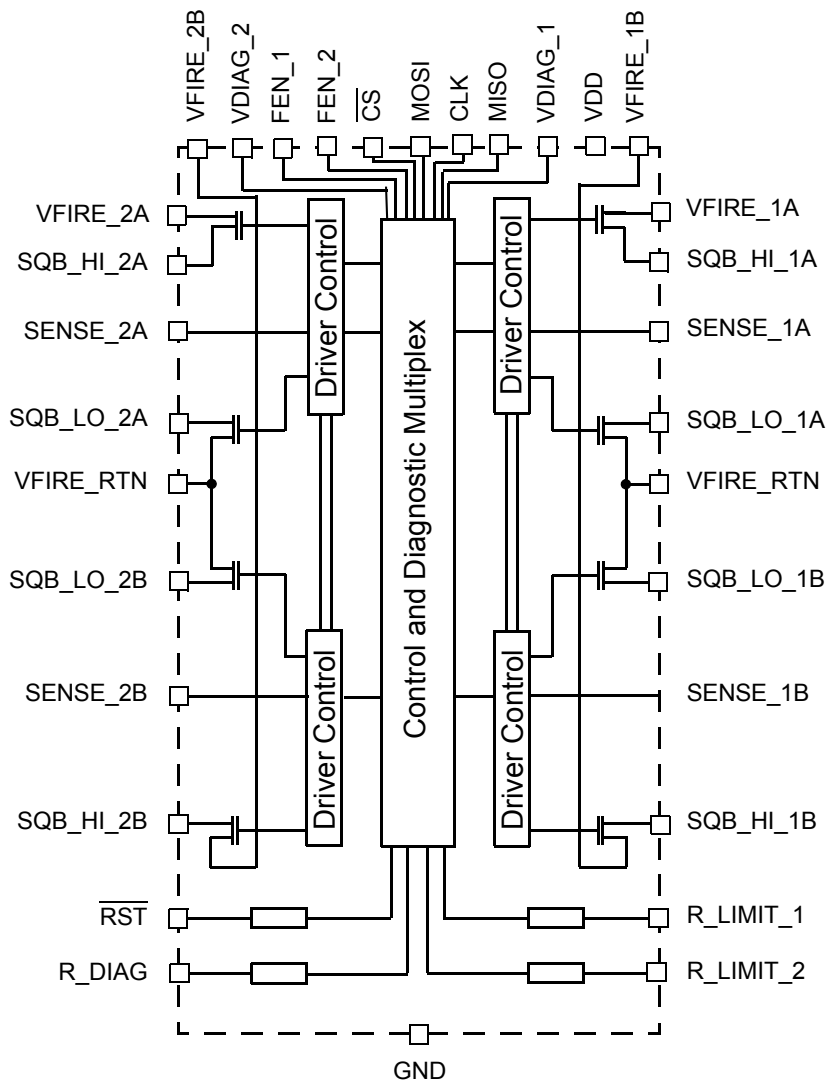


Figure 2. 33797 Simplified Internal Block Diagram

## PIN CONNECTIONS

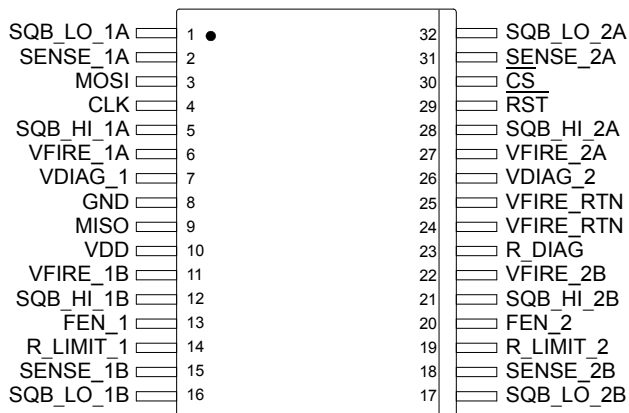


Figure 3. Pin Function Description

Table 2. Pin Function Description

Pin	Pin Name	Pin Function	Formal Name	Pin Description
1	SQB_LO_1A	Output	Squib Lo 1A	Drain of the low side switch that connects to the low pin of Squib_1A
2	SENSE_1A	Input	Squib Sense 1A	Used during standard applications involving a four channel squib driver IC or during cross-coupling applications involving two four channel squib driver ICs (squib driver IC #1 and squib driver IC #2).
3	MOSI	Input	Data Input 1	Serial data input for SPI interface.
4	CLK	Input	Serial Clock	Serial clock input for SPI interface.
5	SQB_HI_1A	Output	Squib Hi 1A	Drain of the high side switch that connects to the low pin of Squib_1A
6	VFIRE_1A	Supply	Squib Firing Supply 1A	Firing supply pin for Squib_1A.
7	VDIAG_1	Input	Squib Diagnostic 1A and 1A	Diagnostic pin for high side safing sensor for squibs 1A and 1B and the VFIRE supply voltage.
8	GND	Ground	Device Ground	Device ground pin for internal logic and diagnostic circuitry.
9	MISO	Output	Data Output 0	Serial data output for SPI interface.
10	VDD	Input	Logic Power	Device power pin for internal logic and diagnostic circuitry.
11	VFIRE_1B	Supply	Squib Firing Supply 1B	Firing supply pin for Squib_1B.
12	SQB_HI_1B	Output	Squib Hi 1B	Drain of the high side switch that connects to the low pin of Squib_1B
13	FEN_1	Input	FET Driver 1A and 1B	Active high input signal to enable operation of the squib_1A and Squib_1BFET drivers.
14	R_LIMIT_1	Output	Limit Resistor - 1A and 1B	External resistor to ground is used to set current limit for Squib_1A and squib_1B FET drivers.
15	SENSE_1B	Input	Squib Sense 1B	Used during standard applications involving a four channel squib driver IC and during cross-coupling applications involving two four channel squib driver ICs (squib driver IC #1 and squib driver IC #2).

**Table 2. Pin Function Description (continued)**

Pin	Pin Name	Pin Function	Formal Name	Pin Description
16	SQB_LO_1B	Output	Squib Lo 1B	Drain of the low side switch that connects to the low pin of Squib_1B
17	SQB_LO_2B	Output	Squib Lo 2B	Drain of the low side switch that connects to the low pin of Squib_2B
18	SENSE_2B	Input	Squib Sense 2B	Used during standard applications involving a four channel squib driver IC and during cross-coupling applications involving two four channel squib driver ICs (squib driver IC #1 and squib driver IC #2).
19	R_LIMIT_2	Output	Limit Resistor - 2A and 2B	External resistor to ground is used to set current limit for Squib_2A and squib_2B FET drivers.
20	FEN_2	Input	FET Driver 2A and 2B	Active high input signal to enable operation of the squib_2A and Squib_2B FET drivers.
21	SQB_HI_2B	Output	Squib Hi 2B	Drain of the high side switch that connects to the low pin of Squib_2B.
22	VFIRE_2B	Supply	Squib Firing Supply 2B	Firing supply pin for squib_2B.
23	R_DIAG	Input	Limit Resistor - Diagnostic	External resistor to ground is used to set the diagnostic current for squib resistance.
24	VFIRE_RTN	Ground	Squib Fire Power Ground	Power Ground for squibs 1A, 1B, 2A, and 2B
25	VFIRE_RTN	Ground	Squib Fire Power Ground	Power Ground for squibs 1A, 1B, 2A, and 2B
26	VDIAG_2	Supply	Squib Diagnostic 2A and 2b	Diagnostic pin for high side safing sensor for squibs 2A and 2B and the VFIRE supply voltage.
27	VFIRE_2A	Supply	Squib Firing Supply 2A	Firing supply pin for squib_2A
28	SQB_HI_2A	Output	Squib Hi 2A	Drain of the high side switch that connects to the low pin of Squib_2A
29	RST	Input	Reset	Reset, Active Low
30	CS	Input	Chip Select	Chip Select for SPI interface, Active Low
31	SENSE_2A	Input	Squib Sense 2A	Used during standard applications involving a four channel squib driver IC or during cross-coupling applications involving two four channel squib driver ICs (squib driver IC #1 and squib driver IC #2).
32	SQB_LO_2A	Output	Squib Lo 2A	Drain of the low side switch that connects to the low pin of Squib_2A

## ELECTRICAL CHARACTERISTICS

### MAXIMUM RATINGS

**Table 3. Maximum Ratings**

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
<b>INPUT ELECTRICAL RATINGS</b>			
Voltage on VDD	$V_{DD}$	7.0	V
Voltage on Input pins $\overline{CS}$ , CLK, D1, D0, FEN_1, FEN_2, $\overline{RESET}$ , R_DIAG, R_LIMIT_X	$V_I$	-0.3 to $V_{DD} + 0.3$	V
Voltage on Squib pins SQB_HI_XX, SQB_LO_XX, SENSE_XX	$V_{VFIRE\_XX}$	-0.3 to $V_{VFIRE} + 0.3$	V
Voltage on pins VDIAG_X, VFIRE_XX	VDIAG_X	-0.3 to 35	V
ESD Voltage <sup>(1)</sup> Human Body Model Machine Model	$V_{ESD1}$ $V_{ESD2}$	$\pm 2000$ $\pm 200$	V
Maximum $V_{VFIRE}$ with Pulsed Output <sup>(1), (2)</sup> $R_{SQUIB} = 2.0 \Omega$ , $t_{ON} = 0.8$ ms, $I_{SQUIB} = 2.24$ A $R_{SQUIB} = 1.2 \Omega$ , $t_{ON} = 0.8$ ms, $I_{SQUIB} = 2.24$ A $R_{SQUIB} = 0.1 \Omega$ , $t_{ON} = 0.60$ ms, $I_{SQUIB} = 2.24$ A	$V_{FPULSE}$	35 25 25	V
<b>THERMAL RATINGS</b>			
Storage Temperature	$T_{STG}$	155	°C
Junction Temperature Ambient Continuous (Prior to Squib Deployment) $t \leq 5.0$ ms (Post-squib Deployment)	$T_A$ $T_{JCONT}$ $T_{JDPYD}$	85 100 300	°C
Peak Package Reflow Temperature During Reflow <sup>(3), (4)</sup>	$T_{PPRT}$	Note 4	°C
Thermal Resistance (Junction-to-Ambient)	$R_{\theta JA}$	74	°C/W

Notes

- ESD1 testing is performed in accordance with the Human Body Model ( $C_{ZAP} = 100$  pF,  $R_{ZAP} = 1500 \Omega$ ), ESD2 testing is performed in accordance with the Machine Model ( $C_{ZAP} = 200$  pF,  $R_{ZAP} = 0 \Omega$ ).
- With a nominal squib load, the FET squib driver will not enter thermal shutdown until the driver has been active for a minimum of 2.1 ms. The individual squib driver thermal shutdown will not affect other squib driver firing "ON" times. With a shorted squib load, the FET squib driver will not enter thermal shutdown until the driver has been active for a minimum of 2.1 ms. When the thermal shutdown limit is exceeded, the FET driver will turn OFF and the thermal status bit will be set to 1. The FET squib driver can be activated through the arm/fire command when the  $TEMP_{RENABLE}$  (MIN) is reached (thermal shutdown status "0"). Nominal squib load is  $2.15 \Omega \pm 0.15 \Omega$ . Shorted squib load is  $0.1 \Omega$ .
- Three squib driver with  $R_{SQUIB} = 0.1 \Omega$  conditions. Remaining squib driver conditions:  $R_{SQUIB} = 1.2 \Omega$ ,  $t_{ON} = 4.0$  ms,  $I_{SQUIB} = 2.0$  A,  $V_{VDIAG\_X} = V_{VFIRE\_XX} = 35$  V.
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescle's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to [www.freescale.com](http://www.freescale.com), search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxx enter 33xxx), and review parametrics.

**Table 3. Maximum Ratings**

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
<b>OPERATING RATING</b> <sup>(6)</sup>			
FET Driver Firing Current	$I_{\text{SQUIB}}$		A
$R_{\text{SQUIB}} = 2.0 \Omega$ , $V_{\text{SQUIBHI}} = 16 \text{ V}$ , $t_{\text{ON}} = 2.6 \text{ ms}$		3.0	
$R_{\text{SQUIB}} = 1.2 \Omega$ , $V_{\text{SQUIBHI}} = 16 \text{ V}$ , $t_{\text{ON}} = 2.6 \text{ ms}$		3.0	
$R_{\text{SQUIB}} = 0.1 \Omega$ , $V_{\text{SQUIBHI}} = 16 \text{ V}$ , $t_{\text{ON}} = 2.6 \text{ ms}$		3.0	

**Notes**

- 6 Operating ratings indicate conditions for which the device is intended to be functional. For guaranteed specifications and test conditions, refer to the static and dynamic electrical characteristics tables on the following pages.

### STATIC ELECTRICAL CHARACTERISTICS

**Table 4. Static Electrical Characteristics**

Characteristics noted under conditions  $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$ ;  $7.0\text{ V} \leq V_{VFIRE\_XX} \leq 35\text{ V}$ ;  $V_{VDIAG\_X} = V_{VFIRE\_XX}$ ;  
 $FEN\ 1 = FEN\ 2 = V_{DD}$ ;  $R_{R\_LIMIT\_X} = 10\text{ k}\Omega \pm 1\%$ ,  $R_{R\_DIAG} = 10\text{ k}\Omega \pm 1\%$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq +85\text{ }^\circ\text{C}$ ,  $GND = 0$ , unless otherwise noted.  
 Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>INPUT VOLTAGE (VDD)</b>					
Input Voltage	$V_{DD}$	4.75	5.0	5.25	V
<b>FET DRIVERS</b>					
Leakage Current at Minimum High Side Driver Breakdown Voltage	$I_{DHSD}$	–	39	100	$\mu\text{A}$
Leakage Current at Minimum Low Side Driver Breakdown Voltage	$I_{DLSD}$	–	65	100	$\mu\text{A}$
High Side Driver Current Limit Range Set via Rlimit Resistor with Low Battery Condition $t_{ON} \leq 4.0\text{ ms}$ , $R_{R\_LIMIT\_X} = 10\text{ k}\Omega$ , $5.0\text{ V} \leq V_{VFIRE} \leq 7.0\text{ V}$ , $R_{SQUB} = 2.0\ \Omega$	$I_{HS(LBAT)}$	1.09	1.4	2.9	A
High Side Driver Low Current Limit Range Set via Rlimit Resistor $t_{ON} \leq 2.6\text{ ms}$ , $R_{R\_LIMIT\_X} = R_L = 4.32\text{ k}\Omega$ , $7.0\text{ V} \leq V_{VFIRE} \leq 35\text{ V}$	$I_{HS(LOSET)}$	0.81	0.93	1.03	A
High Side Driver Nominal Current Limit Range Set via Rlimit Resistor $t_{ON} \leq 2.6\text{ ms}$ , $R_{R\_LIMIT\_X} = R_L = 10\text{ k}\Omega$ , $7.0\text{ V} \leq V_{VFIRE} \leq 35\text{ V}$	$I_{HS(NOM)}$	1.21	1.4	1.54	A
High Side Driver High Current Limit Range Set via Rlimit Resistor $t_{ON} \leq 0.8\text{ ms}$ , $R_{R\_LIMIT\_X} = R_L = 45.3\text{ k}\Omega$ , $7.0\text{ V} \leq V_{VFIRE} \leq 35\text{ V}$	$I_{HS(HISET)}$	1.76	2.0	2.24	A
Low Side Drivers Current Limit $7.0\text{ V} = SQLO < 16\text{ V}$ $SQLO = 16\text{ V}$	$I_{LS}$	2.1 2.24	2.47 2.65	3.0 3.14	A
High Side Driver Current Limit Detect Threshold <sup>(7)</sup> $7.0\text{ V} \leq V_{VFIRE} \leq 35\text{ V}$	$I_{MEAS}$	$I_{HS} \times 0.85$	–	$I_{HS} \times 1.0$	A
Driver ON Resistance (per FET) $V_{VFIRE} = 5.0\text{ V}$ , $I_{LOAD} = 0.5\text{ A}$	$R_{DS(ON)}$	–	–	1.0	$\Omega$
VDD Operating Current Standby (Diagnostics off, SPI "OFF") No Fire—Worst Case Diagnostics (\$83/\$2F Command Active) Firing (with All FET Drivers "ON")	$I_{DD}$	–	2.0 15 4.3	5.0 18.5 6.0	mA
VFIRE Quiescent Current <sup>(8)</sup> With Diagnostics Off	$I_{RRE}$	22	34	55	$\mu\text{A}$
VDIAG Current During Squib Diagnostics With Squib Resistance Diagnostics Active	$I_{RRE}$	32	37	43	mA
VFIRE Operating Current During Firing Excluding Firing Current, $I_{HS} = 2.0\text{ A}$	$I_{RRE}$	–	1.8	11	mA
VDIAG Operating Current During Firing Per $V_{DIAG}$ pin, excluding Firing Current, $I_{HS} = 2.0\text{ A}$	$I_{RRE}$	–	140	200	$\mu\text{A}$

Notes

- 7 Guaranteed by design
- 8 VFIRE quiescent current includes any leakage current through squib.



**Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$ ;  $7.0\text{ V} \leq V_{VFIRE\_XX} \leq 35\text{ V}$ ;  $V_{VDIAG\_X} = V_{VFIRE\_XX}$ ;  
 $FEN\ 1 = FEN\ 2 = V_{DD}$ ;  $R_{R\_LIMIT\_X} = 10\text{ k}\Omega \pm 1\%$ ,  $R_{R\_DIAG} = 10\text{ k}\Omega \pm 1\%$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq +85\text{ }^\circ\text{C}$ ,  $GND = 0$ , unless otherwise noted.  
 Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VFIRE1A / VFIRE2A Current During High Side Safing Sensor Diagnostics (Command \$CO) Per VFIREXA pin, with High Side Safing Sensor Diagnostic active	$I_{RRE}$	260	350	415	$\mu\text{A}$
VFIRE1B / VFIRE2B Current During High Side Safing Sensor Diagnostics (Command \$CO) Per VFIREXB pin, with High Side Safing Sensor Diagnostic active	$I_{RRE}$	22	32	55	$\mu\text{A}$
VFIRE1B / VFIRE2B Current During VFIRE Diagnostics (Command \$C5) Either VFIRE1B or VFIRE2B Diagnostic active	$I_{RRE}$	0.3	2.0	3.8	mA
VFIRE Quiescent Current - Total All VFIRE pins measured together, with Diagnostics Off	$I_{QVFIRETOTAL}$	90	135	180	$\mu\text{A}$
Maximum Allowable External Capacitance to Ground <sup>(9)</sup> Per Squib pin SQB_LO and SQB_HI	$C_{S_{MAX}}$	–	–	0.12	$\mu\text{F}$
Maximum Allowable External Resistance to Ground During Firing <sup>(9)</sup> VFIRE_RTN pin to Ground	$R_{S_{MAX}}$	–	–	0.15	$\Omega$
Individual FET Driver Thermal Shutdown <sup>(9), (10)</sup>	$T_{SD}$	160	–	190	C
FET Driver Thermal Shutdown Re-enable Threshold After Drive Cool down <sup>(9), (10)</sup>	$T_{REN}$	90	–	110	C

**FET DRIVERS HIGH AND LOW SIDE DRIVER TRANSISTOR STATUS/DIAGNOSTICS (\$82, \$83 COMMANDS)**

Voltage Transistor Test Threshold for High Side Driver Transistor	$V_{TRANTST1}$	5.5	6.0	6.5	V
High Side Driver Current Limit During High Side Driver Transistor Diagnostics $15\text{ V} \leq V_{VFIRE\_XX} \leq 35\text{ V}$	$I_{TRANTST1}$	2.0	10	50	mA
Voltage Transistor Test Threshold for Low Side Driver Transistor	$V_{TRANTST2}$	1.0	1.4	2.0	V
Low Side Driver Current Limit During Low Side Driver Transistor Diagnostics $15\text{ V} \leq V_{VFIRE\_XX} \leq 35\text{ V}$	$I_{TRANTST2}$	2.0	10	50	mA

**FEN INPUT PIN (FEN\_1 AND FEN\_2)**

Internal Current Pull-down	$I_{FEN}$	-25	-40	-50	$\mu\text{A}$
Logic Low Level	$V_{FEN(LO)}$	0.0	2.5	$0.35 \times V_{DD}$	V
Fire Enable Pin Logic High Level	$V_{FEN(HI)}$	$0.65 \times V_{DD}$	2.5	$1.0 \times V_{DD}$	V

**Notes**

- 9 Guaranteed by design.
- 10 With a nominal squib load, the FET squib driver will not enter thermal shutdown until the driver has been active for a minimum of 2.1 ms. The individual squib driver thermal shutdown will not affect other squib driver firing ON times. With a shorted squib load, the FET squib driver will not enter thermal shutdown until the driver has been active for a minimum of 2.1 ms. When the thermal shutdown limit is exceeded, the FET driver will turn OFF and the thermal status bit will be set to 1. The FET squib driver can be activated through the arm/fire command when the  $TEMP_{REENABLE}$  (MIN) is reached (thermal shutdown status "0"). Nominal squib load:  $2.15\ \Omega \pm 0.15\ \Omega$ . Shorted squib load:  $0.1\ \Omega$ .

**Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$ ;  $7.0\text{ V} \leq V_{VFIRE\_XX} \leq 35\text{ V}$ ;  $V_{VDIAG\_X} = V_{VFIRE\_XX}$ ;  
 $FEN\ 1 = FEN\ 2 = V_{DD}$ ;  $R_{R\_LIMIT\_X} = 10\text{ k}\Omega \pm 1\%$ ,  $R_{R\_DIAG} = 10\text{ k}\Omega \pm 1\%$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq +85\text{ }^\circ\text{C}$ ,  $GND = 0$ , unless otherwise noted.  
 Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>RST INPUT PIN (ACTIVE LOW) <sup>(11)</sup></b>					
System Reset Threshold	$V_{DDRST}$	–	–	4.1	V
Internal Current Pull-down	$I_{RST}$	-6.0	-10	-15	$\mu\text{A}$
$\overline{\text{RST}}$ Logic Low Level	$V_{RST(LO)}$	0.0	2.5	$0.35 \times V_{DD}$	V
$\overline{\text{RST}}$ Logic High Level	$V_{RST(HI)}$	$0.65 \times V_{DD}$	2.5	$1.0 \times V_{DD}$	V

**SQUIB DIAGNOSTICS (\$D0–\$D3 COMMANDS) <sup>(12)</sup>**

Diagnostic Current Through Squib <sup>(13)</sup>	$I_{DIAG}$	30	34	40.5	mA
Resistance Threshold 1 <sup>(13)</sup>	$R_{TH1}$	1.2	1.4	1.6	$\Omega$
Resistance Threshold 2 <sup>(13)</sup>	$R_{TH2}$	1.6	1.8	2.1	$\Omega$
Resistance Threshold 3 <sup>(13)</sup>	$R_{TH3}$	2.1	2.4	2.6	$\Omega$
Resistance Threshold 4 <sup>(13)</sup>	$R_{TH4}$	2.6	2.9	3.2	$\Omega$
Resistance Threshold 5 <sup>(13)</sup>	$R_{TH5}$	3.3	3.7	4.4	$\Omega$
Resistance Threshold 6 <sup>(13)</sup>	$R_{TH6}$	4.6	5.4	6.0	$\Omega$
Resistance Threshold 7 <sup>(13)</sup>	$R_{TH7}$	5.7	6.5	7.1	$\Omega$
Resistance Threshold 8 <sup>(13)</sup>	$R_{TH8}$	6.7	7.8	8.5	$\Omega$

**SQUIB SHORT-TO-BATTERY/GROUND DIAGNOSTICS AND SQUIB HARNESS SHORT-TO-BATTERY/GROUND DIAGNOSTICS WITH AN OPEN SQUIB (\$C1, \$C3 COMMANDS)**

Voltage Threshold for SQB_LO and SQB_HI Shorted to $V_{PWR}$ $7.0\text{ V} \leq V_{VDIAG\_X} \leq 35\text{ V}$	$V_{THSB}$	5.7	6.0	6.4	V
Voltage Threshold for SQB_LO and SQB_HI Shorted to Ground $7.0\text{ V} \leq V_{VDIAG\_X} \leq 35\text{ V}$	$V_{THSG}$	1.3	1.4	1.6	V
Current Sink Shorts Measurements $I_{SQB\_LO\_XX}$ <sup>(14)</sup> $1.0\text{ V} \leq SENSE\_XX \leq 16\text{ V}$ , Typical = $800\ \mu\text{A}$	$I_{SINKSHRTS}$	-500	-800	-900	$\mu\text{A}$
Current Source Shorts Measurements $I_{SQB\_HI\_XX}$ <sup>(14)</sup> $1.0\text{ V} \leq SENSE\_XX \leq 16\text{ V}$ , $7.0\text{ V} \leq V_{VDIAG\_X} \leq 35\text{ V}$	$I_{SOURSHRTS}$	1.7	3.5	3.7	mA
Voltage Threshold for SQB_LO or SQB_HI Shorted to $V_{PWR}$ with an Open Squib using \$C3 Command $R_{SQUIB} = \text{Open}$	$V_{THSB\_SO}$	5.75	–	6.79	V

Notes

- Reset Bar range of operation: The minimum system reset bar threshold/active will be set to "0" for a value of  $V_{DD} \leq 4.1\text{ V}$ .
- By changing the  $R_{DIAG}$  resistor value, the resistance thresholds can be varied in a linear relationship. The  $R_{DIAG}$  resistance can be changed by  $\pm 10\%$  to shift the thresholds by  $\pm 10\%$ . Design goal for resistance threshold change is  $\pm 15\%$ .  $R_{DIAG}$  threshold limit may have to be changed to accommodate  $\pm 15\%$  change. Example: Shifting the  $R_{DIAG}$  resistance value  $\pm 10\%$ , the resistance threshold will change by  $\pm 10\%$ . Refer to [Table 5](#), page 13.
- $R_{R\_DIAG} = 10\text{ k}\Omega \pm 1.0\%$
- XX = 1A, 1B, 2A, or 2B.

**Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$ ;  $7.0\text{ V} \leq V_{VFIRE\_XX} \leq 35\text{ V}$ ;  $V_{VDIAG\_X} = V_{VFIRE\_XX}$ ;  
 $FEN\ 1 = FEN\ 2 = V_{DD}$ ;  $R_{R\_LIMIT\_X} = 10\text{ k}\Omega \pm 1\%$ ,  $R_{R\_DIAG} = 10\text{ k}\Omega \pm 1\%$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq +85\text{ }^\circ\text{C}$ ,  $GND = 0$ , unless otherwise noted.  
 Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Voltage Threshold for SQB_LO or SQB_HI Shorted to Ground with an Open Squib using \$C3 Command $R_{SQIB} = \text{Open}$	$V_{THSG\_SO}$	1.3	1.8	2.0	V

**DIAGNOSTICS FOR SQUIB CONTINUITY BETWEEN SENSE\_XX AND SQB\_LO\_XX (\$C2 COMMAND)**

Current Threshold for SQUIB_LO_1A, 1B, 2A, and 2B Continuity Check for Standard and Cross-coupled Conditions (\$C2) SQUIB_LO_XXCONT <sup>(15)</sup> $7.0\text{ V} \leq V_{VDIAG\_X} \leq 35\text{ V}$	$I_{THSQB\ CON}$	150	–	350	$\mu\text{A}$
--	------------------	-----	---	-----	---------------

**DIAGNOSTICS FOR SQUIB SHORT BETWEEN FIRING LOOPS (\$E0–\$E3, \$E8 COMMANDS)**

Voltage Threshold for Standard Squib Connection $7.0\text{ V} \leq V_{VDIAG\_X} \leq 35\text{ V}$	$V_{THSQBNOM}$	1.0	1.4	2.0	V
Voltage Threshold for SQUIB_X Shorted to SQUIB_Y (1 or More Shorted Conditions) Short Between Squib Lines (Loops) (SQUIB_XX_SSQB_YY) <sup>(16)</sup>	$V_{THSSQB}$	1.0	1.4	2.0	V

**VDIAG SUPPLY DIAGNOSTICS (\$C0 COMMAND)**

VDIAG Supply Voltage High Threshold	$V_{DHI}$	15	17	19.0	V
VDIAG Supply Voltage Low Threshold	$V_{DLO}$	5.7	6.5	7.2	V

**VFIRE SUPPLY DIAGNOSTICS VFIRE\_1B AND VFIRE\_2B (\$C5COMMAND)**

VFIRE Supply Voltage High Threshold	$V_{FDHI}$	15	17	19.0	V
VFIRE Supply Voltage Low Threshold	$V_{FLO}$	5.7	6.5	7.2	V

**VDIAG SUPPLY DIAGNOSTICS VDIAG\_1 AND VDIAG\_2 (ADDITIONAL VOLTAGE THRESHOLDS) (\$C6 COMMAND)**

VDIAG Supply Voltage Threshold 4	$V_{VDIAG\_X\ V4}$	29.8	32.8	38.5	V
VDIAG Supply Voltage Threshold 3	$V_{VDIAG\_X\ V3}$	25.5	27.7	30.5	V
VDIAG Supply Voltage Threshold 2	$V_{VDIAG\_X\ V2}$	20.5	22.6	26.5	V
VDIAG Supply Voltage Threshold 1	$V_{VDIAG\_X\ V1}$	16	18.4	21.0	V

**VFIRE\_RTN DIAGNOSTICS (\$C9 COMMAND)**

R_RTN1 Short-to-Ground Threshold (Open Ground Connection)	$R_{RTN1}$	0.15	–	0.6	$\Omega$
R_RTN2 Short-to-Ground Threshold (Open Ground Connection)	$R_{RTN2}$	0.15	–	0.6	$\Omega$

**HIGH SIDE SAFING SENSOR DIAGNOSTICS (\$C0 COMMAND)**

R_HS Valid Resistor Range $15\text{ V} \leq V_{VDIAG\_X} \leq 35\text{ V}$	$R_{HS}$	4.1	5.1	6.1	$\text{k}\Omega$
R_HS Open Threshold $15\text{ V} \leq V_{VDIAG\_X} \leq 35\text{ V}$	$R_{HSO}$	6.1	7.2	9.0	$\text{k}\Omega$

**Notes**

15 XX = 1A, 1B, 2A, or 2B

16 XX and YY = 1A, 1B, 2A, or 2B

**Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$ ;  $7.0\text{ V} \leq V_{VFIRE\_XX} \leq 35\text{ V}$ ;  $V_{VDIAG\_X} = V_{VFIRE\_XX}$ ;  
 $FEN\ 1 = FEN\ 2 = V_{DD}$ ;  $R_{R\_LIMIT\_X} = 10\text{ k}\Omega \pm 1\%$ ,  $R_{R\_DIAG} = 10\text{ k}\Omega \pm 1\%$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq +85\text{ }^\circ\text{C}$ ,  $GND = 0$ , unless otherwise noted.  
 Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
R_HS Short Threshold	$R_{HSS}$	2.8	–	4.1	$\text{k}\Omega$
VFIRE_XA & VFIRE_XB Current during High Side Safing Test at Open Threshold VFIRE_1A & VFIRE_1B or VFIRE_2A & VFIRE_2B	$I_{1HSO}$	270	360	410	$\mu\text{A}$
VFIRE_XA & VFIRE_XB Current during High Side Safing Test at Short Threshold VFIRE_1A & VFIRE_1B or VFIRE_2A & VFIRE_2B	$I_{1HSS}$	287	385	439	$\mu\text{A}$

**HIGH SIDE SAFING SENSOR DIAGNOSTICS WITH 1 SAFING SENSOR IN FIRING PATH CONNECTED TO VFIRE\_1A AND VFIRE\_2A PINS (GUARANTEED BY DESIGN) (\$C0 COMMAND)**

Total VFIRE_XX Current during High Side Safing Test at Open Threshold VFIRE_1A, VFIRE_1B, VFIRE_2A & VFIRE_2B pins	$I_{2HSO}$	574	705	848	$\mu\text{A}$
Total VFIRE_XX Current during High Side Safing Test at Short Threshold VFIRE_1A, VFIRE_1B, VFIRE_2A & VFIRE_2B pins	$I_{2HSS}$	605	748	892	$\mu\text{A}$
R_HS Valid Resistor Range $15\text{ V} \leq V_{VDIAG\_X} \leq 35\text{ V}$	$R_{2HS}$	2.10	–	2.93	$\text{k}\Omega$
R_HS Open Threshold $15\text{ V} \leq V_{VDIAG\_X} \leq 35\text{ V}$	$R_{2HSO}$	2.93	3.35	4.43	$\text{k}\Omega$
R_HS Short Threshold $15\text{ V} \leq V_{VDIAG\_X} \leq 35\text{ V}$	$R_{2HSS}$	1.14	1.61	2.10	$\text{k}\Omega$

**R\_LIMIT RESISTOR DIAGNOSTICS (\$C8 COMMAND)**

R_LIMIT Valid Resistor Range	$R_{RL}$	4.32	–	45.3	$\text{k}\Omega$
R_LIMIT Open Threshold (“Out of Range Threshold”)	$R_{RLO}$	60	76	105	$\text{k}\Omega$
R_LIMIT Short-to-Ground Threshold (“Out of Range Threshold”)	$R_{RLS}$	2.82	3.5	4.31	$\text{k}\Omega$
Maximum External Capacitance to Ground	$C_{RL}$	–	–	20	$\text{pF}$

**R\_DIAG RESISTOR DIAGNOSTICS (\$C8 COMMAND) <sup>(17)</sup>**

R_DIAG Valid Resistor Range	$R_{RD}$	8.0	–	13	$\text{k}\Omega$
R_DIAG Open Threshold (“Out of Range Threshold”)	$R_{RDO}$	13	23	60	$\text{k}\Omega$
R_DIAG Short-to-Ground Threshold (“Out of Range Threshold”)	$R_{RDS}$	3.0	5.4	8.0	$\text{k}\Omega$
Maximum External Capacitance to Ground	$C_{RD}$	–	–	20	$\text{pF}$

Notes

- By changing the R\_DIAG resistor value, the resistance thresholds can be varied by a linear relationship. The R\_DIAG resistance could be changed by  $\pm 10\%$  to shift the thresholds by  $\pm 10\%$ . Design goal for resistance threshold change is  $\pm 15\%$ . R\_DIAG threshold limit may have to be changed to accommodate  $\pm 15\%$  change. Example: Shifting the R\_DIAG resistance value  $\pm 10\%$ , the resistance threshold will change by  $\pm 10\%$ . Refer to [Table 5](#).

**Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$ ;  $7.0\text{ V} \leq V_{VFIRE\_XX} \leq 35\text{ V}$ ;  $V_{VDIAG\_X} = V_{VFIRE\_XX}$ ;  
 FEN 1 = FEN 2 =  $V_{DD}$ ;  $R_{R\_LIMIT\_X} = 10\text{ k}\Omega \pm 1\%$ ,  $R_{R\_DIAG} = 10\text{ k}\Omega \pm 1\%$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq +85\text{ }^\circ\text{C}$ , GND = 0, unless otherwise noted.  
 Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>SERIAL INTERFACE</b>					
Output Logic Low Level (D0) $I_{SINK} = -800\text{ }\mu\text{A}$	$V_{OLOW}$	0.0	–	0.2	$\times V_{DD}$
Output Logic High Level (D0) $I_{SOURCE} = 800\text{ }\mu\text{A}$	$V_{OHIGH}$	0.7	–	1.0	$\times V_{DD}$
Input Logic Threshold (D1, $\overline{CS}$ , CLK)	$V_{LTHR}$	0.35	–	0.65	$\times V_{DD}$
D1 Pull-down Current	$I_{D1}$	-6.0	-10	-15	$\mu\text{A}$
CLK Pull-down Current	$I_{CLK}$	-6.0	-10	-15	$\mu\text{A}$
$\overline{CS}$ Pull-up Current	$I_{CSBAR}$	10	20	30	$\mu\text{A}$
HI-Z Leakage (D0)	$I_{HI-Z}$	–	–	$\pm 10$	$\mu\text{A}$

**Table 5. Resistance Range vs.  $R_{DIAG}$** 

$R_{DIAG}$	$I_{DIAG}$ (NOM)	$R_{TH1}$ Min/Max	$R_{TH2}$ Min/Max	$R_{TH3}$ Min/Max	$R_{TH4}$ Min/Max	$R_{TH5}$ Min/Max	$R_{TH6}$ Min/Max	$R_{TH7}$ Min/Max	$R_{TH8}$ Min/Max
8.0 k $\Omega$ (-20%)	41	0.9 / 1.3	1.2 / 1.7	1.6 / 2.1	2.0 / 2.6	2.6 / 3.6	3.6 / 4.8	4.5 / 5.7	5.3 / 6.8
9.0 k $\Omega$ (-10%)	38	1.0 / 1.4	1.4 / 1.9	1.9 / 2.3	2.3 / 2.9	2.0 / 4.0	4.1 / 5.4	5.1 / 6.4	6.0 / 7.7
10.0 k $\Omega$	35	1.2 / 1.6	1.6 / 2.1	2.1 / 2.6	2.6 / 3.2	3.3 / 4.4	4.6 / 6.0	5.7 / 7.1	6.7 / 8.5
11.0 k $\Omega$ (+10%)	32	1.3 / 1.8	1.8 / 2.3	2.3 / 2.9	2.9 / 3.6	3.6 / 4.9	5.0 / 6.6	6.2 / 7.8	7.4 / 9.4
12.0 k $\Omega$ (+20%)	29	1.4 / 1.9	1.9 / 2.5	2.5 / 3.1	3.1 / 3.9	3.9 / 5.3	5.5 / 7.2	6.8 / 8.6	8.0 / 10.2
13.0 k $\Omega$ (+30%)	26	1.5 / 2.1	2.1 / 2.7	2.7 / 3.4	3.4 / 4.2	4.2 / 5.8	6.0 / 7.8	7.4 / 9.3	8.7 / 11.1

### DYNAMIC ELECTRICAL CHARACTERISTICS

**Table 6. Dynamic Electrical Characteristics**

Characteristics noted under conditions  $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$ ;  $7.0\text{ V} \leq V_{VFIRE\_XX} \leq 35\text{ V}$ ;  $V_{VDIAG\_X} = V_{VFIRE\_XX}$ ;  
 $FEN\ 1 = FEN\ 2 = V_{DD}$ ;  $R_{R\_LIMIT\_X} = 10\text{ k}\Omega \pm 1\%$ ,  $R_{R\_DIAG} = 10\text{ k}\Omega \pm 1\%$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq +85\text{ }^\circ\text{C}$ ,  $GND = 0$ , unless otherwise noted.  
 Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>SERIAL INTERFACE</b>					
CLK Cycle Time (1/FCLK) <sup>(18)</sup>	$t_{CYC}$	200	–	–	ns
CLK High Time <sup>(18)</sup> $V_{CLK} > V_{DD} \times 70\%$	$t_{HI}$	73	–	–	ns
CLK Low Time <sup>(18)</sup> $V_{CLK} < V_{DD} \times 20\%$	$t_{LO}$	73	–	–	ns
Clock Rise Time <sup>(18)</sup> $V_{CLK} = 20\% V_{DD}$ to $70\% V_{DD}$ , $C_{LOAD} = 100\text{ pF}$	$t_{RISE}$	–	–	20	ns
Clock Fall Time <sup>(18)</sup> $V_{CLK} = 70\% V_{DD}$ to $20\% V_{DD}$ , $C_{LOAD} = 100\text{ pF}$	$t_{FALL}$	–	–	20	ns
Data Out Rise Time <sup>(19)</sup> $V_{DO} = 20\% V_{DD}$ to $70\% V_{DD}$ , $C_{LOAD} = 100\text{ pF}$	$t_R$	–	–	20	ns
Data Out Fall Time <sup>(19)</sup> $V_{DO} = 70\% V_{DD}$ to $20\% V_{DD}$ , $C_{LOAD} = 100\text{ pF}$	$t_F$	–	–	20	ns
Chip Select Setup Time <sup>(19)</sup> CSB ↓ Before CLK ↑	$t_{LEAD}$	73	–	–	ns
Chip Select Hold Time <sup>(19)</sup> CLK ↓ Before CSB ↑	$t_{LAG}$	73	–	–	ns
Data In Setup Time <sup>(19)</sup> D1 Valid Before CLK ↑	$t_{SU}$	30	–	–	ns
Data In Hold Time <sup>(19)</sup> D1 Hold Time After CLK ↑	$t_H$	30	–	–	ns
Data Out Access Time <sup>(19)</sup> CSB ↓ to D0 Valid	$t_A$	–	–	73	ns
Data Out Disable Time <sup>(19)</sup> CSB ↑ to D0 HI-Z	$t_{DIS}$	–	–	73	ns
Data Out Valid Time <sup>(19)</sup> CLK ↑ to D0 Valid, $C_{LOAD} = 100\text{ pF}$	$t_V$	–	–	75	ns
Data Out Hold Time <sup>(19)</sup> D0 held After CLK ↑	$t_{HO}$	0.0	–	–	ns
Diagnostic Delay Time (Between Two Successive Commands)	$t_{DIAG}$	2.5	–	–	μs

Notes

- 18 Determined by Design
- 19 Guaranteed by Characterization

**Table 6. Dynamic Electrical Characteristics (continued)**

Characteristics noted under conditions  $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$ ;  $7.0\text{ V} \leq V_{VFIRE\_XX} \leq 35\text{ V}$ ;  $V_{VDIAG\_X} = V_{VFIRE\_XX}$ ;  
 FEN 1 = FEN 2 =  $V_{DD}$ ;  $R_{R\_LIMIT\_X} = 10\text{ k}\Omega \pm 1\%$ ,  $R_{R\_DIAG} = 10\text{ k}\Omega \pm 1\%$ ,  $-40\text{ }^\circ\text{C} \leq T_A \leq +85\text{ }^\circ\text{C}$ , GND = 0, unless otherwise noted.  
 Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>FET DRIVERS</b>					
Turn-On Delay Time $\overline{\text{CS}} \uparrow$ to 80% $I_{HS}$	$t_{ON}$	–	–	72	$\mu\text{s}$
Turn-Off Delay Time $\overline{\text{CS}} \uparrow$ to 20% $I_{HS}$	$t_{OFF}$	–	–	10	$\mu\text{s}$
Diagnostic Timing/Resolution $5.0\text{ V} \leq V_{VDIAG\_X} \leq 35\text{ V}$ , $I_{HS} \geq I_{MEAS}$ , $0\text{ s} \leq t_{MEASURE\_TIME} \leq 6.375\text{ ms}$ , $C_{SQIB\_HI} = 0.12\text{ }\mu\text{F}$ , $C_{SQIB\_LO} = 0.12\text{ }\mu\text{F}$	$t_{RESOLUTION}$	21.25	25	28.75	$\mu\text{s}$

**DIAGNOSTIC DELAY TIME**

Squib Resistance Diagnostic Delay Time <sup>(20)</sup> From CSB $\uparrow$ Until Transistor Test Results Are Valid, $C_{SQIB\_HI} = 0.12\text{ }\mu\text{F}$ , $C_{SQIB\_LO} = 0.12\text{ }\mu\text{F}$	$t_{DIAG1}$	–	–	300	$\mu\text{s}$
Squib Open/Short Diagnostic Delay Time <sup>(20)</sup> From CSB $\uparrow$ Until Squib Open/Short Diagnostic Results Are Valid, $C_{SQIB\_HI} = 0.12\text{ }\mu\text{F}$ , $C_{SQIB\_LO} = 0.12\text{ }\mu\text{F}$	$t_{DIAG2}$	–	–	3000	$\mu\text{s}$
VDIAG Supply Diagnostic Delay Time From CSB $\uparrow$ until VDIAG Diagnostic Results Are Valid <sup>(20)</sup>	$t_{DIAG4}$	–	–	100	$\mu\text{s}$
$V_{FIRE}$ Supply Diagnostic Delay Time <sup>(20)</sup> $15\text{ V} \leq V_{VDIAG\_X} \leq 35\text{ V}$ , From CSB $\uparrow$ Until High Side Safing Sensor Diagnostic Results Are Valid, $C_{VDIAG} < 0.015\text{ }\mu\text{F}$	$t_{DIAG6}$	–	–	500	$\mu\text{s}$
High Side Safing Sensor Diagnostic Delay Time <sup>(20)</sup> $15\text{ V} \leq V_{VDIAG\_X} \leq 35\text{ V}$ , From CSB $\uparrow$ Until High-Side Safing Sensor Diagnostic Results Are Valid, $C_{VDIAG} < 0.015\text{ }\mu\text{F}$	$t_{DIAG7}$	–	–	500	$\mu\text{s}$
FET Drivers High and Low Side Driver Transistor Diagnostic Delay Time <sup>(20)</sup> $15\text{ V} \leq V_{VDIAG\_X} \leq 35\text{ V}$ , From CSB $\uparrow$ Until Transistor Test Results Are Valid, $C_{SQIB\_HI} = 0.12\text{ }\mu\text{F}$ , $C_{SQIB\_LO} = 0.12\text{ }\mu\text{F}$ , $C_{VDIAG} < 0.015\text{ }\mu\text{F}$	$t_{DIAG9}$	–	–	1000	$\mu\text{s}$
$V_{FIRE\_RTN}$ Diagnostic Delay Time <sup>(20)</sup> From CSB $\uparrow$ Until $V_{FIRE\_RTN}$ Diagnostic Results Are Valid	$t_{DIAG10}$	–	–	300	$\mu\text{s}$
Squib Continuity Diagnostic Delay Time <sup>(20)</sup> From CSB $\uparrow$ Until $V_{THSQBCON}$ Diagnostic Results Are Valid	$t_{DIAG11}$	–	–	3000	$\mu\text{s}$
Squib Short Between Firing Loops Diagnostic Delay Time From CSB $\uparrow$ Until $V_{THSSQB}$ Diagnostic Results Are Valid <sup>(20)</sup>	$t_{DIAG12}$	–	–	3000	$\mu\text{s}$

**FEN INPUT PIN**

Minimum Pulse Width	$FEN_{FILTER}$	12	14	16	$\mu\text{s}$
---------------------	----------------	----	----	----	---------------

## Notes

20 Guaranteed by Characterization

### TIMING DIAGRAMS

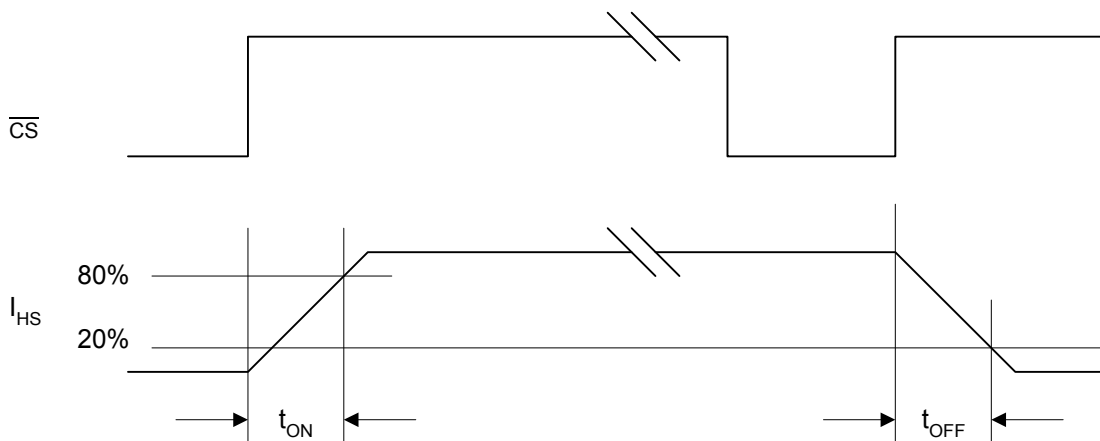


Figure 4. Driver Timing Diagram

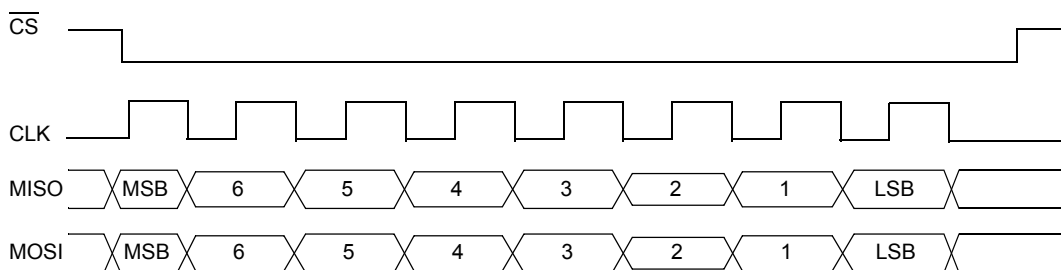


Figure 5. Freescale SPI

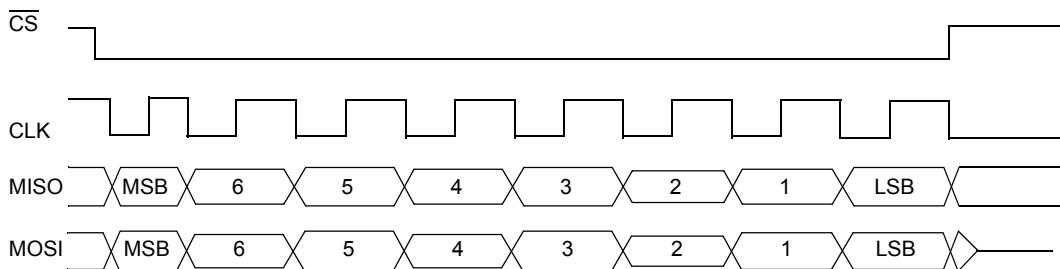


Figure 6. Alternative SCI Mode



## FUNCTIONAL DESCRIPTION

### INTRODUCTION

The Four Channel Squib Driver IC is a complete squib diagnostic and deployment interface for use in automotive air bag modules. Extensive diagnostics and system control features are incorporated to provide fail-safe operation.

The device contains a serial peripheral interface (SPI) compatible 8-bit interface for microprocessor control. This interface allows the microprocessor to set up and read back the results of all internal diagnostic functions. Squib resistance level, along with possible shorts-to-battery or ground, open ground connections, or shorts between squib firing loops, are included in the diagnostic set. Additionally, the squib supply voltage levels can be checked and the low

side fire return can be checked for an open condition (open ground connection). The SPI interface, along with the additional FEN pin, is used to arm and fire a selected squib.

The device has the capability to be used in a standard four-channel squib driver IC or in a cross-coupled state with the high and low side squib drivers located on separate squib driver ICs.

Both the high side and low side output drivers are protected against temporary shorts to battery or ground. The current limit threshold is set by an external resistor.

### FUNCTIONAL PIN DESCRIPTION

#### INTRODUCTION

In this section references are made to XX; e.g., in SENSE\_XX, SQB\_LO\_XX, and SQB\_LO\_XX\_CONT. In these and similar instances, XX denotes 1A, 1B, 2A, and 2B.

#### SERIAL CLOCK (SCLK)

Serial clock input for SPI interface. Data on the D1 pin is clocked into the device on the rising edge. Data is clocked out of the device via the D0 pin on the falling edge. Default state is low with no connection.

#### CHIP SELECT ( $\overline{\text{CS}}$ )

Chip select for SPI interface. Active low. On rising edge, data shifted into the shift register is internally latched. On falling edge, diagnostic results are latched into shift register. Default state is high with no connection.

#### MASTEROUT/SLAVE IN (MOSI)

Serial data input to 33797 SPI interface. Default state is low with no connection.

#### MASTER IN/SLAVE OUT (MISO)

Serial data output from 33797 SPI interface.

#### FET DRIVER 1A AND 1B (FEN\_1)

Active high input signal to enable operation of squibs 1A and 1B FET drivers. All diagnostic functions are available while pin is low. Default state is low with no connection.

#### FET DRIVER 2A AND 2B (FEN\_2)

Active high input signal to enable operation of squibs 2A and 2B FET drivers. All diagnostic functions are available while pin is low. Default state is low with no connection.

#### DEVICE GROUND (GND)

Device ground pin for internal logic and diagnostic circuitry.

#### DEVICE POWER (VDD)

Device power pin for internal logic and diagnostic circuitry.

#### RESET ( $\overline{\text{RST}}$ )

Reset Bar. Active low. With low input signal the internal functions of the squib driver IC are disabled and all data in the serial interface shift registers is cleared. Default state is low with no connection.

#### LIMIT RESISTOR - DIAGNOSTIC (R\_DIAG)

External resistor to ground is used to set the diagnostic current for squib resistance.

#### LIMIT RESISTOR 1A AND 1B (R\_LIMIT\_1)

External resistor to ground is used to set current limit for squibs 1A and 1B FET drivers.

#### LIMIT RESISTOR 2A AND 2B (R\_LIMIT\_2)

External resistor to ground is used to set current limit for squibs 2A and 2B FET drivers.

#### SQUIB DIAGNOSTIC 1A AND 1B (VDIAG\_1)

Diagnostic pins for the high side safing sensors for squibs 1A and 1B, as well as the VFIRE supply voltage.

#### SQUIB DIAGNOSTIC 2A AND 2B (VDIAG\_2)

Diagnostic pins for the high side safing sensors for squibs 2A and 2B, as well as the VFIRE supply voltage.

## SQUIB SENSE XX (SENSE\_XX)

The Sense pins are used *exclusively* for diagnostics related to the squib, driver FETs, or harness. Commands using the Sense pins include:

- C1, C2, C3, C9
- D<3:0>
- E<3:0>
- E9
- 82/1x
- 83/2x

Independent of the system configuration, normal or cross coupled, the Sense pin, xx and SquibHi, xx of a single IC are *always* connected to the *same* squib with the SquibHi pin connected to the high pin of the squib and the Sense pin connected to the low pin of the squib. A cross coupled configuration is achieved by *only cross coupling* the squib low pins. See [Figure 7](#) and [Figure 8](#).

## STANDARD APPLICATIONS

In the standard mode, the \$C2 (SQUIB\_LO\_XX\_CONT) command will be used to check continuity of the low side driver from the SQB\_LO\_XX pin to the high side driver FET (see [Figure 6](#)).

## CROSS-COUPLED APPLICATIONS

Used during cross-coupling applications involving two four channel squib driver ICs (squib driver IC #1 and squib driver IC #2). SENSE\_XX pins from squib driver IC #1 are connected to their respective squib minus pins (Squib Low/ SQB\_LO\_XX) from squib driver IC #2 ([Figure 8](#)).

SENSE\_XX pins are used to feed diagnostic signals back to squib driver IC #1 for determining squib resistance, short-to-battery/ground, and squib loop-to-loop short conditions.

During a fire event, the fire current passes from squib driver IC #1 high side driver through the squib to squib driver IC #2 low side driver ([Figure 8](#)). In the cross-coupled mode, the squib driver IC #2 \$C2 (SQUIB\_LO\_XX\_CONT) command will be used to check continuity of the low side driver from the SQB\_LO\_XX pin to the low side driver FET.

## DESIGN NOTES

Diagnostics always have the form of a forcing function and a measurement or sense function. In a cross couple

configuration, most diagnostics are unaffected and are single commands except for \$C2 Low Side FET Continuity and \$E<3:0> Harness Shorts, and 83/2x Low Side FET test. This command must be sent to each IC to be executed. For these three diagnostics, two commands are required because the *forcing function* and *sensing function* are on separate ICs.

Harness Shorts Diagnostics: Force using \$E<3:0> on IC#1, Sense \$E8 on IC2

Low Side FET Continuity: Force using \$C1 on IC#1, Sense using \$C2 on IC#2

Low Side FET Test: Force using \$C1 on IC#1, Sense using \$C2 on IC#2

An active 600  $\mu$ A current sink is located in the SENSE\_XX pin. The sink current is used to pull the charge off of the external EMC/filter caps after a diagnostic measurement has been made.

## SQUIB HI XX (SQB\_HI\_XX)

Squib high pins for squibs 1A, 1B, 2A, and 2B. These pins are connected to the sources of the high side FET drivers, as well as the diagnostic circuitry.

## SQUIB LOW XX (SQB\_LO\_XX)

Squib low pins for squibs 1A, 1B, 2A, and 2B. These pins are connected to the drains of the low side FET drivers, as well as the diagnostic circuitry.

## SQUIB FIRING SUPPLY XX (VFIRE\_XX)

Firing supply pins for squibs 1A, 1B, 2A, and 2B. These pins are connected to the drains of the high side FET drivers. Feedback for high side safing for squibs 1A and 1B will be referenced from VFIRE\_1A and squibs 2A and 2B from VFIRE\_2A. For high side safing, VFIRE\_1B should be connected to VFIRE\_1A pin and VFIRE\_2B to VFIRE\_2A pin.

## SQUIB FIRE POWER GROUND (VFIRE\_RTN)

Return for squibs 1A, 1B, 2A AND 2B. The pins are tied to the source pins of both low side FET drivers, as well as the diagnostic circuitry. The RTN pins are tied internally.

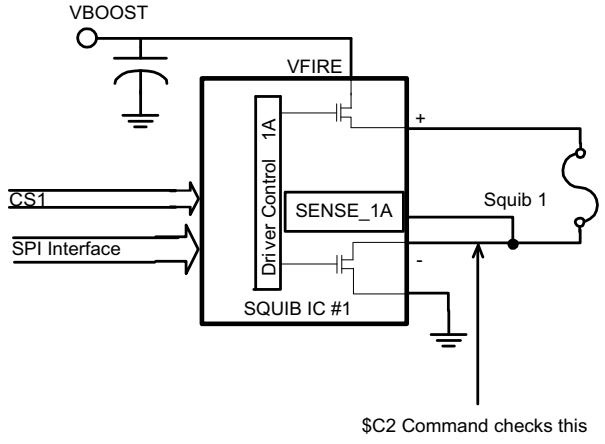


Figure 7. Standard Squib Firing

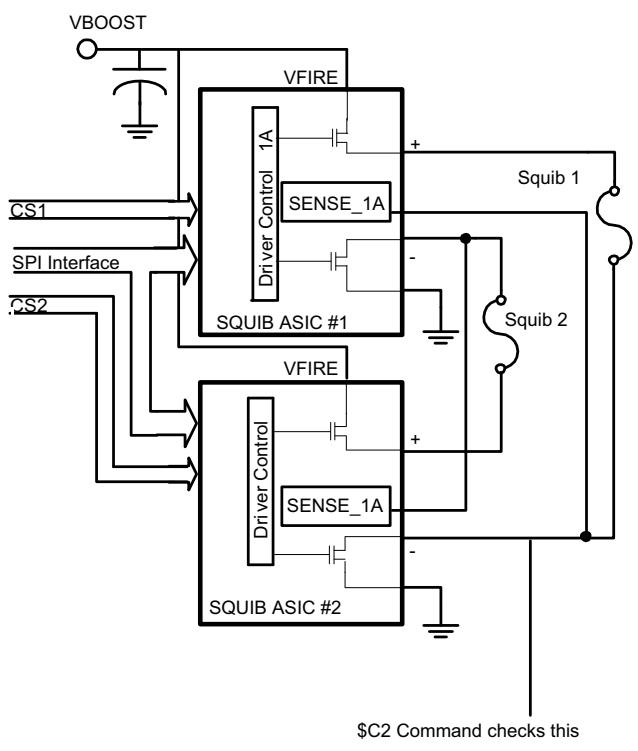


Figure 8. Cross-coupled Squib Firing

## FUNCTIONAL DEVICE OPERATION

### OPERATIONAL MODES

#### INTRODUCTION

In this section references are made to XX; e.g., in SQB\_HI\_XX, SQB\_LO\_XX, and SENSE\_XX pins. SQB\_HI\_XX refers to SQB\_HI\_1A, SQB\_HI\_1B, SQB\_HI\_2A or SQB\_HI\_2B, SQB\_LO\_1A, etc.

#### SERIAL INTERFACE

An 8-bit shift register is provided for communication through the serial port to a microprocessor. The four wire SPI interface is used to read from, and write to, the shift register. Data written to the shift register will control the firing of the FET switches or select a diagnostic mode. Data is sequentially shifted into and out of the shift register, most significant bit first.

Data read from the shift register will contain the results of the diagnostic mode selected in the previous 8-bit write. If a NOP command is written, all diagnostic modes are cleared and the data in the shift registers will be read out. With any undefined commands, all diagnostic modes are cleared and the data in the shift registers will be read out. All functions are set when  $\overline{CS}$  goes high. All diagnostic commands are cleared on the next valid SPI command.

#### SPI INTERFACE INTEGRITY CHECK

The \$96 command with corresponding \$69 return byte during the next 8-bit write is used as an echo function to diagnose the SPI integrity (refer to [Table 9](#)).

The Diagnostic Data Out bits not containing data are set to zero.

Only 8-bit words will be accepted. Any words that are  $\leq 7$  bits or  $\geq 9$  bits will be ignored or cleared.

The second byte for command programming will be treated as a NOP if any FET is firing. The programming commands must be sequential or they will be treated as a NOP.

The four channel squib driver IC is a slave peripheral device designed to interface to a Freescale SPI or other serial peripheral interface. Data is read on the rising edge of CLK, and data is transferred out on the rising edge of CLK. On the falling edge of  $\overline{CS}$ , the IC configures itself for one of two SPI modes. If CLK is low, the IC will configure itself to be in Freescale SPI mode (see [Figure 5](#)). If CLK is high, the IC will configure itself to be in an alternative SCI mode (see [Figure 5](#)). In both cases, data is still read off the rising edge and transferred off the falling edge of the CLK. When the IC is deselected ( $\overline{CS}$  goes high), then D0 is a high-impedance output.

Response bit 7 of command \$C8 (refer to [Table 8](#), page 24) is hard-wired to "1" or "0" to identify the squib IC as a four or two channel squib driver IC. When a \$C8 command is issued for the four channel squib driver IC, the response bit 7 is set

to a "0". When a \$C8 command is issued for the two channel squib driver IC, the response bit 7 is set to a "1".

#### STANDARD SQUIB IC FUNCTION

The standard squib IC application utilizes the high and low side squib drivers from the same squib driver ICs (see [Figure 6](#), Standard Squib Firing).

The SENSE\_XX (1A, 1B, 2A, 2B) pin is connected to SQB\_LO\_XX (1A, 1B, 2A, 2B). Squib diagnostics are conducted using this pin. In the standard mode, the \$C2 (SQUIB\_LO\_XX\_CONT) command will be used to check continuity of the low side driver from the SQB\_LO\_XX pin (1A, 1B, 2A, 2B) to the low side driver FET ([Figure 6](#)).

The low side driver continuity is checked during the continuity test. The driver continuity information will be cleared after the information is transmitted on the next valid SPI command.

#### EXAMPLE—STANDARD SQUIB COMMAND SPI SEQUENCE FROM MICROCONTROLLER

TX: Request squib short-to-battery/GND diagnostic measurement (\$C1).

RX: Previous executed command information.

TX: Request squib 1A resistance measurement (\$D0-\$D3).

RX: Receive results from short-to-battery/GND diagnostics.

TX: Request squib 1B resistance measurement (\$D0-\$D3).

RX: Receive measured squib 1A resistance information.

TX: Request squib 2A resistance measurement (\$D0-\$D3).

RX: Receive measured squib 1B resistance information.

TX: Request squib 2B resistance measurement (\$D0-\$D3).

RX: Receive measured squib 2A resistance information

TX: Request continuity command (\$C2).

RX: Receive measured squib 2B resistance information

TX: Request another command sequence.

RX: Receive low side driver 1A, 1B, 2A, and 2B continuity information. Latches will be cleared after data transferred from the squib IC (clear on rising edge of chip select).

TX: Request loop-to-loop short command (\$E0-\$E3)

RX: Previous executed command information.

TX: Request another command sequence.  
 RX: Receive loop-to-loop results from test.

### CROSS-COUPLED SQUIB IC FUNCTION

The cross-coupled application utilizes the high and low side squib drivers from two different squib driver ICs (see [Figure 8](#), Cross-Coupled Squib Firing, page 19.) Through the SPI interface, the squib IC will maintain the capability to conduct standard diagnostics (short-to-battery, short-to-ground, short between squibs, and squib diagnostics) between two different squib ICs. The squib IC must maintain the capability to fire the squib drivers with the ARM and FIRE command in either cross-coupled or single IC applications.

When the firing squib driver IC is used in cross-coupled applications, the low side squib driver must be activated prior to activating the high side squib driver.

Cross-coupling the high and low side squib driver from two different squib driver ICs must be done without interfering with standard squib operations when the squib IC is used in an application where the high and low side squib drivers are located on the same IC.

All remaining diagnostic functions will operate standard in either a cross-coupled or single IC applications. These functions include  $R_{R\_DIAG}$ ,  $R_{R\_LIMIT\_X}$ , high side,  $V_{VFIRE\_XX}$ ,  $V_{VFIRE\_RTN}$ ,  $V_{TRANSTX}$ , squib current timing measurement, and FEN\_1 and FEN\_2 diagnostics.

The SENSE\_1A (1B, 2A, or 2B) pin squib IC #1 is connected to SQB\_LO\_1A (1B, 2A, or 2B) pin squib driver IC #2 and is used to feed the diagnostic signal for determining squib resistance and short-to-battery/ground conditions (see [Figure 8](#), page 19). During a fire event, the fire current passes from squib driver IC #1 high side driver through the squib to squib driver IC #2 low side driver. In the cross-coupled mode, the squib driver IC #2 \$C2 (SQUIB\_LO\_1A\_CONT, [1B, 2A, or 2B]) command will be used to check continuity of the low side driver from the SQB\_LO\_1A (1B, 2A, or 2B) pin to the low side driver FET.

The low side driver continuity is checked during the continuity test. The driver continuity information will be cleared after the information is transmitted on the next valid SPI command.

### EXAMPLE—CROSS-COUPLED SQUIB COMMAND SPI SEQUENCE FROM MICROCONTROLLER

TX: Squib IC #1 request squib 1A resistance measurement (\$D0).  
 RX: Previous executed command information.

TX: Run another command on the same squib IC #1.  
 RX: Receive measured squib 1A resistance information.

TX: Squib IC #1 request continuity command (\$C2).  
 RX: Previous executed command information.

TX: Squib IC #2 request continuity command (\$C2).  
 RX: Previous executed command information.

TX: Squib IC #2 request continuity command (\$C2).  
 RX: Receive low side driver continuity information for low side drivers which reside on IC #2.

TX: Squib IC #1 request another command sequence.  
 RX: Receive low side driver continuity information for low side drivers that reside on IC #1.

TX: Squib IC #1 request loop-to-loop short command (\$E0–\$E3).  
 RX: Previous executed command information.

TX: Squib IC #2 request loop to loop short command for other ICs (\$E8).  
 RX: Previous executed command information.

TX: Squib IC #2 request loop-to-loop short command for other ICs (\$E8).  
 RX: Receive loop-to-loop results from test run on IC #1.

TX: Squib IC #1 request another command sequence.  
 RX: Receive loop-to-loop results from test run on IC #1.

### FIRING A SQUIB

The firing of a squib driver requires the FEN\_1 and FEN\_2 pins to be high and two separate 8-bit writes be made to the shift register. With FEN\_1 pin high, squibs 1A and 1B can be armed and fired. With FEN\_2 pin high, squibs 2A and 2B can be armed and fired. The first write is to ARM squib drivers in preparation of receiving the fire command. Squib 1A and squib 1B can be armed separately from squib 2A and squib 2B (refer to [Table 7](#)) or all squibs can be fired at once (refer to [Table 8](#)). All ARM and 5X (Fire) commands will be echoed back on the SPI Data output.

**Table 7. Squib Firing Commands**

Hex Code	Command Description							
A0	ARM Squib Drivers 1A and 1B							
A1	ARM Squib Drivers 2A and 2B							
Byte #1								
Byte #2	Squib B High Side	Squib B Low Side	Squib A High Side	Squib A Low Side	Squib 2B	Squib 2A	Squib 1B	Squib A1
A0	ARM Squib Drivers 1A and 1B							
A1	ARM Squib Drivers 2A and 2B							
A2					ARM Squib Drivers 1A, 1B, 2A, 2B			
50	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
51	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON
52	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
53	OFF	OFF	ON	ON	OFF	OFF	ON	ON
54	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF
55	OFF	ON	OFF	ON	OFF	ON	OFF	ON
56	OFF	ON	ON	OFF	OFF	ON	ON	OFF
57	OFF	ON	ON	ON	OFF	ON	ON	ON
58	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF
59	ON	OFF	OFF	ON	ON	OFF	OFF	ON
5A	ON	OFF	ON	OFF	ON	OFF	ON	OFF
5B	ON	OFF	ON	ON	ON	OFF	ON	ON
5C	ON	ON	OFF	OFF	ON	ON	OFF	OFF
5D	ON	ON	OFF	ON	ON	ON	OFF	ON
5E	ON	ON	ON	OFF	ON	ON	ON	OFF
5F	ON	ON	ON	ON	ON	ON	ON	ON

The second write is to actually fire the desired driver. The four most significant bits of the second write are used to establish a parity with the four most significant bits of the first write. The four least significant bits are the data bits, and each bit represents a squib driver or squib driver pair. If there is a parity mismatch of the four most significant bits, the data bits will be ignored and the squib drivers will not have their status changed. The 2-byte write sequence must then be started again. During the first write, when the drivers are armed, all diagnostic functions are cleared.

Once fired, a driver can only be turned off by one of the following:

- Sending a valid 2-byte write sequence through the shift register.
- Having the reset pin pulled low.
- Having the thermal shutdown limit exceeded (once minimum firing duration requirement has been met; refer to Note <sup>(4)</sup> in [Maximum Ratings](#)).

- Having the FEN pin pulled low. Note that the code sequences allow any combination of drivers to be turned on or off.

Once fired, the current limit measurement register increments when the squib current is measured and is above the  $I_{MEAS}$  threshold during the timer activation.

The FEN\_1 or FEN\_2 pin must be high to enable firing of the drivers. If fire command is active and the FEN (1 or 2) pin is pulled low, the FET drivers will turn off (assuming the latch and hold function is not in effect; refer to paragraph entitled FEN\_1 and FEN\_2, [FEN\\_1 and FEN\\_2 \(FEN\) \(\\$C8 Command\)](#)). If fire command is active and the FEN (1 or 2) pin is pulled high, the FET driver will turn on.

During the firing of a squib, significant I•R losses may occur, which could cause a voltage shift across a circuit board trace. It is recommended that current paths for discharging the firing supply storage capacitors through the squib be kept as short as possible and isolated from logic and diagnostic grounds.



**Table 8. Diagnostic Bit Definitions**

Hex Code	Command Description	Diagnostic Data Out (Available on Next Command)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	NOP	0	0	0	0	0	0	0	0
70	Squib 1A Current Measurement Time	SQB_1A BIT 7 MS	SQB_1A BIT 6	SQB_1A BIT 5	SQB_1A BIT 4	SQB_1A BIT 3	SQB_1A BIT 2	SQB_1A BIT 1	SQB_1A BIT 0 LS
71	Squib 1B Current Measurement Time	SQB_1B BIT 7 MS	SQB_1B BIT 6	SQB_1B BIT 5	SQB_1B BIT 4	SQB_1B BIT 3	SQB_1B BIT 2	SQB_1B BIT 1	SQB_1B BIT 0 LS
72	Squib 2A Current Measurement Time	SQB_2A BIT 7 MS	SQB_2A BIT 6	SQB_2A BIT 5	SQB_2A BIT 4	SQB_2A BIT 3	SQB_2A BIT 2	SQB_2A BIT 1	SQB_2A BIT 0 LS
73	Squib 2B Current Measurement Time	SQB_2B BIT 7 MS	SQB_2B BIT 6	SQB_2B BIT 5	SQB_2B BIT 4	SQB_2B BIT 3	SQB_2B BIT 2	SQB_2B BIT 1	SQB_2B BIT 0 LS
79	Squib X Current Status	0	0	0	0	SQB_2B Current Limit Status	SQB_2A Current Limit Status	SQB_1B Current Limit Status	SQB_1A Current Limit Status
7F	Thermal Shutdown Status Thermal <sub>SD</sub>	Thermal LSDSTAT_2B	Thermal HSDSTAT_2B	Thermal LSDSTAT_2A	Thermal HSDSTAT_2A	Thermal LSDSTAT_1B	Thermal HSDSTAT_1B	Thermal LSDSTAT_1A	Thermal HSDSTAT_1A
C0	VDIAG and High Side Safing Sensor Diagnostics	RSSLO	RSSHI	V <sub>DIAG_2</sub> VDHI	V <sub>DIAG_2</sub> VDLO	RSSLO	RSSHI	V <sub>DIAG_1</sub> VDHI	V <sub>DIAG_1</sub> VDLO
C1	Squib Short-to-Ground/Short-to-Battery Diagnostics	SQB_2B NO_SH_GND	SQB_2B NO_SH_BATT	SQB_2A NO_SH_GND	SQB_2A NO_SH_BATT	SQB_1B NO_SH_GND	SQB_1B NO_SH_BATT	SQB_1A NO_SH_GND	SQB_1A NO_SH_BATT
C2	Low Side Driver Continuity Status	0	0	0	0	SQB_LO_2B_CONT	SQB_LO_2A_CONT	SQB_LO_1B_CONT	SQB_LO_1A_CONT
C3	Harness Short-to-Ground/ Short-to-Battery with Squib Open (No Squib Present)	SQB_2B OPEN NO_SH_GND	SQB_2B OPEN NO_SH_BATT	SQB_2A OPEN NO_SH_GND	SQB_2A OPEN NO_SH_BATT	SQB_1B OPEN NO_SH_GND	SQB_1B OPEN NO_SH_BATT	SQB_1A OPEN NO_SH_GND	SQB_1A OPEN NO_SH_BATT
Hex Code	Command Description	Diagnostic Data Out (Available on Next Command)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C5	VFIRE_1B and VFIRE_2B Voltage	0	0	0	V <sub>FIRE_B</sub> Tested	X	X	V <sub>HI</sub>	V <sub>LO</sub>
C6	VDIAG_1 and VDIAG_2 Diagnostics	V <sub>DIAG_2</sub> V4	V <sub>DIAG_2</sub> V3	V <sub>DIAG_2</sub> V2	V <sub>DIAG_2</sub> V1	V <sub>DIAG_1</sub> V4	V <sub>DIAG_1</sub> V3	V <sub>DIAG_1</sub> V2	V <sub>DIAG_1</sub> V1

**Table 8. Diagnostic Bit Definitions (continued)**

C8	FEN Status, R_LIMIT_X, R_DIAG Status, IC Type	1	R_LIMIT_2 NO_FAULT	R_LIMIT_1 NO_FAULT	R_DIAG NO_FAULT	FEN 2 Latch Status	FEN 1 Latch Status	FEN 2 Status	FEN 1 Status
C9	VFIRE_RTN Status (Open Ground)	0	0	0	0	0	0	V <sub>FIRE_RTN_2</sub> VF2LOW	V <sub>FIRE_RTN_1</sub> VF1LOW
D0	Squib 1A Resistance	SQB_1A RC8	SQB_1A RC7	SQB_1A RC6	SQB_1A RC5	SQB_1A RC4	SQB_1A RC3	SQB_1A RC2	SQB_1A RC1
D1	Squib 1B Resistance	SQB_1B RC8	SQB_1B RC7	SQB_1B RC6	SQB_1B RC5	SQB_1B RC4	SQB_1B RC3	SQB_1B RC2	SQB_1B RC1
D2	Squib 2A Resistance	SQB_2A RC8	SQB_2A RC7	SQB_2A RC6	SQB_2A RC5	SQB_2A RC4	SQB_2A RC3	SQB_2A RC2	SQB_2A RC1
D3	Squib 2B Resistance	SQB_2B RC8	SQB_2B RC7	SQB_2B RC6	SQB_2B RC5	SQB_2B RC4	SQB_2B RC3	SQB_2B RC2	SQB_2B RC1
E0	Shorts Between Squib Loops, Squib 1A	0	0	0	0	SQB_2B SQB_1A	SQB_2A SQB_1A	SQB_1B SQB_1A	SQB_1A
E1	Shorts Between Squib Loops, SQUIB 1B	0	0	0	0	SQB_2B SQB_1B	SQB_2A SQB_1B	SQB_1B	SQB_1A SQB_1B
E2	Shorts Between Squib Loops, Squib 2A	0	0	0	0	SQB_2B SQB_2A	SQB_2A	SQB_1B SQB_2A	SQB_1A SQB_2A
E3	Shorts Between Squib Loops, Squib 2B	0	0	0	0	SQB_2B	SQB_2A SQB_2B	SQB_1B SQB_2B	SQB_1A SQB_2B
E8	Shorts Between Squib Loops, for Additional ICs	0	0	0	0	SQB_2B SHORT	SQB_2A SHORT	SQB_1B SHORT	SQB_1A SHORT



**Table 9. Command Programming and Diagnostic Bit Definitions**

Hex Code	Command Description	Command Programming Input and Diagnostic Data Out (Available on Next Command) <sup>(21)</sup>							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3X	Current Measurement Register Reset Command for Squib X Current 1 = ON	0	0	1	1	SQB_2B Data/Timer Reset	SQB_2A Data/Timer Reset	SQB_1B Data/Timer Reset	SQB_1A Data/Timer Reset
	DATA OUT Squib X Current Register Reset Status	0	0	1	1	SQB_2B Data/Timer Reset	SQB_2A Data/Timer Reset	SQB_1B Data/Timer Reset	SQB_1A Data/Timer Reset
80	Unlock for FEN 1 Counter Registers Programming.	1	0	0	0	0	0	0	0
	Response DATA Output: Command Echoed	1	0	0	0	0	0	0	0
XX	Programming Command for FEN 1 Counter 1 = ON	FEN1 CNT BIT 7 MSB	FEN1 CNT BIT 6	FEN1 CNT BIT 5	FEN1 CNT BIT 4	FEN1 CNT BIT 3	FEN1 CNT BIT 2	FEN1 CNT BIT 1	FEN1 CNT BIT 0 LSB
	Response DATA OUT FEN 1 Counter Programming Status	FEN1 CNT BIT 7 MSB	FEN1 CNT BIT 6	FEN1 CNT BIT 5	FEN1 CNT BIT 4	FEN1 CNT BIT 3	FEN1 CNT BIT 2	FEN1 CNT BIT 1	FEN1 CNT BIT 0 LSB
81	Unlock for FEN 2 Counter Registers Programming	1	0	0	0	0	0	0	1
	Response DATA Output: Command Echoed	1	0	0	0	0	0	0	1

**Notes**

- 21 The second byte for command programming will be treated as a NOP if any FET is firing. The programming commands have to be sequential or they will be treated as a NOP.

**Table 9. Command Programming and Diagnostic Bit Definitions (continued)**

Hex Code	Command Description	Command Programming Input and Diagnostic Data Out (Available on Next Command) <sup>(22)</sup>							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XX	Programming Command for FEN 2 Counter 1 = ON	FEN2 CNT BIT 7 MS	FEN2 CNT BIT 6	FEN2 CNT BIT 5	FEN2 CNT BIT 4	FEN2 CNT BIT 3	FEN2 CNT BIT 2	FEN2 CNT BIT 1	FEN2 CNT BIT 0 LS
	Response DATA OUT FEN 2 Counter Programming Status	FEN2 CNT BIT 7 MS	FEN2 CNT BIT 6	FEN2 CNT BIT 5	FEN2 CNT BIT 4	FEN2 CNT BIT 3	FEN2 CNT BIT 2	FEN2 CNT BIT 1	FEN2 CNT BIT 0 LS
82	Unlock to Test High Squib Drivers 1A, 1B, 2A, 2B	1	0	0	0	0	0	1	0
	Response DATA Output: Command Echoed	1	0	0	0	0	0	1	0
1X	High Side Driver Transistor Test Command	0	0	0	1	SQB_2B High Side Driver "ON"	SQB_2A High Side Driver "ON"	SQB_1B High Side Driver "ON"	SQB_1A High Side Driver "ON"
	Response DATA OUT High Side Driver Transistor Status $V_{TRANTST1}$	0	0	0	0	SQB_2B HSDSTAT_2B	SQB_2A HSDSTAT_2A	SQB_1B HSDSTAT_1B	SQB_1A HSDSTAT_1A
83	Unlock to Test Low Squib Drivers 1A, 1B, 2A, and 2B	1	0	0	0	0	0	1	1
	Response Data Output: Command Echoed	1	0	0	0	0	0	1	1
2X	Low Side Driver Transistor Test Command	0	0	1	0	SQB_2B Low Side Driver "ON"	SQB_2A Low Side Driver "ON"	SQB_1B Low Side Driver "ON"	SQB_1A Low Side Driver "ON"
	Response DATA OUT Low Side Driver Transistor Status $V_{TRANTST2}$	0	0	0	0	SQB_2B LSDSTAT_2B	SQB_2A LSDSTAT_2A	SQB_1B LSDSTAT_1B	SQB_1A LSDSTAT_1A

Notes

- 22 The second byte for command programming will be treated as a NOP if any FET is firing. The programming commands have to be sequential or they will be treated as a NOP.

**Table 9. Command Programming and Diagnostic Bit Definitions (continued)**

Hex Code	Command Description	Command Programming Input and Diagnostic Data Out (Available on Next Command) <sup>(23)</sup>							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
90	Reserved for Freescale Read NVM Low	X	X	X	X	X	X	X	X
91	Reserved for Freescale Read NVM High	X	X	X	X	X	X	X	X
92	Reserved for Freescale NVM Enable	X	X	X	X	X	X	X	X
93	Reserved for Freescale Test Mode Enable	X	X	X	X	X	X	X	X
96	SPI Integrity Check	1	0	0	1	0	1	1	0
	Response DATA OUT: \$69 Echo to Diagnose the SPI Integrity	0	1	1	0	1	0	0	1

**Notes**

- 23 The second byte for command programming will be treated as a NOP if any FET is firing. The programming commands have to be sequential or they will be treated as a NOP.

## PROTECTION AND DIAGNOSIS FEATURES

The diagnostic circuit's internal references are provided by a bandgap voltage reference, and by scaled currents determined by the resistor value of R\_DIAG and the value of the bandgap voltage. Refer to [Table 8](#), and [Table 9](#), as necessary throughout this section.

### R\_DIAG and R\_LIMIT\_X RESISTOR DIAGNOSTICS (\$C8 COMMAND)

This function monitors reference currents derived by the R\_LIMIT\_1, R\_LIMIT\_2, and R\_DIAG resistors. An open pin or short to ground will cause the comparator to give an "out of range resistor value" indication. A short to VDD will have the same effect as an open pin and will cause an "out of range resistor value" indication.

### R\_LIMIT\_X and R\_DIAG DATA RESULTS

If R\_LIMIT\_X is open, shorted to ground, or shorted to VDD, the bit R\_LIMIT\_NO\_FAULT will be set to "0". Standard operation will have this bit set to "1".

If R\_DIAG is open, shorted to ground, or shorted to VDD, the bit R\_DIAG\_NO\_FAULT will be set to "0". Standard operation will have this bit set to "1".

The FEN 1 and FEN 2 status bits are a reflection of the FEN\_1 and FEN\_2 pins.

### HIGH SIDE SAFING SENSOR DIAGNOSTICS (\$C0 COMMAND)

This function monitors the VFIRE\_XX pin connection to the VDIAG\_X pin. The high side safing function is attached to the VFIRE\_1A and VFIRE\_2A pins. The high side safing function is not available on the VFIRE\_1B and VFIRE\_2B pins.

When enabled, this diagnostic circuit will typically draw less than 500  $\mu$ A from the VFIRE supply voltage source.

Internal window comparators will monitor the voltage difference between the VDIAG\_X pin and the VFIRE\_XX pin, and will provide two bits of data to indicate if the pin voltage is either above (open) or below (shorted) the threshold levels.

When using a high side safing sensor, typical 5.1 k $\Omega$  reference resistor must be placed across the sensor to provide a current path for the diagnostic circuit. As long as there is a current path and the safing sensor switch is open, the resulting differential voltage will fall between the comparator thresholds so neither an open fault nor a shorted fault condition will be indicated. A closed safing sensor will be

indicated as a short, and a loss of the connection between the VDIAG\_X pin and the VFIRE\_XX pin will be indicated as an open. Any external capacitance on the VFIRE\_XX pin will affect the time needed to settle to an accurate value.

### HIGH SIDE SAFING SENSOR DIAGNOSTIC DATA RESULTS

If the VFIRE\_XX pin is shorted to the VDIAG\_X pin, the RSSLO bit will be set to “0” and the RSSHI bit will be set to “0”. If the VFIRE\_XX pin has no connection to the VDIAG\_X pin, the RSSLO bit will be set to “1” and the RSSHI bit will be set to “1”. Standard operation with a safing sensor resistor will have the RSSHI bit set to “0” and the RSSLO bit set to “1”.

### FIRING SUPPLY VOLTAGE (VDIAG\_X) DIAGNOSTICS (\$C0 COMMAND)

This function monitors the voltage on the VDIAG\_X pin. The supply voltage is compared to two thresholds (nominal and minimum) and will provide two bits of data to indicate if the pin voltage is above, below, or in between the predetermined threshold levels. There is one diagnostic circuit for each VDIAG\_X pin.

### VDIAG\_X SUPPLY VOLTAGE DIAGNOSTIC DATA RESULTS

If the VDIAG\_X voltage is above the high limit, bits VDHI and VDLO will both be set to “1”. If the VDIAG\_X voltage is between the high limit and the low limit, bit VDHI will be set to “0” and VDLO will be set to “1”. If the VDIAG\_X voltage is below the low limit, bits VDHI and VDLO will both be set to “0”.

### FIRING SUPPLY VOLTAGE (VFIRE\_XX) DIAGNOSTICS (\$C5 COMMAND)

This function monitors the voltage on the VFIRE\_XX pin. The supply voltage is compared to two thresholds (nominal and minimum) and will provide two bits of data to indicate if the pin voltage is above, below, or in between the predetermined threshold levels. There is one diagnostic circuit for each VFIRE\_XX pin.

### VFIRE\_XX SUPPLY VOLTAGE DIAGNOSTIC DATA RESULTS

If the VFIRE\_XX voltage is above the high limit, bits VFHI and VFLO will both be set to “1”. If the VFIRE\_XX voltage is between the high limit and the low limit, bit VFHI will be set to “0” and VFLO will be set to “1”. If the VFIRE\_XX voltage is below the low limit, bits VFHI and VFLO will both be set to “0”.

### FIRING SUPPLY VOLTAGE DIAGNOSTICS, VDIAG\_X V1, V2, V3, V4 (\$C6 COMMAND)

The VDIAG\_X V1, V2, V3, V4 function monitors voltage on the VDIAG pins. The voltage being measured is then

compared to four thresholds and will provide four bits of data to indicate if the pin voltage is above, below, or between the predetermined threshold levels. There is one diagnostic circuit for each VDIAG\_X pin.

### VDIAG\_X VOLTAGE DIAGNOSTIC DATA RESULTS

If the VDIAG\_X voltage is above the threshold limit, the VDIAG\_X VX bit will be set to “1”. If the VDIAG\_X voltage is below the threshold limit, the VDIAG\_X VX bit will be set to “0”.

### VFIRE\_RTN DIAGNOSTICS (\$C9 COMMAND)

This function monitors the resistance on the VFIRE\_RTN pin for open pin connections. The VFIRE\_RTN voltage is compared to a threshold to determine if the VFIRE\_RTN pin connection between the pin and the printed circuit board is shorted or open.

### VFIRE\_RTN DIAGNOSTIC DATA RESULTS

If the VFIRE\_RTN pin is above the threshold limit (open), the VFIRE\_RTN X VFXLOW will be set to “1”. If the VFIRE\_RTN pin is below the threshold limit (shorted), the VFIRE\_RTN X VFXLOW will be set to “0”.

VFIRE return tests are disabled during firing.

### DESIGN NOTES

For all standard or cross-coupled squib IC configurations, the SQB\_LO\_XX pin must be tied to a SENSE\_XX pin for either squib IC #1 or squib IC #2 (see [Figure 6](#) and [Figure 8](#)).

An active 600  $\mu$ A current sink is located in the SENSE\_XX pin. The sink current is used to pull the charge off the external EMC/filter caps after a diagnostic measurement has been made.

### SQUIB SHORT-TO-BATTERY/GROUND DIAGNOSTICS (\$C1 COMMAND)

This function monitors the voltage on the SENSE\_XX pins. The voltage is compared to two thresholds (minimum and maximum) and will provide two bits of data to indicate if the pin voltage is above, below, or in between the predetermined threshold levels.

When enabled, a 2.7 mA current source located in the SQB\_HI\_XX pin is activated, sourcing current from the SQB\_HI\_XX to the SENSE\_XX pin. When resistive measurement legs to comparators located in the SENSE\_XX pin are activated, a fault on either side of the squib can be easily detected. An external current path that causes the SQB\_LO\_XX, SQB\_HI\_XX, or SENSE\_XX pin to be pulled below the minimum threshold, will be indicated as a “Short to Ground”.

If the SQB\_LO\_XX, SQB\_HI\_XX, or SENSE\_XX pin has an external current path that causes the pin to be pulled above the maximum threshold, a “Short to Battery” will be indicated.

### SQUIB SHORT-TO-BATTERY/GROUND DIAGNOSTIC DATA RESULTS

If SQB\_LO\_XX, SQB\_HI\_XX, or SENSE\_XX pin is shorted to battery, the bit NO\_SH\_BATT will be set to “0”. If a SQB\_LO\_XX, SQB\_HI\_XX, or SENSE\_XX pin is shorted to ground, the bit NO\_SH\_GND will be set to “0”. During standard operation, both NO\_SH\_BATT and NO\_SH\_GND will be set to “1”.

**Note** This diagnostic circuit uses an internal 2.7 mA current source connected to the SQB\_HI\_XX pin as a bias. If the SQB\_LO\_XX and SQB\_HI\_XX pins have any capacitance (due to discrete capacitors or parasitic loading), the diagnostic condition will require a settling time based on the RC time constant.

### SQUIB HARNESS SHORT-TO-BATTERY/GROUND DIAGNOSTICS WITH AN OPEN SQUIB (\$C3 COMMAND)

This diagnostic function is to be used with no squib present (open squib condition) in the wiring harness. For an open squib condition, the function must monitor the voltage on the SQB\_HI\_XX and SQB\_LO\_XX pins for “Short to Ground” and “Short to Battery” conditions.

This function monitors the voltage on the SENSE\_XX pins. The voltage is compared to two thresholds (minimum and maximum) and will provide two bits of data to indicate if the pin voltage is above, below, or in between the predetermined threshold levels.

When enabled, a pair of opposing N-channel CMOS transistors are activated, creating roughly a 500  $\Omega$  resistance between the SQB\_HI\_XX and SQB\_LO\_XX pins together.

A 2.7 mA current source located in the SQB\_HI\_XX pin is activated, sourcing current from the SQB\_HI\_XX to the SQB\_LO\_XX pin to the SENSE\_XX pin. When resistive measurement legs to comparators located in the SENSE\_XX pin are activated, a short to BAT/GND fault can easily be detected. An external current path that causes the SQB\_LO\_XX, SQB\_HI\_XX, or SENSE\_XX pin to be pulled below the minimum threshold, will be indicated as a “Short-to-Ground”.

If the SQB\_LO\_XX, SQB\_HI\_XX, or SENSE\_XX pin has an external current path that causes the pin to be pulled above the maximum threshold, a “Short-to-Battery” will be indicated.

### SQUIB SHORT-TO-BATTERY/GROUND DIAGNOSTIC DATA RESULTS

If SQB\_LO\_XX, SQB\_HI\_XX, or SENSE\_XX pin is shorted to battery, the bit OPEN\_NO\_SH\_BATT will be set to “0”. If a SQB\_LO\_XX, SQB\_HI\_XX, or SENSE\_XX pin is shorted to Ground, the bit OPEN\_NO\_SH\_GND will be set to “0”. During standard operation, both OPEN\_NO\_SH\_BATT and OPEN\_NO\_SH\_GND will be set to “1”.

#### Notes

1. This diagnostic circuit uses an internal 2.7 mA current source connected to the SQB\_HI\_XX pin as a bias. If

the SQB\_LO\_XX and SQB\_HI\_XX pins have any capacitance (due to discrete capacitors or parasitic loading) the diagnostic condition will require a settling time based on the RC time constant.

2. With an OPEN\_NO\_SH\_GND or OPEN\_NO\_SH\_BATT indicated, the SQB\_HI\_XX or SQB\_LO\_XX line contains the fault condition. The standard squib short-to-battery/ground diagnostics (\$C1) can be executed to determine if the fault condition is on the SQB\_HI\_XX pin or the SQB\_LO\_XX pin.

### CONTINUITY TEST for the LOW SIDE DRIVER SQB\_LO\_XX CONNECTION (\$C2 COMMAND) (LOW SIDE DRIVER CONTINUITY STATUS)

Low side driver continuity is checked during the continuity test diagnostics. This function is used to check continuity at the SQB\_LO\_XX pin connection. When enabled, a 2.0 mA current source located in the SQB\_HI\_XX pin is activated sourcing current from the SQB\_HI\_XX to the SQB\_LO\_XX pin.

For a standard connection, the SQUIB\_LO\_XX\_CON bit will be set to “1”. With an open circuit connection, the SQUIB\_LO\_XX bit will be set to “0”. The driver continuity information will be cleared after the information is transmitted on the next valid SPI command.

### SQUIB RESISTANCE DIAGNOSTICS (\$D0-\$D3 COMMAND)

This function monitors squib resistance. When enabled, a diagnostic current derived from R\_DIAG is passed through the selected squib. The resulting voltage across the squib is amplified and passed to an 8-bit voltage level detector. The eight bits of data will indicate if the selected squib has a resistance value above or below predetermined thresholds. The value of R\_DIAG can be varied to allow the detection range to be altered. Increasing the value of R\_DIAG will reduce the diagnostic current; thus, a higher squib resistance will be needed to reach the same  $R_{TH}$  points. In the case that R\_DIAG is a short-to-ground, the diagnostic current through the squib resistance will typically be less than 50 mA.

### SQUIB RESISTANCE DIAGNOSTIC DATA RESULTS

A comparator result bit set to “1” indicates that the input voltage is above the threshold resistance for that bit. Thus an open squib would cause all bits to be set to “1”; likewise, a shorted squib will cause all bits to be set to “0”.

Squib resistance tests are disabled during firing.

### SQUIB DIAGNOSTICS SHORTS BETWEEN SQUIB LINES (FIRING LOOPS) (\$EX COMMAND)

This function monitors conditions that have shorts between squib lines (firing loops). When enabled, a 2.7 mA current source located in the SQB\_HI\_XX pin is activated sourcing current from the selected SQB\_HI\_XX to the SENSE\_XX pin. The resulting voltage is checked on all other squib lines to

determine if the squib lines are shorted. In applications using more than one squib driver IC, a separate command can also be issued to check all squibs for shorted squib lines.

### SQUIB DIAGNOSTICS SHORTS BETWEEN SQUIB LINES DIAGNOSTIC DATA RESULTS (SHORTS BETWEEN FIRING LOOPS)

A comparator result bit set to “1” for SQUIB\_XX indicates standard test current detected in squib line under test. A comparator result bit set to “0” for SQUIB\_XX indicates faulty diagnostic current detected in squib line under test. A comparator result bit set to “1” for SQUIB\_XX\_SSQB\_YY indicates that the squib line is shorted to the squib under test. A comparator result bit set to “0” for SQUIB\_XX\_SSQB\_YY indicates no shorted squib line detected (standard conditions). If more than two squibs are shorted together, the response will consist of all “0”s.

### RESET (RST)

The RESET pin has an internal current pull-down of typically 40  $\mu$ A. While this pin is low, the internal functions of the squib driver IC are disabled and all data in the serial interface shift registers is cleared. This includes all FEN 1 and 2 counter programming, squib driver activation, and squib driver FET tests. With a minimum system  $V_{DD} \leq 4.1$  V, the system reset bar threshold will be set to “0”.

### FEN\_1 and FEN\_2 (FEN) (\$C8 COMMAND)

FEN\_1 and FEN\_2 have an internal current pull-down of typically 40  $\mu$ A. While the FEN pin is low, firing of the FET drivers is disabled. All internal diagnostic functions and results will be available through the serial interface. The FEN pin must be pulled high to enable firing of the FET drivers. Also, the pin state can be used to turn the FET driver “ON” and “OFF” after the arm and fire command has been issued. (That is, once the FET drivers are turned on, pulling FEN\_1 or FEN\_2 low can turn the drivers off if the latch and hold function is not active, and pulling FEN\_1 or FEN\_2 high will activate the drivers if the fire command is still active). Status of FEN 1 and FEN 2 is contained in the C8 diagnostic byte, as shown in [Table 8](#)).

The FEN\_1 and FEN\_2 function should be capable of latching and holding the enable function for electronic safing function input. This function is required for dual-stage air bag applications. FEN\_1 or FEN\_2 will be considered active when either pin is active (“1”) for more than 12 ms. Tolerance range for the filter to be used will be 12 to 16  $\mu$ s.

When FEN\_1 or FEN\_2 input is active high, the FEN\_1 or FEN\_2 function will be active high. When the FEN\_1 or FEN\_2 input state transitions from high to low, a programmable latching function will hold the FEN function active until the timeout of the FEN timer. The programmable latch and hold function will be capable of delays from 1.0 ms to 255 ms, in 1.0 ms increments. The timer is reset to programmed time when FEN\_1 or FEN\_2 pin transitions from “0” to “1”. The programmable counter delay will be set

through an SPI command during module power-up/prove-out. The default for the counter will be 0 ms.

The bits FEN 1 and FEN 2 STATUS are a reflection of their respective pins.

The counter will be reset to 0-sec time during a reset condition.

#### Notes

1. Status information will be required to read counter-programmed value.
2. Precautions need to be taken in the design to prevent the latching function from becoming a glitch catching function.

### FEN 1 and FEN 2 COUNTER PROGRAMMING (\$80 and \$81 COMMAND)

The FEN 1 and FEN 2 counters require two separate 8-bit writes be made to the shift register. The first write is to unlock (\$80 or \$81) and reset the FEN counter registers in preparation of receiving a command. The second byte contains the programming information to set the required counter delay time (0 ms to 255 ms with 1.0 ms interval). Squib IC Power-Up default and \$80 or \$81 followed by \$00 command will set the counter to 0 ms timer delay (refer to [Table 9](#), page [25](#).)

The FEN 1 and FEN 2 Counter programming status bits are a reflection of the counters programming. The programming status information can be compared to the data sent to ensure the squib driver was programmed properly. Counter programming status will be shifted from the shift register during the next read/write operation ([Table 9](#)). All unlock commands will be echoed back on the SPI Data output.

### FET DRIVER CURRENT LIMIT

A single resistor is used to set the current limit protection of the high side drivers of both squib channels. The low side current limit is never less than the high side current limit.

**Table 10.  $R_{R\_LIMIT\_X}$  Current Limit**

$R_{R\_LIMIT\_X}$	$V_{VFIRE} = 7.0$ V	$V_{VFIRE} = 35$ V
4.32 k $\Omega$	0.92 A	0.92 A
10 k $\Omega$	1.37 A	1.37 A
45.3 k $\Omega$	2.0 A	2.0 A

Example of current limit conditions:

$$R_{R\_LIMIT\_X} = 10 \text{ k}\Omega, I_{HS} = A \pm A$$

The high side driver controls the current through the squib. The current limit for the low side driver is only to protect the low side driver stage from excessive current in the event of a short to battery.

With  $R_{R\_LIMIT\_X}$  conditions  $< 4.32$  k $\Omega$  or shorted to ground, the current limit will default to the  $R_{R\_LIMIT\_X} = 10$  k $\Omega$  current limit, not to exceed. With  $R_{R\_LIMIT\_X}$  resistance value  $> 60$  k $\Omega$



or open, the current limit will default to the  $R_{R\_LIMIT\_X} = 10\text{ k}\Omega$  maximum current limit.

### FET DRIVER CURRENT LIMIT MEASUREMENT (\$7X COMMAND)

This function measures the firing current in each squib line and records the “ON” time in which the  $I_{MEAS}$  is above the threshold for each squib. (Refer to Dynamic Electrical Characteristics table, [Dynamic Electrical Characteristics](#).) The timing registers can be reset via SPI command so additional current measurements can be made.

An 8-bit message will be used to determine 255 time steps. The driver current limit measurement is activated when each individual high side driver is activated. Each time the squib current is measured above the  $I_{MEAS}$  threshold during the timer activation, a status bit will be set to “1”. If the current measured is not above the  $I_{MEAS}$  threshold during the timer activation, the timing data log bit will not increment. Each squib timing register can be reset via SPI command so additional current measurements can be made. Initial squib IC power-up will reset the timing registers (i.e., “Power-ON Reset”). When reset, the current limit measurement register byte will be set to \$00.

Command \$79 will indicate the status of the current limit measurement comparator. The current limit measurement from the test is captured and loaded into the register on the next valid SPI command. When the firing current is above  $I_{MEAS}$ , the current limit is activated and the status bit will be set to “1”. If the firing current is below  $I_{MEAS}$ , the current limit status bit will be set to “0”.

### FET DRIVER CURRENT LIMIT MEASUREMENT RESET COMMAND (\$3X COMMAND)

The current limit status registers can be individually reset with the command set found in [Table 9](#). When the register bit is set to “1” for squib X, the current measurement register will be reset to \$00.

### SQUIB DRIVER THERMAL SHUTDOWN (\$7F COMMAND)

With a nominal squib load, the FET squib driver will *not* enter thermal shutdown until the driver has been active for a minimum of 2.09 ms. The individual squib driver thermal shutdown will not affect other squib drivers firing “ON” times.

With a shorted squib load, the FET squib driver will *not* enter thermal shutdown until the driver has been active for a minimum of 2.090 ms. For the shorted squib load, the associated FET squib driver *may* enter thermal shutdown with an “ON” time of  $2.09\text{ ms} \leq t_{ON} \leq 2.82\text{ ms}$ .

When the thermal shutdown limit is exceeded, the thermal status will be set to “1”. The thermal shutdown status (\$7F) diagnostics latch the thermal bit status when executed. The Squib Driver Thermal shutdown status latch will be cleared after the information is transmitted on the next valid SPI

command (i.e., TX: NOP or next \$7F, latch cleared on rising edge of chip select).

The FET squib driver can be activated through the arm/fire command when the  $TEMP_{RENEWABLE}(\text{MIN})$  is reached (thermal shutdown status “0”).

### $V_{TRANTSTX}$ , HIGH AND LOW SIDE SQUIB DRIVER FET TEST and STATUS (\$82 TO \$83 COMMAND)

This function checks the squib driver FET transistor status. The high and low side squib driver FET test requires FEN\_1 and FEN\_2 pins to be low and two separate 8-bit write commands to be made to the shift register. With the FEN\_1 and FEN\_2 pins status LOW, the first write is to unlock in preparation of receiving the diagnostic command for testing the high and low side squib drivers. The unlock command (\$82 and \$83) is an “AND” function with the FEN\_1 and FEN\_2 BAR. All transistor test unlock commands (\$82 and \$83) will be echoed back on the SPI Data output.

The high or low side squib driver FET test will be aborted if firing from any FET is enabled.

During the first write (unlock command), all diagnostic functions are cleared. After the second write is completed, all other diagnostic functions are made available again.

Squib 1A, squib 1B, squib 2A, and squib 2B high side squib drivers will be activated and diagnosed by the \$82 followed by \$1X diagnostic command (refer to [Table 9](#)). A load from the SQB\_HI\_XX pin to the SENSE\_XX pin is required for the high side squib driver to be tested.

Squib 1A, squib 1B, squib 2A, and squib 2B low side squib drivers will be activated and diagnosed by the \$83 followed by \$2X diagnostic command ([Table 9](#)).

When enabled the high or low side FET driver will be enabled and current limited to a nominal current limit of 10 mA. The high and low side driver test time is not automated and is controlled through SPI.

When either a \$82 or a \$83 command is issued, the previous transistor test will stop to prevent coinciding high and low side FET drive transistors from turning “ON”. This prevents high and low side drivers from being activated simultaneously.

**Note** The high or low side squib driver test is capable of checking a code sequence, allowing any combination of high or low side drivers to be tested.

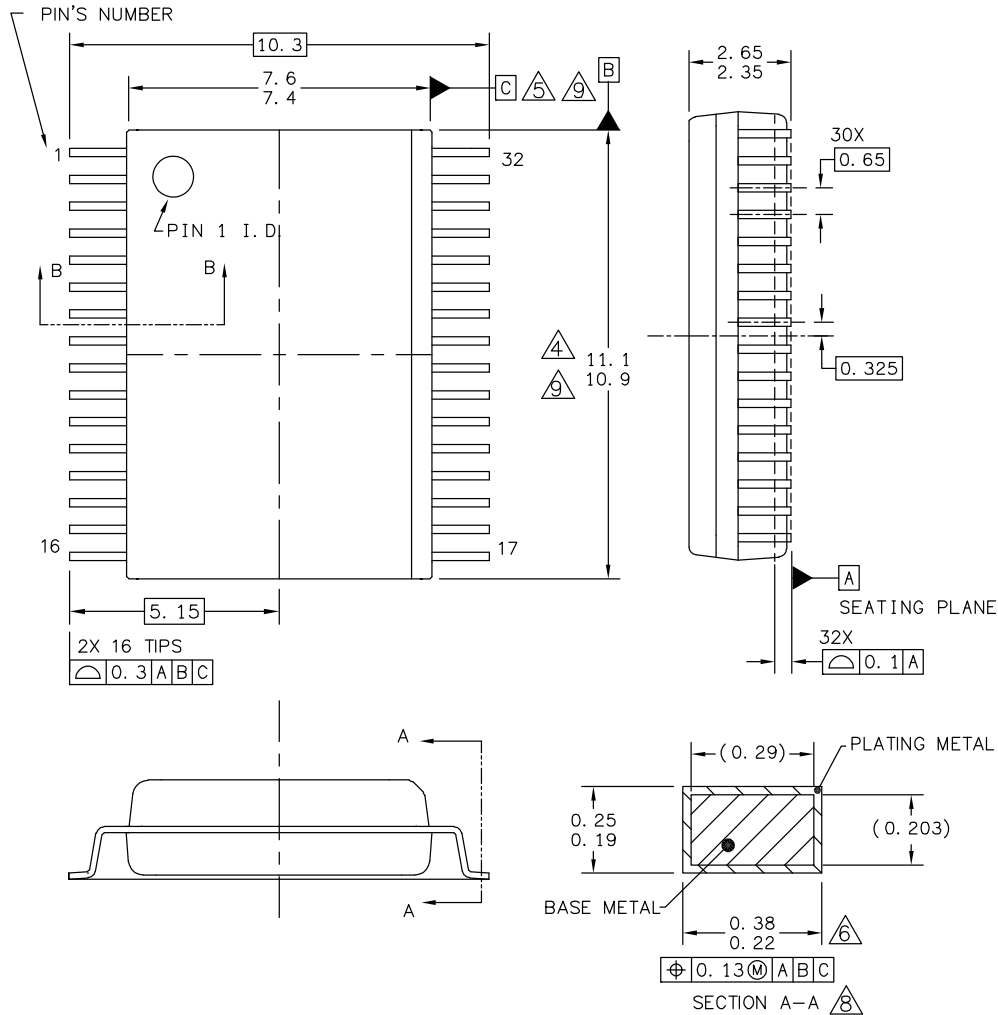
The diagnostic squib driver bit (HSDSTAT\_X or LSDSTAT\_X) will be set to “1” if the squib driver did *not* activate (turn “ON”) during the diagnostic test. The diagnostic squib driver bit (HSDSTAT\_X or LSDSTAT\_X) will be set to “0” if the squib driver did activate (turn “ON”) during the diagnostic test. Diagnostic data will be shifted from the shift register during the next read/write operation.

The diagnostic squib driver register will be set/cleared to “0” when the unlock command is loaded (\$82 or \$83 loaded with rising edge of CS). A diagnostic bit set to “0” indicates standard squib driver transistor operation.

# PACKAGING

## PACKAGE DIMENSIONS

Important For the most current revision of the package, visit [www.freescale.com](http://www.freescale.com) and do a keyword search on the 98A drawing number below.

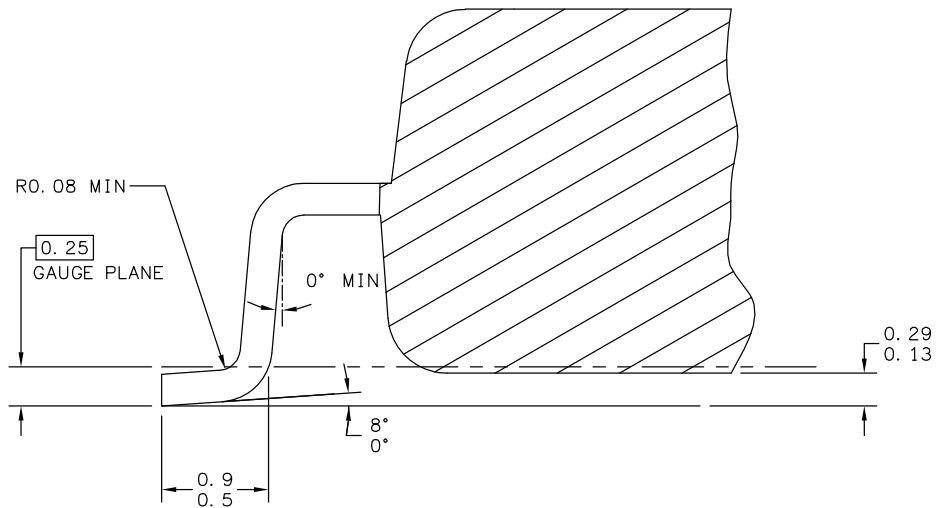


© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	<b>MECHANICAL OUTLINE</b>	PRINT VERSION NOT TO SCALE	
TITLE: 32LD SOIC W/B, 0.65 PITCH CASE OUTLINE	DOCUMENT NO: 98ARH99137A	REV: B	
	CASE NUMBER: 1324-03	07 APR 2005	
	STANDARD: FREESCALE		

**EW SUFFIX (PB-FREE)**

32-PIN  
98ARH99137A  
REVISION B





SECTION B-B

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	<b>MECHANICAL OUTLINE</b>	PRINT VERSION NOT TO SCALE	
TITLE: 32LD SOIC W/B, 0.65 PITCH CASE OUTLINE	DOCUMENT NO: 98ARH99137A	REV: B	
	CASE NUMBER: 1324-03	07 APR 2005	
	STANDARD: FREESCALE		

**EW SUFFIX (PB-FREE)**  
32-PIN  
98ARH99137A  
REVISION B

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	<b>MECHANICAL OUTLINE</b>	PRINT VERSION NOT TO SCALE	
TITLE: 32LD SOIC W/B, 0.65 PITCH, CASE OUTLINE	DOCUMENT NO: 98ARH99137A	REV: B	
	CASE NUMBER: 1324-03	07 APR 2005	
	STANDARD: FREESCALE		

**EW SUFFIX (PB-FREE)**  
32-PIN  
98ARH99137A  
REVISION B

## REVISION HISTORY

Revision	Date	Description of Changes
3.0	11/2006	<ul style="list-style-type: none"> <li>• Updated to the current Freescale format and style</li> <li>• Implemented Revision History page</li> <li>• Added MCZ33797EK/R2</li> <li>• Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from <a href="#">Maximum Ratings on page 6</a>. Added note with instructions from <a href="http://www.freescale.com">www.freescale.com</a>.</li> </ul>
4.0	6/2007	<ul style="list-style-type: none"> <li>• In Static Electrical Table changed Input Voltage minimum from 4.57 to <a href="#">4.75 on page 7</a>, for symbol <math>I_{THSQB\ CON}</math>, corrected Unit of Measurement from mA to <math>\mu A</math>, and for VDIAG Supply Diagnostics, changed Command from \$C5 to \$C6 on page <a href="#">10</a></li> <li>• Changed <a href="#">High Side Safing Sensor Diagnostic Data Results on page 28</a>.</li> <li>• Updated Outline Drawing to Revision B.</li> </ul>
5.0	11/2011	<ul style="list-style-type: none"> <li>• Removed MCZ33797EK/R2 from the ordering information and added MC33797BPEW/R2</li> <li>• Updated the Static and Dynamic Electrical Characteristics Table (min and max ratings) for MC33797BPEW.</li> </ul>
6.0	2/2014	<ul style="list-style-type: none"> <li>• No technical changes. Revised back page. Updated document properties. Added SMARTMOS sentence to last paragraph.</li> </ul>

**How to Reach Us:**

**Home Page:**  
[freescale.com](http://freescale.com)

**Web Support:**  
[freescale.com/support](http://freescale.com/support)

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: [freescale.com/SalesTermsandConditions](http://freescale.com/SalesTermsandConditions).

Freescale and the Freescale logo are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off.SMARTMOS is a trademark of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© 2014 Freescale Semiconductor, Inc.

Document Number: MC33797  
Rev 6.0  
2/2014