

RMPA5251

4.90-5.85 GHz InGaP HBT Linear Power Amplifier

General Description

The RMPA5251 power amplifier is designed for high performance WLAN applications in the 4.9 to 5.35 and 5.15 to 5.85 GHz frequency bands. The low profile 16 pin 3 x 3 x 0.9 mm package with internal matching on both input and output to 50Ω minimizes next level PCB space and allows for simplified integration. The on-chip detector provides power sensing capability while the logic control provides power saving shutdown options. The PA's low power consumption and excellent linearity are achieved using our InGaP Heterojunction Bipolar Transistor (HBT) technology.

Features

- 4.9 to 5.85 GHz Operation
- 27dB small signal gain
- 26dBm output power @ 1dB compression

- 2.5% EVM at 18.0dBm modulated power out
- 3.3V single positive supply operation
- · Adjustable bias current operation
- · Two power saving shutdown options (bias and logic control)
- Integrated power detector with >18dB dynamic range
- Low profile 16 pin 3 x 3 x 0.9 mm standard QFN leadless package
- Internally matched to 50Ω
- · Minimal external components
- Optimized for use in IEEE 802.11a WLAN applications



Device

Electrical Characteristics 1,3 802.11a OFDM

Modulation (with 176ms burst time, 100ms idle time) 54Mbps Data Rate, 16.7 MHz Bandwidth

•			, .				
Parameter	Minimum	Typical	Maximum	Minimum	Typical	Maximum	Unit
Frequency ¹⁰	4.90		5.35	5.15		5.85	GHz
Supply Voltage	3.0	3.3	3.6	3.0	3.3	3.6	V
Gain		27			28		dB
Total Current @ 18dBm P _{OUT}		250			240		mA
Total Current @ 19dBm P _{OUT}		260			250		mA
EVM @ 18dBm P _{OUT} ²		2.5			2.5		%
EVM @ 19dBm P _{OUT} ²		3.5			3.5		%
Detector Output @ 19dBm P _{OUT}		450			500		mV
Detector Threshold ⁴		5.0			5.0		dBm
P _{OUT} Spectral Mask Compliance ^{5, 6}		21.0			20.0		dBm

Electrical Characteristics 1 Single Tone

Parameter	Minimum	Typical	Maximum	Minimum	Typical	Maximum	Unit
Frequency ¹⁰	4.90		5.35	5.15		5.85	GHz
Supply Voltage	3.0	3.3	3.6	3.0	3.3	3.6	V
Gain ⁷		27			27.5		dB
Total Quiescent Current ^{7, 11}		140–220			140–220		mA

Notes:

- 1. VC1, VC2, VC3, VM1, VM2, VM3 = 3.3 Volts, Tc=25°C, PA is constantly biased, 50Ω system.
- 2. Percentage includes system noise floor of EVM=0.8%.
- 3. Not measured 100% in production.
- Nour measured at P_{IN} corresponding to power detection threshold.
 Measured at P_{IN} at which Spectral Mask Compliance is satisfied. Two-sample windowing length applied.
- 6. P_{IN} is adjusted to point where performance approaches spectral mask requirements.
- 7. 100% Production screened.
- 8. Bias Current is included in the total quiescent current.
- 9. VL is set to logic level for device off operation.
- 10. See Application information on Page 3.
- 11. See Data on Page 8.

Electrical Characteristics 12 Single Tone (Continued)

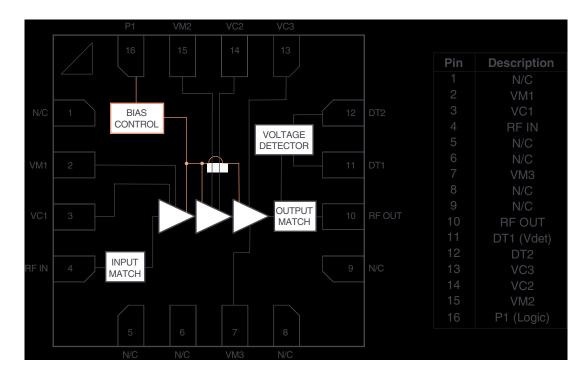
Parameter	Minimum	Typical	Maximum	Minimum	Typical	Maximum	Unit
Bias Current at pin VM ⁸		16			16		mA
P1dB Compression ⁷		26			26		dBm
Current @ P1dB Comp ⁷		425			425		mA
Standby Current ⁹		1.9			1.9		mA
Shutdown Current (VM=0V)		<1.0			<1.0		μΑ
Input Return Loss		12			16		dB
Output Return Loss		10			10		dB
Detector Output at P1dB Comp		2			2		V
Detector P _{OUT} Threshold ^{3, 4}		7.0			7.0		dBm
Frequency	4.90		5.35	5.15		5.85	GHz
2 nd Harmonic Output at P1dB		-30			-30		dBc
3rd Harmonic Output at P1dB		-35			-35		dBc
Logic Shutdown Control Pin (VL):							
Device Off		0.0	0.8		0.0	0.8	V
Device On	2.0	2.4		2.0	2.4		V
Logic Current		10			100		μΑ
Turn-on Time ¹³		<1			<1		μS
Turn-off Time		<1			<1		μS
Spurious (Stability) ¹⁴		-65			-65		dBc

Absolute Ratings¹⁵

Symbol	Parameter	Value	Units
VC1, VC2	Positive Supply Voltage	4.0	V
IC1-IC3	Supply Current		
	IC1	50	mA
	IC2	150	mA
	IC3	500	mA
VM	Voltage Mirror	4	V
V_L	Logic Voltage	5	V
P _{IN}	RF Input Power	10	dBm
T _{CASE}	Case Operating Temperature	-40 to +85	°C
T _{STG}	Storage Temperature	-55 to +150	°C

- Notes:
 3. Not measured 100% in production.
 4. P_{OUT} measured at P_{IN} corresponding to power detection threshold.
 5. Measured at P_{IN} at which Spectral Mask Compliance is satisfied. Two-sample windowing length applied.
 6. P_{IN} is adjusted to point where performance approaches spectral mask requirements.
 7. 100% Production screened.
 8. Bias Current is included in the total quiescent current.
 9. VL is set to logic level for device off operation.
 10. See Application information on Page 3.
 11. See Data on Page 8.
 12. VC1, VC2, VC3, VM1, VM2, VM3 = 3.3 Volts, Tc=25°C, PA is constantly biased, 50€∂ system
 13. Measured from Device On signal turn on, (Logic High) to the point where RF POUT stabilizes to 0.5dB.
 14. Load VSWR is set to 8:1 and the angle is varied 360 degrees. POUT = -30dBm to P1dB.
 15. No permanent damage with only one parameter set at extreme limit. Other parameters set to typical values.

Functional Block Diagram



Application Information

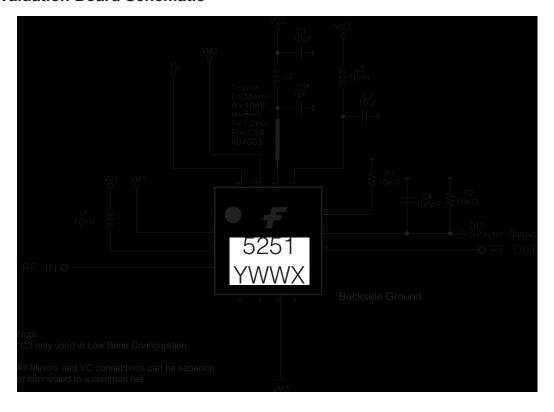
The RMPA5251 can be optimized to work over 2 frequency ranges, 4.9 to 5.35 GHz (Low Band) and 5.15 to 5.85 GHz (High Band).

Using the 2 external component configurations described on the next page, the RMPA5251 can be optimized to give the best EVM, power and gain over a specified bandwidth.

The data on sheets 7-9 shows the performance when the evaluation board is configured for either low or high band performance.

©2004 Fairchild Semiconductor Corporation

Evaluation Board Schematic



Evaluation Board Bill of Materials

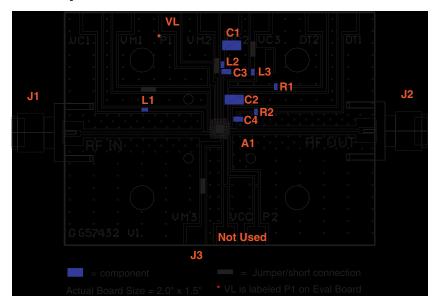
RMPA5251 4.90 to 5.35 GHz Operation Eval Board BOM (Low Band)

No.	Ref	Value	Unit	Qty	Size	Description	MFG	Part No.	Comments
1	C1,C2	10	μF	2	0805	10µF Capacitor	Murata	GRM21BR60J106KE01D	Decoupling Capacitor
2	C3	1	pF	1	0603	1pF Capacitor	Murata	GRM39C0G010B100V	
3	C4	100	pF	1	0402	100pF Capacitor	Murata	GRM1885C1H101JA01D	Detector Capacitor
4	R1,R2	10K	Ω	2	0402	10K Ω Resistor	IMS	RCI-0402-1002J	Detector Resistor
5	L1,L2,L3	10	nH	3	0402	10nH Inductor	Toko	LLV1005FB10NJ	RF Choke
6	B1			1		Fixture Board	Crown Circuits	G657432	
7	J1,J2			2		Jack End Launch SMA	Johnson Components	142-0701-841	
8	J3			11		Right Angle Single Header	Digikey	S1322-12-ND	
9	A1			1		Packaged MMIC	Fairchild	RMPA5251	

RMPA5251 5.15 to 5.8	GHz Operation	Eval Board BOM	(High Band)

No.	Ref	Value	Unit	Qty	Size	Description	MFG	Part No.	Comments
1	C1,C2	10	μF	2	0805	10 μF Capacitor	Murata	GRM21BR60J106K	Decoupling
									Capacitor
2	C4	100	pF	1	0402	100 pF Capacitor	Murata	GRM1885C1H101JA01D	Detector
									Capacitor
3	R1,R2	10K	Ω	2	0402	10 KΩ Resistor	IMS	RCI-0402-1002J	Detector Resistor
4	L1,L3	10	nΗ	2	0402	10 nH Inductor	Toko	LLV1005FB10NJ	RF Choke
5	L2	15	nΗ	1	0402	15 nH Inductor	Toko	LLV1005FB15NJ	RF Choke
6	B1			1		Fixture Board	Crown Circuits	G657432	
7	J1,J2			2		Jack End Launch	Johnson	142-0701-841	
						SMA	Components		
8	J3			11		Right Angle Single	Digikey	S1322-12-ND	
						Header			
9	A1			1		Packaged MMIC	Fairchild	RMPA5251	

Evaluation Board Layout



Evaluation Board Operation

Recommended turn-on sequence:

- 1) Connect RF ports J1, J2 to RF test equipment.
- 2) Connect common ground terminal to the Ground (GND) pin on the board.
- 3) Connect logic control pin VL to positive supply.
- 4) Connect terminals VC1, VC2 and VC3 together and connect to positive supply (VC).
- 5) Connect terminals VM1, VM2 and VM3 together and connect to positive supply (VM).
- 6) Connect voltmeter to Detector Output, pin DT1.
- 7) Connect pin DT2 to ground.
- 8) Apply high voltage of +2.4V to logic control pin VL. (On)
- 9) Apply positive voltage of 3.3V to VC1, VC2 and VC3 (first, second and third stage collector).
- 10) Apply positive voltage of 3.3V to VM1, VM2 and VM3 (bias networks)².
- 11) At this point, you should expect to observe the following positive currents flowing into the pins:

Pin	Current
VL	~150 µA
VC (Total)	~184 mA
VM (Total)	~16 mA

- 12) Apply input RF power to SMA connector pin RF IN. Currents on collector pins will vary depending on the input drive level.
- 13) Vary positive voltage VL from +2.4V to +0.5V to shut down the amplifier or alter the power level.

Shut down current flow into the pins:

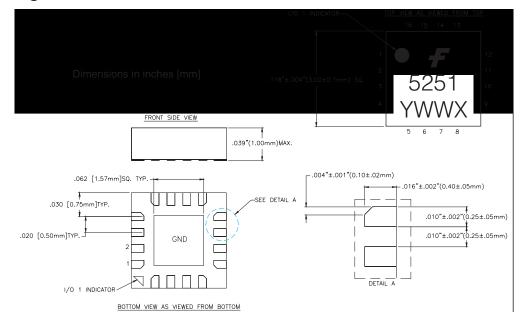
Pin Current ٧L <1 nA VC (total) <1 nA VM (total) <1.9 mA

Recommended turn-off sequence:

Use reverse order described in the turn-on sequence above.

- 1. Turn on sequence is not critical and it is not necessary to sequence power supplies in actual system level design.
 2. VM may be adjusted from +2.9 to +3.3V to adjust bias current operation. See Typical Characteristics.

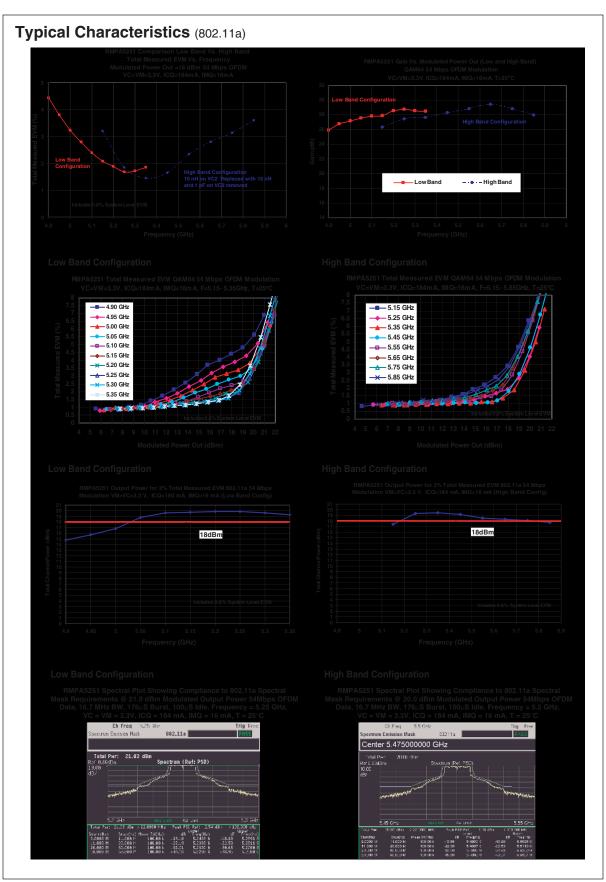
Package Outline



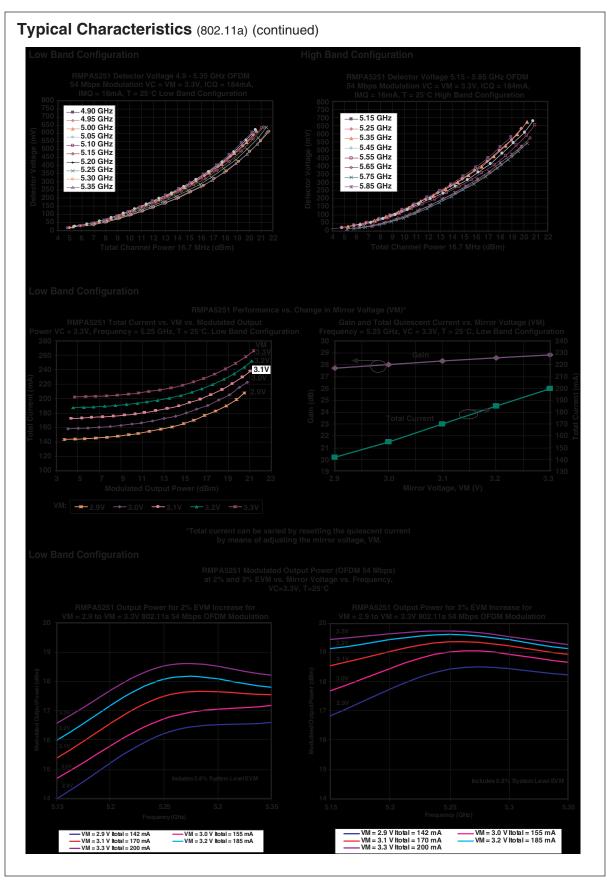
Application Information

Precautions to Avoid Permanent Device Damage:

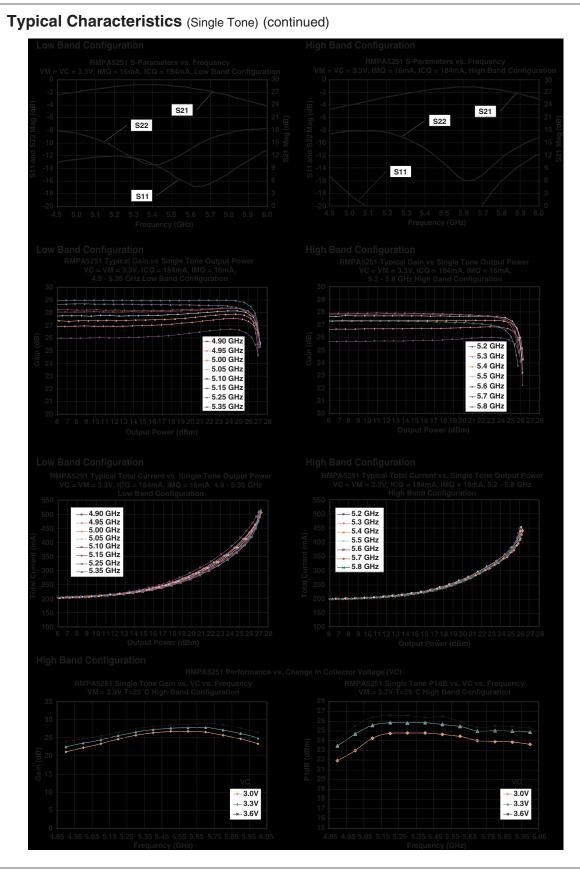
- -Static Sensitivity: Follow ESD precautions to protect against ESD damage:
- A properly grounded static-dissipative surface on which to place devices.
- Static-dissipative floor or mat.
- A properly grounded conductive wrist strap for each person to wear while handling devices.



©2004 Fairchild Semiconductor Corporation RMPA5251 Rev. D



©2004 Fairchild Semiconductor Corporation RMPA5251 Rev. D



©2004 Fairchild Semiconductor Corporation RMPA5251 Rev. D

