Features

- PowerPC™ 405 32-bit RISC processor core operating up to 200 MHz
- PC-100 Synchronous DRAM (SDRAM) interface operating up to 100 MHz
  - 32-bit interface for non-ECC applications
  - 40-bit interface serves 32 bits of data plus 8 check bits for ECC applications
- External Peripheral Bus
  - Flash ROM/Boot ROM interface
  - Direct support for 8-, 16-, or 32-bit SRAM and external peripherals
  - Up to eight devices
  - External Mastering supported
- DMA support for external peripherals, internal UART and memory
  - Scatter-gather chaining supported.
  - Four channels
- PCI Revision 2.2 Compliant Interface (32-bit, up to 66 MHz).
  - PCI Bus interface may be configured to operate synchronously or asynchronously to the chip input clock
  - Internal PCI Bus Arbiter which may be disabled for use with an external arbiter
- Ethernet 10/100 Mbps (full-duplex) support
  - Medium Independent Interface (MII)
- Programmable Interrupt Controller supports interrupts from a variety of sources
  - Supports 7 external and 19 internal interrupts
  - Edge triggered or level-sensitive
  - Positive or negative active
  - Non-critical or critical interrupt to 405 processor core
  - Programmable critical interrupt priority ordering
  - Programmable critical interrupt vector for faster vector processing
- Programmable Timers
- Two serial ports (16550 compatible UART)
- One IIC (I^2C) interface
- General Purpose I/O (GPIO) available
- Supports JTAG for board level testing
- Internal Processor Local Bus (PLB) runs at SDRAM interface frequency
- Supports PowerPC processor boot from PCI memory

Description

Designed specifically to address embedded applications, the 405GP provides a high-performance, low-power solution that interfaces to a wide range of peripherals by incorporating on-chip power management features and intrinsically lower power dissipation requirements.

This chip contains a high-performance RISC processor core, SDRAM controller, PCI bus interface, Ethernet interface, control for external ROM and peripherals, DMA with scatter-gather support, serial ports, IIC interface, and general purpose I/O.

Technology: IBM CMOS SA12E 0.25 µm (0.18 µm L_{eff})

Package: 35 mm, 456-ball enhanced plastic ball grid array (E-PBGA)

Power (estimated): Typical 1.2 W
Maximum 2.0 W

Contents

Figures

Tables

Ordering Information

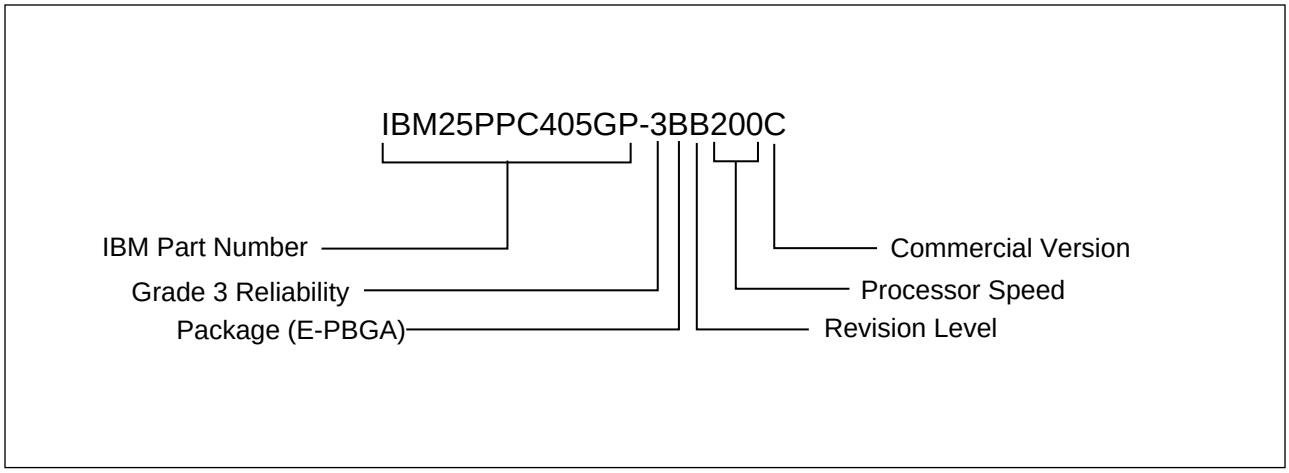
Product Name	OEMLS Part Number	Processor Frequency	Package	Rev Level
PPC405GP	IBM25PPC405GP-3BB200C	200MHz	35mm 456 E-PBGA	B

This section provides the part numbering nomenclature for the PPC405GP. For availability, contact your local IBM sales office.

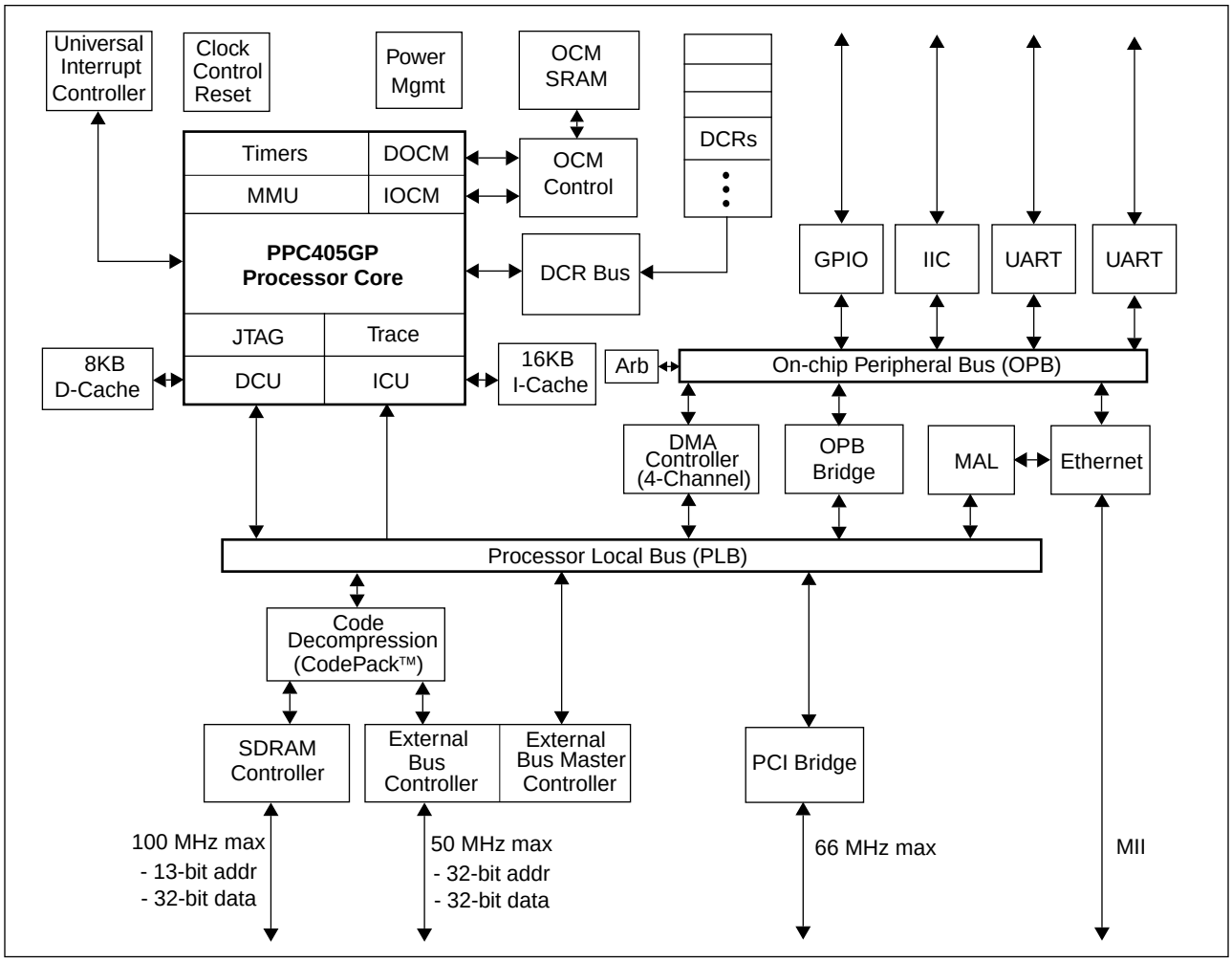
The part number contains a part modifier. This modifier provides for identification of future enhancements (for example, higher performance).

Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

IBM Part Number Key



PPC405GP Embedded Controller Functional Block Diagram



The 405GP is designed using the IBM Microelectronics Blue Logic™ methodology in which major functional blocks are integrated together to create an application-specific ASIC product. This approach provides a consistent way to create complex ASICs using IBM CoreConnect™ Bus Architecture.

Note: IBM CoreConnect busses provide:

- 64-bit PLB interfaces up to 100MHz
- 32-bit On-chip Peripheral Bus (OPB) interfaces up to 50MHz

Address Map Support

The 405GP incorporates two simple and separate address maps. The first is a fixed processor address map that serves the PowerPC family of processors. This address map defines the possible contents of various address regions which the processor may access. The second address map is for Device Configuration Registers (DCR). This address map is accessed by software running on the 405GP processor through the use of MTDCR and MFDCR commands.

SysMem Memory Address Map 4GB System Memory

Function	Sub Function	Start Address	End Address	Size
Local Memory/Peripherals[1]		0000 0000	7FFF FFFF	2GB
PCI Core Space		8000 0000	EF5F FFFF	2GB - 258MB
	PCI Memory	8000 0000	E7FF FFFF	1.66GB
	PCI I/O	E800 0000	E800 FFFF	64kB
	Reserved	E801 0000	E87F FFFF	
	PCI I/O	E880 0000	EBFF FFFF	56MB
	Reserved	EC00 0000	EEBF FFFF	
	PCI Configuration Registers	EEC0 0000	EEC0 0007	8B
	Reserved	EEC0 0008	EECF FFFF	
	PCI Interrupt Acknowledge	EED0 0000	EEDF FFFF	1MB
	Reserved	EEE0 0000	EF3F FFFF	
	PCI local Configuration Registers	EF40 0000	EF40 003F	64B
	Reserved	EF40 003D	EF5F FFFF	
Internal Peripherals		EF60 0000	EFFF FFFF	10MB
	UART0	EF60 0300	EF60 0307	8B
	Reserved			248B
	UART1	EF60 0400	EF60 0407	8B
	Reserved			248B
	IIC0	EF60 0500	EF60 051F	32B
	Reserved			224B
	OPB Arbiter	EF60 0600	EF60 063F	64B
	Reserved			192B
	GPIO Controller Registers	EF60 0700	EF60 077F	128B
	Reserved			128B
	Ethernet Controller Registers	EF60 0800	EF60 08FF	256B
	Reserved			9.75MB
Expansion ROM[2]		F000 0000	FFDF FFFF	254MB
Boot ROM[2, 3]		FFE0 0000	FFFF FFFF	2MB

1. The Local Memory/Peripheral area of the memory map may be configured for SDRAM, ROM or Peripherals.
2. The Boot ROM and Expansion ROM area of the memory map are intended for use by ROM or Flash-type devices. While locating volatile SDRAM and SRAM in this region is supported by the controller it is not recommended that these regions be used for this purpose.
3. When the optional boot from PCI Memory is selected, the PCI Boot ROM address space begins at FFFE 0000 (size is 128KB).

DCR Address Map 4KB Device Configuration Register

Function	Base Address Strap/Parameter	Start Address(0:9)	End Address(0:9)	Size
DCR Address Space		000	3FF	1KW (4KB)[1]
Reserved		000	010	16W
Memory Controller Registers	[0:8] = 00 0001 000	010	011	2W
External Bus Controller Registers	[0:8] = 00 0001 001	012	013	2W
Decompression Controller Registers	[0:8] = 00 0001 010	014	015	2W
Reserved		016	017	2W
On-Chip Memory Controller Registers	[0:8] = 00 0001 011	018	01F	8W
Reserved		020	07F	96W
PLB Registers	[0:5] = 00 0100	080	08F	16W
Reserved		090	09F	16W
OPB Bridge Out Registers	[0:6] = 00 0110 0	0A0	0A7	8W
Reserved		0A8	0AF	8W
Clock, Control and Reset	parm=10'h0B0	0B0	0B7	8W
Power Management	parm=10'h0B8	0B8	0BF	8W
Interrupt Controller	parm=10'h0C0	0C0	0CF	16W
Reserved		0D0	0FF	48W
DMA Controller Registers	[0:3] = 01 00	100	13F	64W
Reserved		140	17F	64W
Ethernet MAL Registers	[0:2] = 01 1	180	1FF	128W
Reserved		200	3FF	512W

1. DCR address space is addressable with up to 10 bits (1024 or 1K unique addresses). Each unique address represents a single 32-bit (word) register, or 1 kiloword (KW) (which equals 4 KB).

PLB to PCI Interface

The PLB to PCI interface core provides a mechanism for connecting PCI devices to the local PowerPC processor and local memory. This interface is compliant with version 2.2 of the PCI Specification.

Features include:

- Internal PCI bus arbiter for up to six external devices at PCI bus speeds up to 66MHz. Internal arbiter use is optional and may be disabled for systems which employ an external arbiter.
- PLB 3.0 Compliant
- PLB bus frequency up to 100MHz
- 64-bit PLB Master
- 32-bit PLB Slave
- PCI bus frequency up to 66MHz
  - Synchronous operation at 1/n fractions of PLB speed (n = 1 to 4) to 33MHz maximum
  - Asynchronous operation from 1/8 PLB frequency to 66MHz maximum
- 32-bit PCI Address/Data Bus
- Power Management:
  - PCI Bus Power Management v1.1 compliant
- Supports 1:1, 2:1, 3:1, 4:1 clock ratios from PLB to PCI
- Buffering between PLB and PCI:
  - PCI Target 64-byte write post buffer
  - PCI Target 96-byte read prefetch buffer
  - PLB Slave 8-byte write post buffer
  - PLB Slave 64-byte read prefetch buffer
- Error tracking/status
- Supports PCI Target side configuration
- Supports processor access to all PCI address spaces:
  - Single-byte PCI I/O reads and writes
  - PCI memory single-beat and prefetch-burst reads and single-beat writes
  - Single-byte PCI configuration reads and writes (type 0 and type 1)
  - PCI interrupt acknowledge
  - PCI special cycle

- Supports PCI target access to all PLB address spaces
- Supports PowerPC processor boot from PCI memory

SDRAM Memory Controller

The PPC405GP Memory Controller core provides a low latency access path to SDRAM memory. A variety of system memory configurations are supported. The memory controller supports up to four logical banks. Up to 256MB per bank are supported, up to a maximum of 1GB. Memory timings, address and bank sizes, and memory addressing modes are programmable.

Features include:

- 11x8 to 13x11 addressing for SDRAM (2- and 4-bank)
- Memory bus operates at same frequency as PLB
- 32-bit memory interface support
- Programmable address compare for each bank of memory
  - 4GB address space
- Industry standard 168-pin DIMMS are supported (some configurations)
- Up to 100MHz Memory, includes PC100 support
- 4MB to 256MB per bank
- Programmable address mapping and timing
- Auto refresh
- Page Mode Accesses with up to 4 open pages
- Sync DRAM configuration via mode set command
- Power Management (self-refresh)
- Error Checking and Correction (ECC) support
  - Standard SEC/DED coverage
  - Aligned nibble error detect
  - Address error logging
  - Mixed ECC/non-ECC banks
  - Bypass mode

External Peripheral Bus Controller (EBC)

Features include:

- Up to eight ROM, EPROM, SRAM, Flash, and Slave Peripheral I/O banks supported

- Up to 50 MHz operation
- Burst and non-burst devices
- 8-, 16-, 32-bit byte-addressable data bus width support
- Latch data on Ready, Synchronous or Asynchronous
- Programmable 2K clock time-out counter with disable for Ready
- Programmable access timing per device
  - 256 Wait States for non-burst
  - 32 Burst Wait States for first access and up to 8 Wait States for subsequent accesses
  - Programmable CSon, CSoff relative to address
  - Programmable OEon, WEon, WEoff (1 to 4 clockcycles) relative to CS.
- Programmable address mapping
- Peripheral Device pacing with external “Ready”
- External master interface
  - Write posting from external master
  - Read prefetching on PLB for external master reads
  - Bursting capable from external master
  - Allows external master access to all non-EBC PLB slaves
  - External master may control EBC slaves for own access and control

DMA Controller

Features include:

- Supports the following transfers:
  - Memory-to-memory transfers
  - Buffered peripheral to memory transfers
  - Buffered memory to peripheral transfers
- Four channels
- Scatter/Gather capability for programming multiple DMA operations
- 8-, 16-, 32-bit peripheral support (OPB and external)
- 32-bit addressing
- Address increment or decrement

- Internal 32-byte data buffering capability
- Supports internal and external peripherals
- Support for memory mapped peripherals
- Support for peripherals running on slower frequency buses

UART

Features include:

- One 8-pin UART and one 4-pin UART interface provided
- Selectable internal or external serial clock to allow wide range of baud rates
- Register compatibility with NS16550 register set
- Complete status reporting capability
- Transmitter and receiver are each buffered with16-byte FIFOs when in FIFO mode
- Fully programmable serial-interface characteristics
- Support DMA using internal DMA engine

IIC Bus Interface

Features include:

- Compliant with Philips® Semiconductors I^2C Specification, dated 1995
- 100 kHz or 400 kHz operation
- 8-bit data
- 10- or 7-bit address
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters
- Supports fixed V_{DD} IIC interface
- Two independent 4 x 1 byte data buffers
- Twelve memory-mapped, fully programmable configuration registers
- One programmable interrupt request signal
- Provides full management of all IIC bus protocol
- Programmable error recovery

General Purpose (GPIO) IO Controller

Features include:

- Controller functions and GPIO registers are programmed and accessed via memory-mapped OPB bus master accesses
- All GPIOs are pin-shared with other functions. DCRs control whether a particular pin that has GPIO capabilities acts as a GPIO or is used for another purpose. Twenty-three GPIOs are multiplexed with:
  - 7 of 8 chip selects
  - All seven external interrupts
  - All nine instruction trace pins
- Each GPIO output is separately programmable to emulate an open drain driver (i.e., drives to zero, three-stated if output bit is 1)

Universal Interrupt Controller (UIC)

The Universal Interrupt Controller (UIC) provides the control, status, and communications necessary between the various sources of interrupts and the local PowerPC processor.

Features include:

- Supports 7 external and 19 internal interrupts
- Edge triggered or level-sensitive
- Positive or negative active
- Non-critical or critical interrupt to 405 processor core
- Programmable critical interrupt priority ordering
- Programmable critical interrupt vector for faster vector processing

10/100 Mbps Ethernet MAC

Features include:

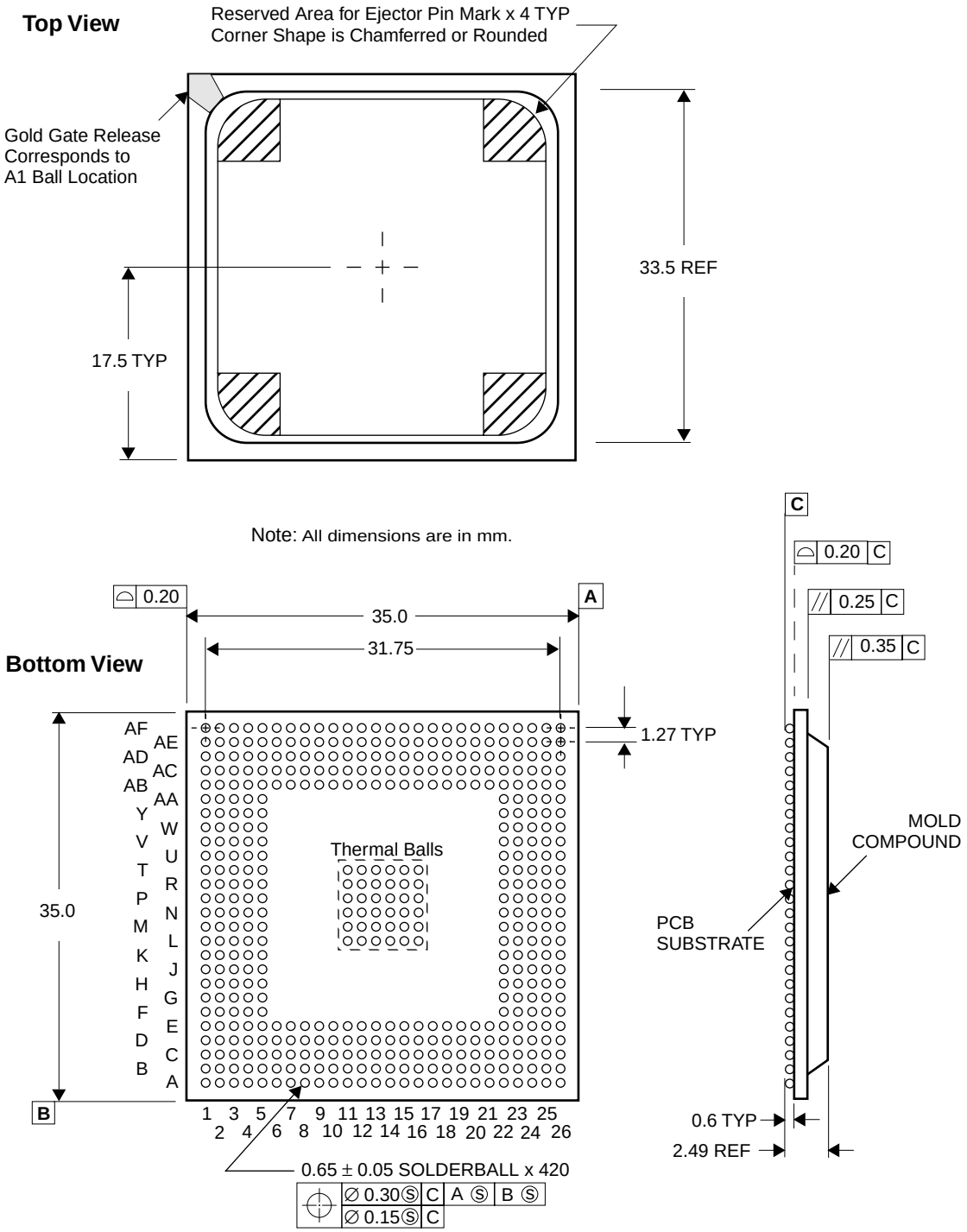
- Capable of handling full/half duplex 100 Mbps and 10 Mbps operation
- Uses the Medium Independent Interface (MII) to the physical layer (PHY not included on chip)

JTAG

Features include:

- IEEE 1149.1 Test Access Port
- IBM RISCWatch Debugger support
- JTAG Boundary Scan Description Language (BSDL)

35mm 456-Ball E-PBGA Package



Signals Listed Alphabetically

Signal Name	Ball	Interface Group	Page
BA0 BA1	AB24 AC24	SDRAM Interface	27
$\overline{\text{BankSel0}}$ $\overline{\text{BankSel1}}$ $\overline{\text{BankSel2}}$ $\overline{\text{BankSel3}}$	AD17 AF17 AE15 AC14	SDRAM Interface	27
BusReq	R3	External MASTER Peripheral Interface	31
$\overline{\text{CAS}}$	AB23	SDRAM Interface	27
ClkEn0 ClkEn1	AB25 AC25	SDRAM Interface	27
DMAAck0 DMAAck1 DMAAck2 DMAAck3	D16 B15 B14 C12	External SLAVE Peripheral Interface	28
DMAReq0 DMAReq1 DMAReq2 DMAReq3	C16 D14 C11 A7	External SLAVE Peripheral Interface	28
DQM0 DQM1 DQM2 DQM3	AC12 AC10 AC6 AA3	SDRAM Interface	27
DQMCB	AC15	SDRAM Interface	27
DrvrInh1 DrvrInh2	E24 E23	System Interface	33
ECC0 ECC1 ECC2 ECC3 ECC4 ECC5 ECC6 ECC7	AE14 AF15 AF14 AD13 AF13 AF12 AE13 AD12	SDRAM Interface	27
EMCMDClk	H24	Ethernet Interface	26
EOT0[TC0] EOT1[TC1] EOT2[TC2] EOT3[TC3]	F3 G2 V2 Y1	External SLAVE Peripheral Interface	28
EMCMDIO[PHYMDIO]	AD26	Ethernet Interface	26
EMCTxD0 EMCTxD1 EMCTxD2 EMCTxD3	J26 L25 L24 P25	Ethernet Interface	26
EMCTxEn	K23	Ethernet Interface	26
EMCTxErr	K25	Ethernet Interface	26
$\overline{\text{ExtAck}}$	Y3	External MASTER Peripheral Interface	31
$\overline{\text{ExtReq}}$	Y4	External MASTER Peripheral Interface	31
$\overline{\text{ExtReset}}$	T3	External MASTER Peripheral Interface	31

Signals Listed Alphabetically

Signal Name	Ball	Interface Group	Page
GPIO1[TS1E] GPIO2[TS2E] GPIO3[TS1O] GPIO4[TS2O] GPIO5[TS3] GPIO6[TS4] GPIO7[TS5] GPIO8[TS6] GPIO9[TrcClk]	D18 C20 A22 AF18 AC9 AE8 AF5 AC7 AB3	System Interface	33
$\overline{\text{Halt}}$	AB26	System Interface	33
HoldAck	U2	External MASTER Peripheral Interface	31
HoldPri	T2	External MASTER Peripheral Interface	31
HoldReq	V1	External MASTER Peripheral Interface	31
IICSCL	AD6	Internal Peripheral Interface	31
IICSDA	AE7	Internal Peripheral Interface	31
IRQ0[GPIO17] IRQ1[GPIO18] IRQ2[GPIO19] IRQ3[GPIO20] IRQ4[GPIO21] IRQ5[GPIO22] IRQ6[GPIO23]	V25 V23 W24 W25 Y24 Y25 AA24	Interrupts Interface	32
MemAddr0 MemAddr1 MemAddr2 MemAddr3 MemAddr4 MemAddr5 MemAddr6 MemAddr7 MemAddr8 MemAddr9 MemAddr10 MemAddr11 MemAddr12	AE22 AC21 AE21 AD21 AF22 AE20 AC19 AE19 AD19 AC18 AF19 AD18 AC17	SDRAM Interface	27
MemClkOut0 MemClkOut1	AC26 AA23	SDRAM Interface	27

Signals Listed Alphabetically

Signal Name	Ball	Interface Group	Page
MemData0	AC13	SDRAM Interface	27
MemData1	AE12		
MemData2	AD11		
MemData3	AC11		
MemData4	AF10		
MemData5	AE11		
MemData6	AD10		
MemData7	AF9		
MemData8	AD9		
MemData9	AE9		
MemData10	AD8		
MemData11	AF7		
MemData12	AC8		
MemData13	AD7		
MemData14	AE6		
MemData15	AE5		
MemData16	AE4		
MemData17	AD5		
MemData18	AD4		
MemData19	AC5		
MemData20	AD1		
MemData21	AB2		
MemData22	AA4		
MemData23	AA2		
MemData24	AB1		
MemData25	Y2		
MemData26	W4		
MemData27	W2		
MemData28	W3		
MemData29	V4		
MemData30	W1		
MemData31	V3		
PCIAD0	A17	PCI Interface	24
PCIAD1	B16		
PCIAD2	C17		
PCIAD3	A18		
PCIAD4	D17		
PCIAD5	C18		
PCIAD6	B18		
PCIAD7	A20		
PCIAD8	B21		
PCIAD9	A23		
PCIAD10	D21		
PCIAD11	B22		
PCIAD12	B23		
PCIAD13	C22		
PCIAD14	C26		
PCIAD15	F25		
PCIAD16	K26		
PCIAD17	L23		
PCIAD18	M25		
PCIAD19	M23		
PCIAD20	N25		
PCIAD21	M26		
PCIAD22	N26		
PCIAD23	P24		
PCIAD24	R24		
PCIAD25	R23		
PCIAD26	P23		
PCIAD27	R25		
PCIAD28	T24		
PCIAD29	U26		
PCIAD30	T25		
PCIAD31	V26		

Signals Listed Alphabetically

Signal Name	Ball	Interface Group	Page
PCIC0[$\overline{BE0}$] PCIC1[$\overline{BE1}$] PCIC2[$\overline{BE2}$] PCIC3[BE3	D19 F24 K24 R26	PCI Interface	24
PCIClk	B20	PCI Interface	24
$\overline{PCIDevSel}$	H25	PCI Interface	24
PCIIDSel	P26	PCI Interface	24
$\overline{PCIFrame}$	J24	PCI Interface	24
$\overline{PCIGnt0}$[$\overline{Req}$] $\overline{PCIGnt1}$ $\overline{PCIGnt2}$ $\overline{PCIGnt3}$ $\overline{PCIGnt4}$ $\overline{PCIGnt5}$	U23 T23 F23 H26 N23 M24	PCI Interface	24
$\overline{PCIINT}$[$\overline{PerWE}$]	C23	PCI Interface	24
$\overline{PCIIRDY}$	J23	PCI Interface	24
PCIParity	E26	PCI Interface	24
$\overline{PCIPErr}$	G25	PCI Interface	24
$\overline{PCIReq0}$[$\overline{Gnt}$] PCIReq1 $\overline{PCIReq2}$ $\overline{PCIReq3}$ $\overline{PCIReq4}$ $\overline{PCIReq5}$	C19 C21 B19 A24 G23 J25	PCI Interface	24
$\overline{PCIReset}$	B24	PCI Interface	24
$\overline{PCISErr}$	G24	PCI Interface	24
$\overline{PCIStop}$	H23	PCI Interface	24
$\overline{PCITRDY}$	G26	PCI Interface	24

Signals Listed Alphabetically

Signal Name	Ball	Interface Group	Page
PerAddr0 PerAddr1 PerAddr2 PerAddr3 PerAddr4 PerAddr5 PerAddr6 PerAddr7 PerAddr8 PerAddr9 PerAddr10 PerAddr11 PerAddr12 PerAddr13 PerAddr14 PerAddr15 PerAddr16 PerAddr17 PerAddr18 PerAddr19 PerAddr20 PerAddr21 PerAddr22 PerAddr23 PerAddr24 PerAddr25 PerAddr26 PerAddr27 PerAddr28 PerAddr29 PerAddr30 PerAddr31	D5 A3 B4 B5 D6 B6 C6 D7 A5 B7 C7 D8 B8 C8 D9 A8 C9 D10 C10 A10 D11 B12 D13 D12 B13 A12 A13 C14 A14 A15 C15 D15	External SLAVE Peripheral Interface	28
$\overline{\text{PerBLast}}$	F2	External SLAVE Peripheral Interface	28
PerClk	E4	External MASTER Peripheral Interface	31
$\overline{\text{PerCS0}}$ $\overline{\text{PerCS1}}$[GPIO10] $\overline{\text{PerCS2}}$[GPIO11] $\overline{\text{PerCS3}}$[GPIO12] $\overline{\text{PerCS4}}$[GPIO13] $\overline{\text{PerCS5}}$[GPIO14] $\overline{\text{PerCS6}}$[GPIO15] $\overline{\text{PerCS7}}$[GPIO16]	B3 C4 C5 A4 B9 B10 A9 B11	External SLAVE Peripheral Interface	28

Signals Listed Alphabetically

Signal Name	Ball	Interface Group	Page
PerData0 PerData1 PerData2 PerData3 PerData4 PerData5 PerData6 PerData7 PerData8 PerData9 PerData10 PerData11 PerData12 PerData13 PerData14 PerData15 PerData16 PerData17 PerData18 PerData19 PerData20 PerData21 PerData22 PerData23 PerData24 PerData25 PerData26 PerData27 PerData28 PerData29 PerData30 PerData31	U4 U3 U1 T4 R2 P4 R4 P2 R1 P1 N3 N1 M1 N2 M3 M4 N4 M2 L3 L4 K1 L2 K3 J1 K4 J3 J2 J4 H3 G1 H2 H4	External SLAVE Peripheral Interface	28
PerErr	B1	External MASTER Peripheral Interface	31
$\overline{\text{PerOE}}$	C2	External SLAVE Peripheral Interface	28
PerPar0 PerPar1 PerPar2 PerPar3	D3 G4 G3 E1	External SLAVE Peripheral Interface	28
PerReady	E3	External SLAVE Peripheral Interface	28
PerR/$\overline{\text{W}}$	C1	External SLAVE Peripheral Interface	28
$\overline{\text{PerWBE0}}$ $\overline{\text{PerWBE1}}$ $\overline{\text{PerWBE2}}$ $\overline{\text{PerWBE3}}$	D2 E2 F4 D1	External SLAVE Peripheral Interface	28
PHYCol	AA25	Ethernet Interface	26
PHYRxClk	AF20	Ethernet Interface	26
PHYCrS	W23	Ethernet Interface	26
PHYRxD0 PHYRxD1 PHYRxD2 PHYRxD3	AE23 AF23 AC20 AD20	Ethernet Interface	26
PHYRxDV	V24	Ethernet Interface	26
PHYRxErr	U24	Ethernet Interface	26
PHYTxClk	E25	Ethernet Interface	26

Signals Listed Alphabetically

Signal Name	Ball	Interface Group	Page
$\overline{\text{RAS}}$	AF24	SDRAM Interface	27
RcvrInh	C25	System Interface	33
SysClk	A25	System Interface	33
SysErr	AD25	System Interface	33
$\overline{\text{SysReset}}$	D22	System Interface	33
TCK	AD22	JTAG Interface	32
TDI	AE24	JTAG Interface	32
TDO	AD23	JTAG Interface	32
TestEn	D26	System Interface	33
TmrClk	D24	System Interface	33
TMS	AC22	JTAG Interface	32
$\overline{\text{TRST}}$	AE26	JTAG Interface	32
$\overline{\text{UART0\_CTS}}$	AB4	Internal Peripheral Interface	31
$\overline{\text{UART0\_DCD}}$	AE18	Internal Peripheral Interface	31
$\overline{\text{UART0\_DSR}}$	AE3	Internal Peripheral Interface	31
$\overline{\text{UART0\_DTR}}$	AF2	Internal Peripheral Interface	31
$\overline{\text{UART0\_RI}}$	AD15	Internal Peripheral Interface	31
$\overline{\text{UART0\_RTS}}$	AD16	Internal Peripheral Interface	31
UART0_Rx	AE16	Internal Peripheral Interface	31
UART0_Tx	AF3	Internal Peripheral Interface	31
$\overline{\text{UART1\_DSR}}$[$\overline{\text{UART1\_CTS}}$]	AC3	Internal Peripheral Interface	31
$\overline{\text{UART1 \_RTS}}$[$\overline{\text{UART1\_DTR}}$]	AD2	Internal Peripheral Interface	31
UART1_Rx	AC1	Internal Peripheral Interface	31
UART1_Tx	AC2	Internal Peripheral Interface	31
UARTSerClk	AE17	Internal Peripheral Interface	31
$\overline{\text{WE}}$	AC16	SDRAM Interface	27

Signals Listed by Ball Assignment

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A1	GND	B14	DMAAck2	D1	PerWBE3	E14	GND
A2	GND	B15	DMAAck1	D2	PerWBE0	E15	V_{DD}
A3	PerAddr1	B16	PCIAD1	D3	PerPar0	E16	V_{DD}
A4	PerCS3[GPIO12]	B17	OV_{DD}	D4	GND	E17	V_{DD}
A5	PerAddr8	B18	PCIAD6	D5	PerAddr0	E18	GND
A6	GND	B19	PCIReq2	D6	PerAddr4	E19	OV_{DD}
A7	DMAReq3	B20	PCIClk	D7	PerAddr7	E20	OV_{DD}
A8	PerAddr15	B21	PCIAD8	D8	PerAddr11	E21	OV_{DD}
A9	PerCS6[GPIO15]	B22	PCIAD11	D9	PerAddr14	E22	GND
A10	PerAddr19	B23	PCIAD12	D10	PerAddr17	E23	DrvrInh2
A11	GND	B24	PCIReset	D11	PerAddr20	E24	DrvInh1
A12	PerAddr25	B25	GND	D12	PerAddr23	E25	PHYTxClk
A13	PerAddr26	B26	GND	D13	PerAddr22	E26	PCIParity
A14	PerAddr28	C1	PerR/W	D14	DMAReq1	F1	GND
A15	PerAddr29	C2	PerOE	D15	PerAddr31	F2	PerBLast
A16	GND	C3	GND	D16	DMAAck0	F3	EOT0[TC0]
A17	PCIAD0	C4	PerCS1[GPIO10]	D17	PCIAD4	F4	PerWBE2
A18	PCIAD3	C5	PerCS2[GPIO11]	D18	GPIO1[TS1E]	F5	OV_{DD}
A19	GND	C6	PerAddr6	D19	PCIC0[BE0]	F22	OV_{DD}
A20	PCIAD7	C7	PerAddr10	D20	No Connect	F23	PCIGnt2
A21	GND	C8	PerAddr13	D21	PCIAD10	F24	PCIC1[BE1]
A22	GPIO3[TS1O]	C9	PerAddr16	D22	SysReset	F25	PCIAD15
A23	PCIAD9	C10	PerAddr18	D23	GND	F26	GND
A24	PCIReq3	C11	DMAReq2	D24	TmrClk	G1	PerData29
A25	SysClk	C12	DMAAck3	D25	AV_{DD}	G2	EOT1[TC1]
A26	GND	C13	OV_{DD}	D26	TestEn	G3	PerPar2
B1	PerErr	C14	PerAddr27	E1	PerPar3	G4	PerPar1
B2	GND	C15	PerAddr30	E2	PerWBE1	G5	OV_{DD}
B3	PerCS0	C16	DMAReq0	E3	PerReady	G22	OV_{DD}
B4	PerAddr2	C17	PCIAD2	E4	PerClk	G23	PCIReq4
B5	PerAddr3	C18	PCIAD5	E5	GND	G24	PCISErr
B6	PerAddr5	C19	PCIReq0[Gnt]	E6	OV_{DD}	G25	PCIPErr
B7	PerAddr9	C20	GPIO2[TS2E]	E7	OV_{DD}	G26	PCITRDY
B8	PerAddr12	C21	PCIReq1	E8	OV_{DD}	H1	GND
B9	PerCS4[GPIO13]	C22	PCIAD13	E9	GND	H2	PerData30
B10	PerCS5[GPIO14]	C23	PCIINT[PerWE]	E10	V_{DD}	H3	PerData28
B11	PerCS7[GPIO16]	C24	GND	E11	V_{DD}	H4	PerData31
B12	PerAddr21	C25	RcvInh	E12	V_{DD}	H5	OV_{DD}
B13	PerAddr24	C26	PCIAD14	E13	GND	H22	OV_{DD}

Signals Listed by Ball Assignment

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
H23	PCIStop	M1	PerData12	P14	GND	U1	PerData2
H24	EMCMDClk	M2	PerData17	P15	GND	U2	HoldAck
H25	PCIDevSel	M3	PerData14	P16	GND	U3	PerData1
H26	PCIGnt3	M4	PerData15	P22	GND	U4	PerData0
J1	PerData23	M5	V_{DD}	P23	PCIAD26	U5	V_{DD}
J2	PerData26	M11	GND	P24	PCIAD23	U22	V_{DD}
J3	PerData25	M12	GND	P25	EMCTxD3	U23	PCIGnt0[Req]
J4	PerData27	M13	GND	P26	PCIIDSel	U24	PHYRxErr
J5	GND	M14	GND	R1	PerData8	U25	OV_{DD}
J22	GND	M15	GND	R2	PerData4	U26	PCIAD29
J23	PCIIRDY	M16	GND	R3	BusReq	V1	HoldReq
J24	PCIFrame	M22	V_{DD}	R4	PerData6	V2	EOT2[TC2]
J25	PCIReq5	M23	PCIAD19	R5	V_{DD}	V3	MemData31
J26	EMCTxD0	M24	PCIGnt5	R11	GND	V4	MemData29
K1	PerData20	M25	PCIAD18	R12	GND	V5	GND
K2	OV_{DD}	M26	PCIAD21	R13	GND	V22	GND
K3	PerData22	N1	PerData11	R14	GND	V23	IRQ1[GPIO18]
K4	PerData24	N2	PerData13	R15	GND	V24	PHYRxDV
K5	V_{DD}	N3	PerData10	R16	GND	V25	IRQ0[GPIO17]
K22	V_{DD}	N4	PerData16	R22	V_{DD}	V26	PCIAD31
K23	EMCTxEn	N5	GND	R23	PCIAD25	W1	MemData30
K24	PCIC2[BE2]	N11	GND	R24	PCIAD24	W2	MemData27
K25	EMCTxErr	N12	GND	R25	PCIAD27	W3	MemData28
K26	PCIAD16	N13	GND	R26	PCIC3[BE3]	W4	MemData26
L1	GND	N14	GND	T1	GND	W5	OV_{DD}
L2	PerData21	N15	GND	T2	HoldPri	W22	OV_{DD}
L3	PerData18	N16	GND	T3	ExtReset	W23	PHYCrS
L4	PerData19	N22	GND	T4	PerData3	W24	IRQ2[GPIO19]
L5	V_{DD}	N23	PCIGnt4	T5	V_{DD}	W25	IRQ3[GPIO20]
L11	GND	N24	OV_{DD}	T11	GND	W26	GND
L12	GND	N25	PCIAD20	T12	GND	Y1	EOT3[TC3]
L13	GND	N26	PCIAD22	T13	GND	Y2	MemData25
L14	GND	P1	PerData9	T14	GND	Y3	ExtAck
L15	GND	P2	PerData7	T15	GND	Y4	ExtReq
L16	GND	P3	OV_{DD}	T16	GND	Y5	OV_{DD}
L22	V_{DD}	P4	PerData5	T22	V_{DD}	Y22	OV_{DD}
L23	PCIAD17	P5	GND	T23	PCIGnt1	Y23	No Connect
L24	EMCTxD2	P11	GND	T24	PCIAD28	Y24	IRQ4[GPIO21]
L25	EMCTxD1	P12	GND	T25	PCIAD30	Y25	IRQ5[GPIO22]
L26	GND	P13	GND	T26	GND	Y26	No Connect

Signals Listed by Ball Assignment

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AA1	GND	AB26	$\overline{\text{Halt}}$	AD9	MemData8	AE18	$\overline{\text{UART0\_DCD}}$
AA2	MemData23	AC1	UART1_Rx	AD10	MemData6	AE19	MemAddr7
AA3	DQM3	AC2	UART1_Tx	AD11	MemData2	AE20	MemAddr5
AA4	MemData22	AC3	$\overline{\text{UART1\_DSR}}$ [$\overline{\text{UART1\_CTS}}$]	AD12	ECC7	AE21	MemAddr2
AA5	OV_{DD}	AC4	GND	AD13	ECC3	AE22	MemAddr0
AA22	OV_{DD}	AC5	MemData19	AD14	OV_{DD}	AE23	PHYRxD0
AA23	MemClkOut1	AC6	DQM2	AD15	$\overline{\text{UART0\_RI}}$	AE24	TDI
AA24	IRQ6[GPIO23]	AC7	GPIO8[TS6]	AD16	$\overline{\text{UART0\_RTS}}$	AE25	GND
AA25	PHYCol	AC8	MemData12	AD17	$\overline{\text{BankSel0}}$	AE26	$\overline{\text{TRST}}$
AA26	GND	AC9	GPIO5[TS3]	AD18	MemAddr11	AF1	GND
AB1	MemData24	AC10	DQM1	AD19	MemAddr8	AF2	$\overline{\text{UART0\_DTR}}$
AB2	MemData21	AC11	MemData3	AD20	PHYRxD3	AF3	UART0_Tx
AB3	GPIO9[TrcClk]	AC12	DQM0	AD21	MemAddr3	AF4	Reserved
AB4	$\overline{\text{UART0\_CTS}}$	AC13	MemData0	AD22	TCK	AF5	GPIO7[TS5]
AB5	GND	AC14	$\overline{\text{BankSel3}}$	AD23	TDO	AF6	GND
AB6	OV_{DD}	AC15	DQMCB	AD24	GND	AF7	MemData11
AB7	OV_{DD}	AC16	$\overline{\text{WE}}$	AD25	SysErr	AF8	GND
AB8	OV_{DD}	AC17	MemAddr12	AD26	EMCMDIO [PHYMDIO]	AF9	MemData7
AB9	GND	AC18	MemAddr9	AE1	GND	AF10	MemData4
AB10	V_{DD}	AC19	MemAddr6	AE2	GND	AF11	GND
AB11	V_{DD}	AC20	PHYRxD2	AE3	$\overline{\text{UART0\_DSR}}$	AF12	ECC5
AB12	V_{DD}	AC21	MemAddr1	AE4	MemData16	AF13	ECC4
AB13	GND	AC22	TMS	AE5	MemData15	AF14	ECC2
AB14	GND	AC23	GND	AE6	MemData14	AF15	ECC1
AB15	V_{DD}	AC24	BA1	AE7	IICSDA	AF16	GND
AB16	V_{DD}	AC25	ClkEn1	AE8	GPIO6[TS4]	AF17	$\overline{\text{BankSel1}}$
AB17	V_{DD}	AC26	MemClkOut0	AE9	MemData9	AF18	GPIO4[TS2O]
AB18	GND	AD1	MemData20	AE10	OV_{DD}	AF19	MemAddr10
AB19	OV_{DD}	AD2	$\overline{\text{UART1\_RTS}}$ [$\overline{\text{UART1\_DTR}}$]	AE11	MemData5	AF20	PHYRxClk
AB20	OV_{DD}	AD3	GND	AE12	MemData1	AF21	GND
AB21	OV_{DD}	AD4	MemData18	AE13	ECC6	AF22	MemAddr4
AB22	GND	AD5	MemData17	AE14	ECC0	AF23	PHYRxD1
AB23	$\overline{\text{CAS}}$	AD6	IICSCL	AE15	$\overline{\text{BankSel2}}$	AF24	$\overline{\text{RAS}}$
AB24	BA0	AD7	MemData13	AE16	UART0_Rx	AF25	GND
AB25	ClkEn0	AD8	MemData10	AE17	UARTSerClk	AF26	GND

Pin Lists

The 405GP embedded controller is packaged in a 456-ball enhanced plastic ball grid array (E-PBGA). The following tables describe the package level pinout.

Pin Summary

Block	No. of Signals
PCI	60
Ethernet	18
SDRAM	72
External peripheral	96
External master	9
Internal peripheral	15
Interrupts	7
JTAG	5
System	19
Total signal I/O	**301**
OVDD	32
VDD	24
Gnd	60
Thermal (and Gnd)	36
Reserved	3
Total I/O	**456**

In the following table, each physical pin (ball) is represented in a table row along with a simple description of the pin function. Some signals are multiplexed onto the same pin so that the pin is usable for different functions. Multiplexed signals are shown in square brackets following the default signal (for example, C0:3[$\overline{\text{BE0:3}}$]) and described consecutively within each pin functional description. Active-low signals such as $\overline{\text{BE0:3}}$ are marked with a black overline.

It is expected that in any single application a particular pin will always be programmed to serve the same function. The flexibility of multiplexing allows a single chip to offer a richer pin selection than would otherwise be possible.

In addition to multiplexing, many pins are also multi-purpose. These pins are described in the table using a single row with a text description that indicates the different functional uses of the pin. For example, the EBC peripheral controller address pins are used as outputs by the 405GP to broadcast an address to external slave devices when the 405GP has control of the external bus. When during the course of normal chip operation an external master gains ownership of the external bus, these same pins are used as inputs which are driven by the external master and received by the EBC in the 405GP.

One group of pins is used as strapped inputs during system reset. These pins function as strapped inputs only during reset and are used for other functions during normal operation (see “Strapping” on page 47). Note that these are *not multiplexed* pins since the function of the pins is not programmable.

The table lists the exact signal name associated with each package pin. It also provides a brief description of the function of each pin.

Pin Functional Description (Part 1 of 13)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Ball	Signal Name	Description	I/O	Type	Notes
PCI Interface (Number of pins = 60)					
A17 B16 C17 A18 D17 C18 B18 A20 B21 A23 D21 B22 B23 C22 C26 F25 K26 L23 M25 M23 N25 M26 N26 P24 R24 R23 P23 R25 T24 U26 T25 V26	PCIAD0 PCIAD1 PCIAD2 PCIAD3 PCIAD4 PCIAD5 PCIAD6 PCIAD7 PCIAD8 PCIAD9 PCIAD10 PCIAD11 PCIAD12 PCIAD13 PCIAD14 PCIAD15 PCIAD16 PCIAD17 PCIAD18 PCIAD19 PCIAD20 PCIAD21 PCIAD22 PCIAD23 PCIAD24 PCIAD25 PCIAD26 PCIAD27 PCIAD28 PCIAD29 PCIAD30 PCIAD31	PCI Address/Data Bus. Multiplexed address and data bus	I/O	5V tolerant 3.3V PCI	4
D19 F24 K24 R26	PCIC0[$\overline{\text{BE0}}$] PCIC1[$\overline{\text{BE1}}$] PCIC2[$\overline{\text{BE2}}$] PCIC3[$\overline{\text{BE3}}$]	PCI C (bus command) or $\overline{\text{B}}$yte enable	I/O	5V tolerant 3.3V PCI	4
E26	PCIParity	PCI parity. Parity is even across PCIAD0:31 and PCIC0:3[$\overline{\text{BE0:3}}$]. PCIParity is valid one cycle after either an address or data phase. The PCI device that drove PCIAD0:31 is responsible for driving PCIParity on the next PCI bus clock.	I/O	5V tolerant 3.3V PCI	4
J24	$\overline{\text{PCIFrame}}$	$\overline{\text{PCIFrame}}$ is driven by the current PCI bus master to indicate beginning and duration of a PCI access.	I/O	5V tolerant 3.3V PCI	4
J23	$\overline{\text{PCIIRDY}}$	$\overline{\text{PCIIRDY}}$ is driven by the current PCI bus master. Assertion of $\overline{\text{PCIIRDY}}$ indicates that the PCI initiator is ready to transfer data.	I/O	5V tolerant 3.3V PCI	4
G26	$\overline{\text{PCITRDY}}$	The target of the current PCI transaction drives $\overline{\text{PCITRDY}}$. Assertion of $\overline{\text{PCITRDY}}$ indicates that the PCI target is ready to transfer data.	I/O	5V tolerant 3.3V PCI	4
H23	$\overline{\text{PCIStop}}$	The target of the current PCI transaction may assert $\overline{\text{PCIStop}}$ to indicate to the requesting PCI master that it wants to end the current transaction.	I/O	5V tolerant 3.3V PCI	4

Pin Functional Description (Part 2 of 13)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Ball	Signal Name	Description	I/O	Type	Notes
H25	PCIDevSel	PCIDevSel is driven by the target of the current PCI transaction. A PCI target asserts PCIDevSel when it has decoded an address and command encoding and claims the transaction.	I/O	5V tolerant 3.3V PCI	4
P26	PCIIDSel	PCIIDSel is used during configuration cycles to select the PCI slave interface for configuration	I	5V tolerant 3.3V PCI Rcvr	5
G24	PCISErr	PCISErr is used for reporting address parity errors or catastrophic failures detected by a PCI target.	I/O	5V tolerant 3.3V PCI	4
G25	PCIPErr	PCIPErr is used for reporting data parity errors on PCI transactions. PCIPErr is driven active by the device receiving PCIAD0:31, PCIC0:3[BE0:3], and PCIParity, two PCI clocks following the data in which bad parity is detected.	I/O	5V tolerant 3.3V PCI	4
B20	PCIClk	PCIClk is used as the asynchronous PCI clock when in asynch mode. It is unused when the PCI interface is operated synchronously with the PLB bus.	I	5V tolerant 3.3V PCI Rcvr	5
B24	PCIReset	PCI specific reset	O	5V tolerant 3.3V PCI	
C23	PCIINT[PerWE]	PCI interrupt or Peripheral write enable. Logical AND of the four PerWBE0:3 write byte enables	O	5V tolerant 3.3V PCI	
C19	PCIReq0[Gnt]	Multipurpose signal, used as PCIReq0 when internal arbiter is used, and as Gnt when external arbiter is used.	I	5V tolerant 3.3V PCI Rcvr	4
C21 B19 A24 G23 J25	PCIReq1 PCIReq2 PCIReq3 PCIReq4 PCIReq5	Used as PCIReq1:5 input when internal arbiter is used	I	5V tolerant 3.3V PCI Rcvr	4
U23	PCIGnt0[Req]	Gnt0 when internal arbiter is used or Req when external arbiter is used	O	5V tolerant 3.3V PCI	
T23 F23 H26 N23 M24	PCIGnt1 PCIGnt2 PCIGnt3 PCIGnt4 PCIGnt5	Used as PCIGnt1:5 output when internal arbiter is used.	O	5V tolerant 3.3V PCI	

Pin Functional Description (Part 3 of 13)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Ball	Signal Name	Description	I/O	Type	Notes
Ethernet Interface (Number of pins = 18)					
AD20 AC20 AF23 AE23	PHYRxD3 PHYRxD2 PHYRxD1 PHYRxD0	Received data. This is a nibble wide bus from the PHY. The data is synchronous with the PhyRxClk.	I	5V tolerant 3.3V Rcvr	1, 4
P25 L24 L25 J26	EMCTxD3 EMCTxD2 EMCTxD1 EMCTxD0	Transmit data. A nibble wide data bus towards the net. The data is synchronous to the PHYTxClk.	O	5V tolerant 3.3V LVTTL	6
U24	PHYRxErr	Receive Error. This signal comes from the PHY and is synchronous to the PHYRxClk.	I	5V tolerant 3.3V LVTTL Rcvr	1, 5
AF20	PHYRxClk	Receiver Medium clock. This signal is generated by the PHY.	I	5V tolerant 3.3V LVTTL Rcvr	1, 4
V24	PHYRxDV	Receive Data Valid. Data on the Data Bus is valid when this signal is activated. Deassertion of this signal indicates end of the frame reception.	I	5V tolerant 3.3V LVTTL Rcvr	1, 5
W23	PHYCrS	Carrier Sense signal from the PHY. This is an asynchronous signal.	I	5V tolerant 3.3V LVTTL Rcvr	1, 5
K25	EMCTxErr	Transmit Error. This signal is generated by the Ethernet controller and is connected to the PHY. This signal informs the PHY that an error was detected. This signal is synchronous to the PHYTxClk.	O	5V tolerant 3.3V LVTTL	6
K23	EMCTxEn	Transmit data Enabled. This signal is driven by EMAC2 to the PHY. Data is valid during the active state of this signal. Deassertion of this signal indicates end of frame transmission. This signal is synchronous to the PHYTxClk.	O	5V tolerant 3.3V LVTTL	6
E25	PHYTxClk	This clock comes from the PHY and is the Medium Transmit clock	I	5V tolerant 3V LVTTL Rcvr	1, 4
AA25	PHYCol	Collision signal from the PHY. This is an asynchronous signal	I	5V tolerant 3.3V LVTTL Rcvr	1, 5
H24	EMCMDClk	Management Data Clock. The MDClk is sourced to the PHY. This clock has a period of 400ns, adjustable via the FMO_DIV_CLK register, with no maximum high or low times. Management information is transferred synchronously with respect to this clock.	Ot	5V tolerant 3.3V LVTTL	
AD26	EMCMDIO[PHYMDIO]	Management Data Input/Output is a bidirectional signal between the Ethernet controller and the PHY. It is used to transfer control and status information.	I/O	5V tolerant 3.3V LVTTL	1, 4

Pin Functional Description (Part 4 of 13)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Ball	Signal Name	Description	I/O	Type	Notes
SDRAM Interface (Number of pins = 72)					
AC13 AE12 AD11 AC11 AF10 AE11 AD10 AF9 AD9 AE9 AD8 AF7 AC8 AD7 AE6 AE5 AE4 AD5 AD4 AC5 AD1 AB2 AA4 AA2 AB01 Y2 W4 W2 W3 V4 W1 V3	MemData0 MemData1 MemData2 MemData3 MemData4 MemData5 MemData6 MemData7 MemData8 MemData9 MemData10 MemData11 MemData12 MemData13 MemData14 MemData15 MemData16 MemData17 MemData18 MemData19 MemData20 MemData21 MemData22 MemData23 MemData24 MemData25 MemData26 MemData27 MemData28 MemData29 MemData30 MemData31	Memory data bus	I/O	3.3V LVTTL	4
AC17 AD18 AF19 AC18 AD19 AE19 AC19 AE20 AF22 AD21 AE21 AC21 AE22	MemAddr12 MemAddr11 MemAddr10 MemAddr9 MemAddr8 MemAddr7 MemAddr6 MemAddr5 MemAddr4 MemAddr3 MemAddr2 MemAddr1 MemAddr0	Memory address bus	O	3.3V LVTTL	
AC24 AB24	BA1 BA0	Bank Address supporting up to 4 internal banks	O	3.3V LVTTL	
AF24	$\overline{RAS}$	Row Address Strobe	O	3.3V LVTTL	
AB23	$\overline{CAS}$	Column Address Strobe	O	3.3V LVTTL	
AC12 AC10 AC6 AA3	DQM0 DQM1 DQM2 DQM3	DQM for byte lanes 0, 1, 2, and 3	O	3.3V LVTTL	
AC15	DQMCB	DQM for ECC check bits	O	3.3V LVTTL	

Pin Functional Description (Part 5 of 13)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Ball	Signal Name	Description	I/O	Type	Notes
AE14 AF15 AF14 AD13 AF13 AF12 AE13 AD12	ECC0 ECC1 ECC2 ECC3 ECC4 ECC5 ECC6 ECC7	ECC check bits 0:7	I/O	3.3V LVTTL	4
AD17 AF17 AE15 AC14	$\overline{\text{BankSel0}}$ $\overline{\text{BankSel1}}$ $\overline{\text{BankSel2}}$ $\overline{\text{BankSel3}}$	Select up to four external SDRAM banks	O	3.3V LVTTL	
AC16	$\overline{\text{WE}}$	Write Enable	O	3.3V LVTTL	
AB25 AC25	ClkEn0 ClkEn1	SDRAM Clock Enable	O	3.3V LVTTL	
AC26 AA23	MemClkOut0 MemClkOut1	Two copies of an SDRAM clock allows, in some cases, glueless SDRAM attach without requiring this signal to be repowered by a PLL or zero-delay buffer.	O	3.3V LVTTL	
AF4		Reserved		r	
External SLAVE Peripheral Interface (Number of pins = 96)					
U4 U3 U1 T4 R2 P4 R4 P2 R1 P1 N3 N1 M1 N2 M3 M4 N4 M2 L3 L4 K1 L2 K3 J1 K4 J3 J2 J4 H3 G1 H2 H4	PerData0 PerData1 PerData2 PerData3 PerData4 PerData5 PerData6 PerData7 PerData8 PerData9 PerData10 PerData11 PerData12 PerData13 PerData14 PerData15 PerData16 PerData17 PerData18 PerData19 PerData20 PerData21 PerData22 PerData23 PerData24 PerData25 PerData26 PerData27 PerData28 PerData29 PerData30 PerData31	Peripheral data bus used by 405GP when not in external master mode, otherwise used by external master	I/O	5V tolerant 3.3V LVTTL	1

Pin Functional Description (Part 6 of 13)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Ball	Signal Name	Description	I/O	Type	Notes
D5 A3 B4 B5 D6 B6 C6 D7 A5 B7 C7 D8 B8 C8 D9 A8 C9 D10 C10 A10 D11 B12 D13 D12 B13 A12 A13 C14 A14 A15 C15 D15	PerAddr0 PerAddr1 PerAddr2 PerAddr3 PerAddr4 PerAddr5 PerAddr6 PerAddr7 PerAddr8 PerAddr9 PerAddr10 PerAddr11 PerAddr12 PerAddr13 PerAddr14 PerAddr15 PerAddr16 PerAddr17 PerAddr18 PerAddr19 PerAddr20 PerAddr21 PerAddr22 PerAddr23 PerAddr24 PerAddr25 PerAddr26 PerAddr27 PerAddr28 PerAddr29 PerAddr30 PerAddr31	Peripheral address bus used by 405GP when not in external master mode, otherwise used by external master.	I/O	5V tolerant 3.3V LVTTL	1
D3 G4 G3 E1	PerPar0 PerPar1 PerPar2 PerPar3	Peripheral byte parity signals	I/O	5V tolerant 3.3V LVTTL	1
D2 E2 F4 D1	$\overline{\text{PerWBE0}}$ $\overline{\text{PerWBE1}}$ $\overline{\text{PerWBE2}}$ $\overline{\text{PerWBE3}}$	As outputs, these pins can act as byte-enables which are valid for an entire cycle or as write-byte-enables which are valid for each byte on each data transfer, allowing partial word transactions. As outputs, pins are used by either peripheral controller or DMA controller depending upon the type of transfer involved. Used as inputs when external bus master owns the external interface	I/Ot	5V tolerant 3.3V LVTTL	1, 2
B3	$\overline{\text{PerCS0}}$	Peripheral chip select bank 0	O	5V tolerant 3.3V LVTTL	2
C4 C5 A4 B9 B10 A9 B11	$\overline{\text{PerCS1}}$[GPIO10] $\overline{\text{PerCS2}}$[GPIO11] $\overline{\text{PerCS3}}$[GPIO12] $\overline{\text{PerCS4}}$[GPIO13] $\overline{\text{PerCS5}}$[GPIO14] $\overline{\text{PerCS6}}$[GPIO15] PerCS7[GPIO16]	Seven additional peripheral chip selects or General Purpose I/O - To access this function, software must toggle a DCR register bit.	O[I/O]	5V tolerant 3.3V LVTTL [mux'd]	1,2

Pin Functional Description (Part 7 of 13)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Ball	Signal Name	Description	I/O	Type	Notes
C2	$\overline{\text{PerOE}}$	Used by either peripheral controller or DMA controller depending upon the type of transfer involved. When the 405GP is the bus master it enables the selected SDRAMs to drive the bus.	O	5V tolerant 3.3V LVTTL	2
C1	PerR/$\overline{\text{W}}$	Used by 405GP when not in external master mode as output by either the peripheral controller or DMA controller depending upon the type of transfer involved. High indicates a read from memory, low indicates a write to memory. Otherwise it used by the external master as an input to indicate the direction of transfer.	I/O	5V tolerant	1, 2
E3	PerReady	Used by a peripheral slave to indicate it is ready to transfer data	I	5V tolerant Rcvr	1, 2
F2	$\overline{\text{PerBLast}}$	Used by 405GP when not in external master mode, otherwise used by external master. Indicates the last transfer of a memory access.	I/O	5V tolerant 3.3V LVTTL	1, 4
C16 D14 C11 A7	DMAReq0 DMAReq1 DMAReq2 DMAReq3	DMAReq0:3 are used by slave peripherals to indicate they are prepared to transfer data.	I	5V tolerant Rcvr	1, 5
D16 B15 B14 C12	DMAAck0 DMAAck1 DMAAck2 DMAAck3	DMAAck0:3 are used by 405GP to indicate that data transfers have occurred.	O	5V tolerant 3.3V LVTTL	6
F3 G2 V2 Y1	EOT0[TC0] EOT1[TC1] EOT2[TC2] EOT3[TC3]	End Of Transfer/Terminal Count	I/O	5V tolerant 3.3V LVTTL	1, 5

Pin Functional Description (Part 8 of 13)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Ball	Signal Name	Description	I/O	Type	Notes
External MASTER Peripheral Interface (Number of pins = 9)					
E4	PerClk	Peripheral clock to be used by an external master and by synchronous peripheral slaves	O	5V tolerant 3.3V LVTTL	
T3	$\overline{\text{ExtReset}}$	Peripheral reset to be used by an external master and by synchronous peripheral slaves	O	5V tolerant 3.3V LVTTL	
V1	HoldReq	Hold Request, used by an external master to request ownership of the peripheral bus	I	5V tolerant Rcvr	1, 5
U2	HoldAck	Hold Acknowledge, used by 405GP to transfer ownership of peripheral bus to an external master	O	5V tolerant 3.3V LVTTL	6
Y4	$\overline{\text{ExtReq}}$	ExtReq is used by an external master to indicate it is prepared to transfer data	I	5V tolerant Rcvr	1, 4
Y3	$\overline{\text{ExtAck}}$	ExtAck is used by 405GP to indicate that a data transfer occurred.	O	5V tolerant 3.3V LVTTL	6
T2	HoldPri	Used by an external master to indicate the priority of a given transfer (0 = high, 1 = low)	I	5V tolerant Rcvr	1, 4
R3	BusReq	Used when 405GP needs to regain control of peripheral interface from an external Master	O	5V tolerant 3.3V LVTTL	
B1	PerErr	Used as an input used to record external Master errors and external slave peripheral errors	I	5V tolerant Rcvr	1, 5
Internal Peripheral Interface (Number of pins = 15)					
AE17	UARTSerClk	Serial Clock used to provide an alternative clock to the internally generated serial clock. Used in cases where the allowable internally generated baud rates are not satisfactory. This input can be individually connected to either UART.	I	5V tolerant 3.3V LVTTL	1, 4
AE16	UART0_Rx	UART0 Serial in data	I	5V tolerant 3.3V LVTTL	1, 4
AF3	UART0_Tx	UART0 Serial out data	O	5V tolerant 3.3V LVTTL	6
AE18	$\overline{\text{UART0\_DCD}}$	UART0 Data Carrier Detect	I	5V tolerant 3.3V LVTTL	1, 4
AE3	$\overline{\text{UART0\_DSR}}$	UART0 Data Set Ready	I	5V tolerant 3.3V LVTTL	1, 4
AB4	$\overline{\text{UART0\_CTS}}$	UART0 Clear To Send	I	5V tolerant 3.3V LVTTL	1, 4
AF2	$\overline{\text{UART0\_DTR}}$	UART0 Data Terminal Ready	O	5V tolerant 3.3V LVTTL	6
AD16	$\overline{\text{UART0\_RTS}}$	UART0 Request To Send	O	5V tolerant 3.3V LVTTL	6
AD15	$\overline{\text{UART0\_RI}}$	UART0 Ring Indicator	I	5V tolerant 3.3V LVTTL Rcvr	1, 4

Pin Functional Description (Part 9 of 13)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Ball	Signal Name	Description	I/O	Type	Notes
AC1	UART1_Rx	UART1 Serial In data	I	5V tolerant 3.3V LVTTL Rcvr	1, 4
AC2	UART1_Tx	UART1 Serial Out data.	O	5V tolerant 3.3V LVTTL	6
AC3	$\overline{\text{UART1\_DSR}}$ [UART1_CTS]	UART1 Data Set Ready. or UART1Clear To Send. To access this function, software must toggle a DCR register bit.	I	5V tolerant 3.3V LVTTL Rcvr	1, 4
AD2	$\overline{\text{UART1\_RTS}}$ [UART1_DTR]	Request To Send. Data Terminal Ready. To access this function, software must toggle a DCR register bit.	O	5V tolerant 3.3V LVTTL	6
AD6	IICSCL	IIC Serial Clock	I/O	5V tolerant 3.3V LVTTL	1, 2
AE7	IICSDA	IIC Serial Data	I/O	5V tolerant 3.3V LVTTL	1, 2
Interrupts Interface (Number of pins = 7)					
V25 V23 W24 W25 Y24 Y25 AA24	IRQ0[GPIO17] IRQ1[GPIO18] IRQ2[GPIO19] IRQ3[GPIO20] IRQ4[GPIO21] IRQ5[GPIO22] IRQ6[GPIO23]	Interrupt requests or General Purpose I/O. To access this function , software must toggle a DCR register bit.]	I[I/O]	5V tolerant 3.3V LVTTL	1, 5
JTAG Interface (Number of pins = 5)					
AE24	TDI	Test data in	I	5V tolerant 3.3V LVTTL Rcvr	1, 4
AC22	TMS	JTAG test mode select	I	5V tolerant 3.3V LVTTL Rcvr	1, 4
AD23	TDO	Test data out	O	5V tolerant 3.3V LVTTL	
AD22	TCK	JTAG test clock	I	5V tolerant 3.3V LVTTL Rcvr	1, 4
AE26	$\overline{\text{TRST}}$	JTAG reset	I	5V tolerant Rcvr	5

Pin Functional Description (Part 10 of 13)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Ball	Signal Name	Description	I/O	Type	Notes
System Interface (Number of pins = 19)					
A25	SysClk	Main system clock input	I	5V tolerant 3.3V LVTTL Rcvr	
D22	$\overline{\text{SysReset}}$	Main system reset. This pin may be redriven by the 405GP to allow a system reset to occur.	I/O	5V tolerant 3.3V LVTTL Rcvr	1, 2
D25	AV_{DD}	Clean voltage input for a PLL	I		
AD25	SysErr	Set to 1 when a Machine Check is generated	O	5V tolerant 3.3V LVTTL	
AB26	$\overline{\text{Halt}}$	Halt from external debugger.	I	5V tolerant 3.3V LVTTL Rcvr	1, 4
D18 C20	GPIO1[TS1E] GPIO2[TS2E]	General Purpose I/O or Even Trace execution status.To access this function, software must toggle a DCR register bit.	I/O[O]	5V tolerant 3.3V LVTTL	1, 6
A22 AF18	GPIO3[TS1O] GPIO4[TS2O]	General Purpose I/O Odd Trace execution status. To access this function, software must toggle a DCR register bit.	I/O[O]	5V tolerant 3.3V LVTTL	1 (A22, AF18), 6 (AF18 only)
AC9 AE8 AF5 AC7	GPIO5[TS3] GPIO6[TS4] GPIO7[TS5] GPIO8[TS6]	General Purpose I/O Trace status. To access this function, software must toggle a DCR register bit.	I/O[O]	5V tolerant 3.3V LVTTL	1, 4
AB3	GPIO9[TrcClk]]	General Purpose I/O or Trace interface clock. This signal is a toggling signal which comes out of a register in the CPU which is clocked at the CPU frequency. Therefore, this signal is always half of the CPU core frequency. To access this function, software must toggle a DCR register bit.	I/O[O]	5V tolerant 3.3V LVTTL	1, 4
D26	TestEn	Test Enable	I	5V tolerant Rcvr w/ PD	3
C25	RcvrInh	Receiver Inhibit	I	5V tolerant Rcvr	2
E24 E23	DrvrInh1 DrvrInh2	Driver Inhibit 1 and 2	I	5V tolerant Rcvr	2
D24	TmrClk	This input must toggle at a rate of less than one half the CPU core frequency (less than 100MHz in most cases). It is expected that in almost every case this input will toggle much slower, perhaps in the 1MHz to 10MHz range.	I	5V tolerant 3.3V LVTTL Rcvr	1, 4

Pin Functional Description (Part 11 of 13)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Ball	Signal Name	Description	I/O	Type	Notes
Ground pins (Number of pins = 96)					
A1 A2 A6 A11 A16 A19 A21 A26 B2 B25 B26 C3 C24 D4 D23 E5 E09 E13 E14 E18 E22 F1 F26 H1 J5 J22 L1 L11-L16 L26 M11-M16 N5 N11-N16 N22 P5 P11-P16 P22 R11-R16 T1 T11-T16 T26 V5 V22 W26 AA1 AA26 AB5	GND	Ground **Note:** L11-L16, M11-M16, N11-N16, P11-P16, R11-R16, and T11-T16 are also thermal balls.			

Pin Functional Description (Part 12 of 13)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Ball	Signal Name	Description	I/O	Type	Notes
Ground pins (continued)					
AB9 AB13 AB14 AB18 AB22 AC4 AC23 AD3 AD24 AE1 AE2 AE25 AF1 AF6 AF8 AF11 AF16 AF21 AF25 AF26	GND	Ground			
OV_{DD} pins (Number of pins = 32					
B17 C13 E6 E7 E8 E19 E20 E21 F5 F22 G5 G22 H5 H22 K2 N24 P3 U25 W5 W22 Y5 Y22 AA5 AA22 AB6 AB7 AB8 AB19 AB20 AB21 AD14 AE10	OVDD	Output driver voltage—3.3V			

Pin Functional Description (Part 13 of 13)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Ball	Signal Name	Description	I/O	Type	Notes
V_{DD} pins (Number of pins = 24)					
E10 E11 E12 E15 E16 E17 K5 K22 L5 L22 M5 M22 R5 R22 T5 T22 U5 U22 AB10 AB11 AB12 AB15 AB16 AB17	VDD	Logic voltage—2.5V			
Other pins (Number of pins = 3)					
D20 Y23 Y26		No connection			

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings may cause permanent damage to the device

Characteristic	Symbol	Value	Unit
Supply Voltage (Internal Logic)	V_{DD}	0 to 2.7[1]	V
Supply Voltage (I/O Interface)	OV_{DD}	0 to 3.6[1]	V
PLL Supply Voltage	AV_{DD}	0 to 2.7	V
Input Voltage (3.3V LVTTL receivers)	V_{IN}	0 to 3.6	V
Input Voltage (5.0V LVTTL receivers)	V_{IN}	0 to 5.5	V
Storage Temperature Range	T_{STG}	-55 to 150	°C
Case temperature under bias	T_C	-40 to +120	°C

Note: If $OV_{DD} \geq 0.4V$ it is required that $V_{DD} \geq 0.4V$. Supply excursions not meeting this criteria must be limited to less than 25ms duration during each power up or power down event.

Package Thermal Specifications

The 405GP is designed to operate within a case temperature range of -40˚C to 120˚C. Thermal resistance values for the 456-ball E-PBGA package in a convection environment are as follows:

Parameter	Symbol	Airflow ft/min (m/sec)			Unit
		0 (0)	100 (0.51)	200 (1.02)	
Junction-to-case thermal resistance	θ_{JC}	2	2	2	°C/W
Case-to-ambient thermal resistance (without heat sink)	θ_{CA}	14	13	12	°C/W

Notes:
1. Case temperature, T_C , is measured at top center of case surface with device soldered to circuit board.
2. $T_A = T_C - P \times \theta_{CA}$, where T_A is ambient temperature and P is power consumption.
3. $T_{CMax} = T_{JMax} - P \times \theta_{JC}$, where T_{JMax} is maximum junction temperature and P is power consumption.
4. The above assumes that the chip is mounted on a card with at least one signal and two power planes.

Recommended DC Operating Conditions

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions may affect device reliability.

Notes:

1. PCI drivers meet PCI specifications
2. It is recommended that your system design derive the V_{DD} supply from the OV_{DD} supply so as to minimize the possibility of V_{DD} being present in the absence of OV_{DD}.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Logic Supply Voltage	V_{DD}	2.3	2.5	2.7	V	2
I/O Supply Voltage	OV_{DD}	3.0	3.3	3.6	V	2
PLL Supply Voltage	AV_{DD}	2.3	2.5	2.7	V	
Input Logic High (3.3V LVTTL receivers)	V_{IH}	2.0		OV_{DD}	V	
Input Logic High (5.0V LVTTL receivers)	V_{IH}	2.0		5.5	V	
Input Logic Low	V_{IL}	0		0.8	V	
Output Logic High	V_{OH}	2.4		OV_{DD}	V	
Output Logic Low	V_{OL}	0		0.4	V	
Input Leakage Current (No pull-up or pull-down)	I_{IL1}	0		0	µA	
Input Leakage Current for Pull-Down	I_{IL2}	0 (LPDL)		400 (MPUL)	µA	
Input Leakage Current for Pull-Up	I_{IL3}	–250 (LPDL)		0 (MPUL)	µA	
Input Max Allowable Overshoot (3.3V LVTTL receivers)	V_{IMAO3}			OV_{DD} + 0.6	V	
Input Max Allowable Overshoot (5.0V LVTTL receivers)	V_{IMAO5}			5.5	V	
Input Max Allowable Undershoot (3.3V or 5.0V receivers)	V_{IMAU}	– 0.6			V	
Output Max Allowable Overshoot (3.3V or 5.0V receivers)	V_{OMAO}			OV_{DD} + 0.3	V	
Output Max Allowable Undershoot (3.3V and 5.0V receivers)	V_{OMAU3}	– 0.6			V	
Case Temperature	T_C	– 40		85	°C	

Capacitance

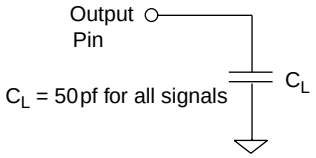
Parameter	Symbol	Maximum	Unit	Notes
Input Capacitance Group 1 (3.3V LVTTL //O)	CIN1	2.5	pF	1, 3
Input Capacitance Group 2 (5V tolerant LVTTL I/O)	CIN2	3.5	pF	2, 3
Input Capacitance Group 3(PCI I/O)	CIN3	5.0	pF	
Input Capacitance Group 1 (RX only pins)	CIN4	0.75	pF	

DC Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Active Operating Current (V_{DD})	I_{DD}		tbd		mA
Active Operating Current (OV_{DD})	I_{ODD}		tbd		mA
PLL Voltage	V_{PLL}	2.3	2.5	2.7	V
PLL VDD Input current	I_{PLL}		16	23	mA

Test Conditions

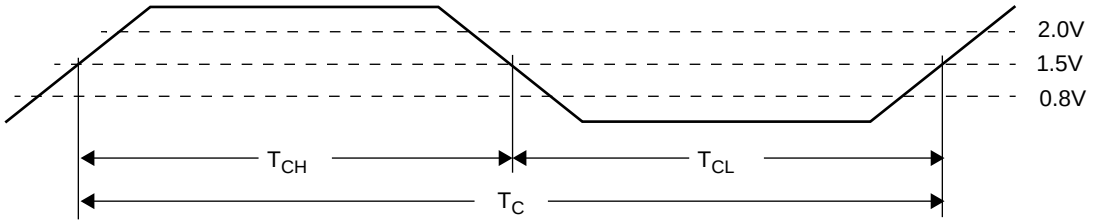
Clock timing and switching characteristics are specified in accordance with operating conditions shown in the table "Recommended DC Operating Conditions." AC specifications are characterized at V_{DD} = 3.14V and T_J = 100˚C with the 50pF test load (C_L) shown in the figure at right.



SysClk and MemClk Timing

Symbol	Parameter	Min	Max	Units
SysClk Input				
F_C	SysClk clock input frequency	25	66.6	MHz
T_C	SysClk clock period	15	40	ns
T_{CH}	Clock input high time	40% of nominal period	60% of nominal period	ns
T_{CL}	Clock input low time	40% of nominal period	60% of nominal period	ns
Note: Input slew rate > 2V/ns				
MemClk Output				
F_C	MemClk clock output frequency		100	MHz
T_C	MemClk clock period	10		ns
T_{CH}	Clock output high time	35% of nominal period	65% of nominal period	ns
T_{CL}	Clock output low time	35% of nominal period	65% of nominal period	ns

Timing Waveform



Spread Spectrum Clocking

Care must be taken when using a spread spectrum clock generator (SSCG) with the 405GP. This controller uses a PLL for clock generation inside the chip. The accuracy with which the PLL follows the SSCG is referred to as tracking skew. The PLL bandwidth and phase angle determine how much tracking skew there is between the SSCG and the PLL for a given frequency deviation and modulation frequency. When using an SSCG with the 405GP the following conditions must be met:

- The frequency deviation must not violate the minimum clock cycle time. Therefore, when operating the 405GP with one or more internal clocks at their maximum supported frequency, the SSCG may only lower the frequency.
- The maximum frequency deviation cannot exceed –5%, and the modulation frequency cannot exceed 40kHz. In some cases, on-board 405GP peripherals impose more stringent requirements (see Note 1).
- Use the Peripheral Bus Clock for logic that is synchronous to the peripheral bus since this clock tracks the modulation.
- Use the SDRAM MemClk since it also tracks the modulation.

Note 1: The PCI clock specification for 66MHz allows a maximum frequency deviation of -1% at a modulation between 30kHz and 33kHz. PCI asynchronous mode is unaffected.

Note 2: The serial port baud rates are synchronous to the modulated clock. The serial port has a tolerance of approximately 1.5% on baud rate before framing errors begin to occur. The 1.5% tolerance assumes that the connected device is running at precise baud rates.

Note 3: Ethernet operation is unaffected.

Note 4: IIC operation is unaffected.

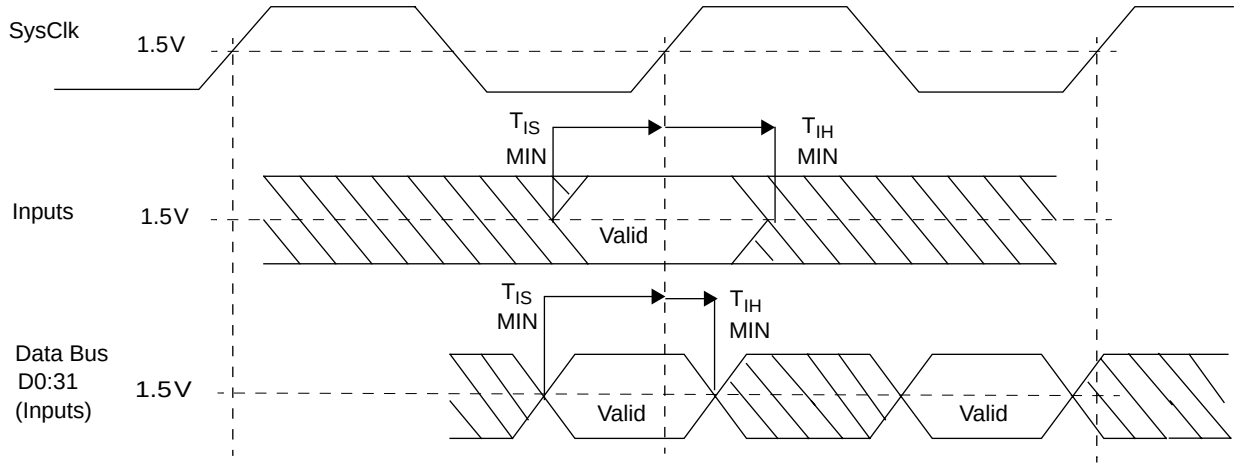
Caution: It is up to the system designer to ensure that any SSCG used with the 405GP meets the above requirements and does not adversely affect other aspects of the system.

Peripheral Interface Clock Timings

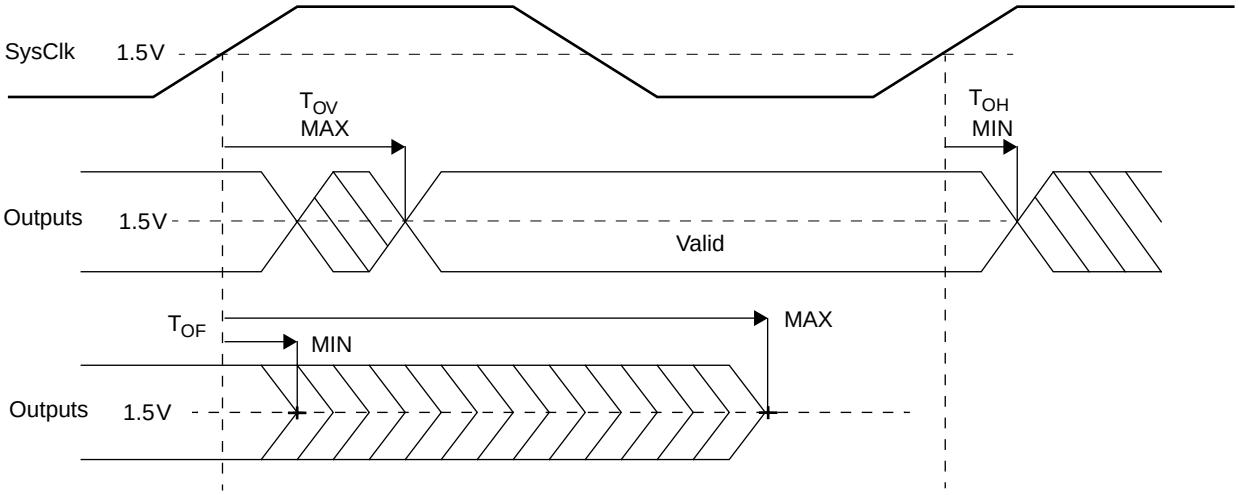
Parameter	Min	Max	Units
PCIClk input frequency (async mode PCI clock)	20	66	MHz
PCIClk period	15	50	ns
PCIClk input high time	40% of nominal period	60% of nominal period	ns
PCIClk input low time	40% of nominal period	60% of nominal period	ns
EMCMDClk output frequency	–	2.5	MHz
EMCMDClk period	400	–	ns
EMCMDClk output high time	160	–	ns
EMCMDClk output low time	160	–	ns
PhyTxClk input frequency	2.5	25	MHz
PhyTxClk period	40	400	ns
PhyTxClk input high time	35% of nominal period	–	ns
PhyTxClk input low time	35% of nominal period	–	ns
PhyRxClk input frequency	2.5	25	MHz
PhyRxClk period	40	400	ns
PhyRxClk input high time	35% of nominal period	–	ns
PhyRxClk input low time	35% of nominal period	–	ns
PerClk output frequency (for external master or synchronous slaves)	–	50	MHz
PerClk period	20	–	ns
PerClk output high time	50% of nominal period	66% of nominal period	ns
PerClk output low time	33% of nominal period	50% of nominal period	ns
UARTSerClk input frequency[1]	–	$10^3/(2T_{OPB}+2ns)$	MHz
UARTSerClk period	$2T_{OPB}+2$	–	ns
UARTSerClk input high time	$T_{OPB}+1$	–	ns
UARTSerClk input low time	$T_{OPB}+1$	–	ns
TmrClk input frequency	–	50	MHz
TmrClk period	20	–	ns
TmrClk input high time	40% of nominal period	60% of nominal period	ns
TmrClk input low time	40% of nominal period	60% of nominal period	ns

[1] T_{OPB} is the period in ns of the OPB clock. The internal OPB clock runs at half the frequency of the PLB clock. The maximum OPB clock frequency is 50 MHz.

Input Setup and Hold Waveform



Output Delay and Float Timing Waveform



I/O Specifications (Part 1 of 4)

Notes:

1. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
2. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
3. PCI timings are for asynchronous operation up to 66MHz . PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.
4. SDRAM CLK0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50 pF load	I/O H (maximum)	I/O L (minimum)		
PCI Interface								
PCIAD0:31	3	0	6	1.8	12.3	15.5	PCIClk	3
PCIC0:3[$\overline{\text{BE}}$0:3]	3	0	6	1.8	12.3	15.5	PCIClk	3
PCIClk	dc	dc		n/a	n/a	n/a		async
$\overline{\text{PCIDevSel}}$	3	0	6	1.8	12.3	15.5	PCIClk	3
$\overline{\text{PCIFrame}}$	3	0	6	1.8	12.3	15.5	PCIClk	3
$\overline{\text{PCIGnt0[Req]}}$ $\overline{\text{PCIGnt1:5}}$	n/a	n/a	6	1.8	12.3	15.5	PCIClk	3
PCIIDSel	3	0	6	1.8	n/a	n/a	PCIClk	3
$\overline{\text{PCIINT[PerWE]}}$	n/a	n/a	dc	dc	12.3	15.5	PCIClk	async
$\overline{\text{PCIIRDY}}$	3	0	6	1.8	12.3	15.5	PCIClk	3
PCIParity	3	0	6	1.8	12.3	15.5	PCIClk	3
$\overline{\text{PCIPErr}}$	3	0	6	1.8	12.3	15.5	PCIClk	3
$\overline{\text{PCIReq0[Gnt]}}$ $\overline{\text{PCIReq1:5}}$	5	0	n/a	n/a	n/a	n/a	PCIClk	3
$\overline{\text{PCIReset}}$	n/a	n/a	n/a	n/a	12.3	15.5	PCIClk	
$\overline{\text{PCISErr}}$	n/a	n/a	n/a	n/a	12.3	15.5	PCIClk	
$\overline{\text{PCIStop}}$	3	0	6	1.8	12.3	15.5	PCIClk	3
$\overline{\text{PCITRDY}}$	3	0	6	1.8	12.3	15.5	PCIClk	3
Ethernet Interface								
EMCMDClk	n/a	n/a	settable	2	9	6		async
EMCMDIO[PHYMDIO]	n/a	n/a	36	2	9	6	PHYTX	
EMCTxD0:3	n/a	n/a	20	2	9	6	PHYTX	
EMCTxEn	n/a	n/a	20	2	9	6	PHYTX	
EMCTxErr	n/a	n/a	20	2	9	6	PHYTX	
PHYCol					9	6		async
PHYCrS					9	6		async
PHYRxClk					n/a	n/a		async
PHYRxD0:3	4	1	n/a	n/a	9	6	PHYRX	
PHYRxDV	4	1	n/a	n/a	9	6	PHYRX	
PHYRxErr	4	1	n/a	n/a	9	6	PHYRX	
PHYTxClk					n/a	n/a		async

I/O Specifications (Part 2 of 4)

Notes:

1. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
2. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
3. PCI timings are for asynchronous operation up to 66MHz . PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.
4. SDRAM CLK0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50 pF load	I/O H (maximum)	I/O L (minimum)		
SDRAM Interface								
BA0:1	n/a	n/a	7.5	1	19	12	SysClk	1, 2
$\overline{\text{BankSel0:3}}$	n/a	n/a	6	1	19	12	SysClk	2
$\overline{\text{CAS}}$	n/a	n/a	7.5	1	19	12	SysClk	1, 2
ClkEn0:1	n/a	n/a	5	1	40	25	SysClk	2
DQM0:3	n/a	n/a	6	1	19	12	SysClk	2
DQMCB	n/a	n/a	6	1	19	12	SysClk	2
ECC0:7	2	1	6	1	19	12	SysClk	2
MemAddr0:12	n/a	n/a	7.5	1	19	12	SysClk	1, 2
MemClkOut0:1	n/a	n/a	0	-1	19	12	SysClk	2,4
MemData0:31	2	1	6	1	19	12	SysClk	2
$\overline{\text{RAS}}$	n/a	n/a	7.5	1	19	12	SysClk	1, 2
$\overline{\text{WE}}$	n/a	n/a	7.5	1	19	12	SysClk	1, 2
External SLAVE Peripheral Interface								
DMAAck0:3	n/a	n/a	8	0	12	8	PerClk	
DMAReq0:3	dc	dc	n/a	n/a	n/a	n/a	PerClk	
EOT0:3[TC0:3]	dc	dc	8	0	12	8	PerClk	
PerAddr0:31	6	1	10	0	19	12	PerClk	
$\overline{\text{PerBLast}}$	6	1	8	0	12	8	PerClk	
$\overline{\text{PerCS0}}$ $\overline{\text{PerCS1:7}}$[GPIO10:16]	n/a	n/a	8	0	12	8	PerClk	
PerData0:31	6	1	10	0	19	12	PerClk	
$\overline{\text{PerOE}}$	n/a	n/a	8	0	12	8	PerClk	
PerPar0:3	6	1	10	0	19	12	PerClk	
PerR/$\overline{\text{W}}$	6	1	8	0	12	8	PerClk	
PerReady	10	1	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{PerWBE0:3}}$	6	1	8	0	12	8	PerClk	
External MASTER Peripheral Interface								
BusReq	n/a	n/a	8	0	12	8	PerClk	
$\overline{\text{ExtAck}}$	n/a	n/a	7	0	12	8	PerClk	
$\overline{\text{ExtReq}}$	6	1	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{ExtReset}}$	n/a	n/a	8	0	19	12	PerClk	
HoldAck	n/a	n/a	8	0	12	8	PerClk	
HoldPri	6	1	n/a	n/a	n/a	n/a	PerClk	
HoldReq	8	1	n/a	n/a	n/a	n/a	PerClk	
PerClk	n/a	n/a	0.9	0.7	19	12	PLB Clk	5
PerErr	6	1	n/a	n/a	n/a	n/a	PerClk	

I/O Specifications (Part 3 of 4)

Notes:

1. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
2. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
3. PCI timings are for asynchronous operation up to 66MHz . PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.
4. SDRAM CLK0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50 pF load	I/O H (maximum)	I/O L (minimum)		
Internal Peripheral Interface								
IICSCL					19	12		
IICSDA					19	12		
$\overline{\text{UART0\_CTS}}$					12	8		
$\overline{\text{UART0\_DCD}}$					12	8		
$\overline{\text{UART0\_DSR}}$					12	8		
$\overline{\text{UART0\_DTR}}$					12	8		
$\overline{\text{UART0\_RI}}$					12	8		
$\overline{\text{UART0\_RTS}}$					12	8		
UART0_Rx					12	8		
UART0_Tx					12	8		
$\overline{\text{UART1\_RTS}}$ [$\overline{\text{UART1\_DTR}}$]					12	8		
$\overline{\text{UART1\_DSR}}$ [$\overline{\text{UART1\_CTS}}$]					n/a	n/a		
UART1_Rx					n/a	n/a		
UART1_Tx					12	8		
UARTSerClk					n/a	n/a		
Interrupts Interface								
IRQ0:6[GPIO17:23]					12	8		
JTAG Interface								
TCK					n/a	n/a		async
TDI					n/a	n/a		async
TDO					12	8		async
TMS					n/a	n/a		async
$\overline{\text{TRST}}$					n/a	n/a		async
System Interface								
DrvrInh1:2	dc	dc	n/a	n/a	n/a	n/a		
GPIO1[TS1E] GPIO2[TS2E] GPIO3[TS1O] GPIO4[TS2O] GPIO5[TS3] GPIO6[TS4] GPIO7[TS5] GPIO8[TS6] GPIO9[TrcClk]					12	8		
$\overline{\text{Halt}}$	dc	dc	n/a	n/a	n/a	n/a		async
RcvrInh	dc	dc	n/a	n/a	n/a	n/a		

I/O Specifications (Part 4 of 4)

Notes:

1. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
2. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
3. PCI timings are for asynchronous operation up to 66MHz . PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.
4. SDRAM CLK0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50 pF load	I/O H (maximum)	I/O L (minimum)		
SysClk			n/a	n/a	n/a	n/a		
SysErr			n/a	n/a	12	8		async
$\overline{\text{SysReset}}$					12	8		async
TestEn	dc	dc	n/a	n/a	n/a	n/a		async
TmrClk	dc	dc	n/a	n/a	n/a	n/a		async

Strapping

While the $\overline{\text{SysReset}}$ input pin is low (system reset), the state of certain I/O pins is read to enable default initial conditions prior to PPC405GP start-up. The actual capture instant is the nearest reference clock edge before the deassertion of reset. These pins must be strapped using external pull-up (logical 1) or pull-down (logical 0) resistors to select the desired default conditions. These pins are use for strap functions only during reset. They are used for other signals during normal operation. The following table lists the strapping pins along with their functions and strapping options:

Strapping Pin Assignments

Function	Option	Ball Strapping		
PLL Tuning for $6 \le M \le 7$ use choice 3 for $7 < M \le 12$ use choice 5 for $12 < M \le 32$ use choice 6 See Note.		**AF3**	**AF2**	**AD16**
	Choice 1; TUNE[5:0] = 010001	0	0	0
	Choice 2; TUNE[5:0] = 010010	0	0	1
	Choice 3; TUNE[5:0] = 010011	0	1	0
	Choice 4; TUNE[5:0] = 010100	0	1	1
	Choice 5; TUNE[5:0] = 010101	1	0	0
	Choice 6; TUNE[5:0] = 010110	1	0	1
	Choice 7; TUNE[5:0] = 010111	1	1	0
	Choice 8; TUNE[5:0] = 100100	1	1	1
PLL Forward Divider		**D16**	**B15**	
	Bypass mode	0	0	
	Divide by 3	0	1	
	Divide by 4	1	0	
	Divide by 6	1	1	
PLL Feedback Divider		**B14**	**C12**	
	Divide by 1	0	0	
	Divide by 2	0	1	
	Divide by 3	1	0	
	Divide by 4	1	1	
PLB Divider from CPU		**P25**	**L24**	
	Divide by 1	0	0	
	Divide by 2	0	1	
	Divide by 3	1	0	
	Divide by 4	1	1	
OPB Divider from PLB		**L25**	**J26**	
	Divide by 1	0	0	
	Divide by 2	0	1	
	Divide by 3	1	0	
	Divide by 4	1	1	

Strapping Pin Assignments

Function	Option	Ball Strapping		
PCI Divider from PLB		**D18**	**C20**	
	Divide by 1	0	0	
	Divide by 2	0	1	
	Divide by 3	1	0	
	Divide by 4	1	1	
External Bus Divider from PLB		**K25**	**K23**	
	Divide by 2	0	0	
	Divide by 3	0	1	
	Divide by 4	1	0	
	Divide by 5	1	1	
ROM Width		**AC2**	**AD2**	
	8-bit ROM	0	0	
	16-bit ROM	0	1	
	32-bit ROM	1	0	
	Reserved	1	1	
ROM Location		**U2**		
	405GP Peripheral Attach	0		
	405GP PCI Attach	1		
PCI Asynchronous Mode Enable		**Y3**		
	Synchronous PCI Mode	0		
	Asynchronous Mode	1		
PCI Arbiter Enable		**AF18**		
	Internal Arbiter Disabled	0		
	Internal Arbiter Enabled	1		

Note: The tune bits adjust parameters that control PLL jitter. The recommended values minimize jitter for the PLL implemented in the 405GP. These bits are shown for information only; and do not require modification except in special clocking circumstances such as spread spectrum clocking. For details on the use of Spread Spectrum Clock Generators (SSCGs) with the 405GP, visit the technical documents area of the IBM PowerPC web site.

(Inside of back cover page)

Copyright

Trademarks

The following are trademarks of International Business Machines Corporation in the United States, or other countries, or both:

Blue Logic	IBM	PowerPC 405GP
CodePack	IBM Logo	
CoreConnect	PowerPC	

Other company, product, and service names may be trademarks or service marks of others.

Preliminary Edition (1/27/00)
This document is the preliminary edition of the PowerPC 405GP Data Sheet. Make sure you are using the correct edition for the level of the product.

While the information contained herein is believed to be accurate, such information is preliminary, and should not be relied upon for accuracy or completeness, and no representations or warranties of accuracy or completeness are made.

This document contains information on a new product under development by IBM. IBM reserves the right to change or discontinue this product without notice.