bq27741-G1 Single-Cell Li-Ion Battery Fuel Gauge with Integrated Protection

1 Features

- Battery Fuel Gauge and Protector for 1-Series Li-Ion Applications
- Microcontroller Peripheral Provides:
  - Accurate Battery Fuel Gauging Supports up to 14,500 mAh
  - External and Internal Temperature Sensors for Battery Temperature Reporting
  - Precision 16-Bit High-Side Coulomb Counter with High-Side Low-Value Sense Resistor (5 mΩ to 20 mΩ)
  - Lifetime and Current Data Logging
  - 64 Bytes of Non-Volatile Scratch Pad Flash
  - SHA-1/HMAC Authentication
- Battery Fuel Gauging Based on Patented Impedance Track™ Technology
  - Models Battery Discharge Curve for Accurate Time-To-Empty Predictions
  - Automatically Adjusts for Aging, Self-Discharge, and Temperature- and Rate-Induced Effects on Battery
- Advanced Fuel Gauging Features
  - Internal Short Detection
  - Tab Disconnection Detection
- Safety and Protection:
  - Over- and Undervoltage Protection with Low-Power Mode
  - Overcharging and Discharging Current Protection
  - Overtemperature Protection
  - Short-Circuit Protection
  - Low-Voltage Notification
  - Voltage Doubler to Support High-Side N-Channel FET Protection
- HDQ and I^2C Interface Formats for Communication with Host System
- Small 15-Ball NanoFree™ (BGA) Packaging

2 Applications

- Smartphones
- PDAs
- Digital Still and Video Cameras
- Handheld Terminals
- MP3 or Multimedia Players

3 Description

The Texas Instruments bq27741-G1 Li-Ion battery fuel gauge is a microcontroller peripheral that provides fuel gauging for single-cell Li-Ion battery packs. The device requires little system microcontroller firmware development for accurate battery fuel gauging. The fuel gauge resides within the battery pack or on the system's main board with an embedded battery (non-removable). The fuel gauge provides hardware-based over- and undervoltage, overcurrent in charge or discharge, and short-circuit protections.

The fuel gauge uses the patented Impedance Track™ algorithm for fuel gauging, and provides information such as remaining battery capacity (mAh), state-of-charge (%), run-time to empty (minimum), battery voltage (mV), and temperature (°C), as well as recording vital parameters throughout the lifetime of the battery.

The device comes in a 15-ball BGA package (2.776 mm × 1.96 mm) that is ideal for space-constrained applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq27741-G1	YZF (15)	2.78 mm × 1.96 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

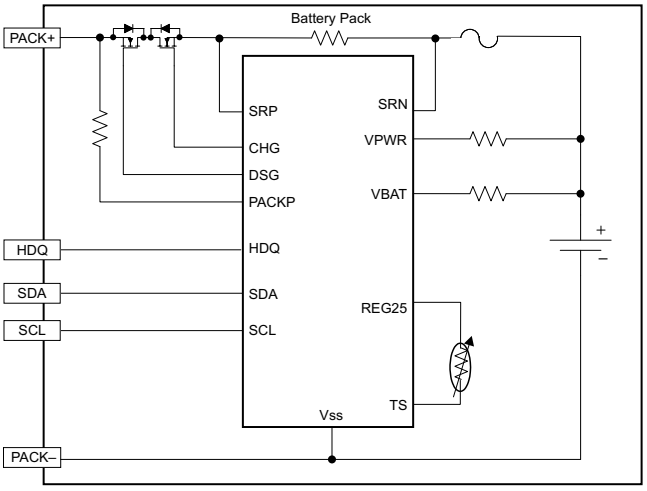


Table of Contents

4 Revision History

Changes from Revision B (April 2015) to Revision C **Page**

- Changed *Pin Configuration and Functions* ... 3
- Changed *Absolute Maximum Ratings* ... 4
- Changed *Recommended Operating Conditions* ... 5
- Changed *Functional Block Diagram* ... 12
- Deleted *UNDERTEMPERATURE FAULT Mode* ... 21
- Added *Community Resources* ... 32

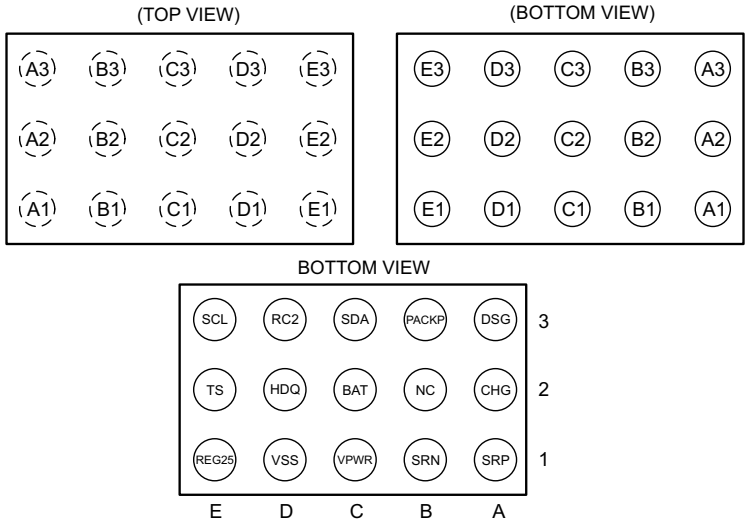
5 Device Comparison Table

PRODUCTION PART NO.(1)	FIRMWARE VERSION	COMMUNICATION FORMAT
bq27741YZFR-G1	1.08	I^2C, HDQ(1)
bq27741YZFT-G1		

(1) bq27741-G1 is shipped in the I^2C mode.

6 Pin Configuration and Functions

YZF Package
15-Pin DSBGA



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
BAT	C2	IA	Cell-voltage measurement input. ADC input
CHG	A2	O	External high-side N-channel charge FET driver
DSG	A3	O	External high-side N-channel discharge FET driver
HDQ	D2	IO	HDQ serial communications line. Open-drain
PACKP	B3	IA	Pack voltage measurement input for protector operation
NC	B2	IO	Not used. Reserved for future GPIO. Recommended to connect to GND.
RC2	D3	IO	General purpose IO. Push-pull output
REG25	E1	P	Regulator output and bq27741-G1 processor power. Decouple with 1-µF ceramic capacitor to V_{SS}.
SCL	E3	IO	Slave I^2C serial communications clock input line for communication with system. Use with 10-kΩ pullup resistor (typical).
SDA	C3	IO	Slave I^2C serial communications data line for communication with system. Open-drain I/O. Use with 10-kΩ pullup resistor (typical).
SRN	B1	IA	Analog input pin connected to the internal coulomb counter where SRN is nearest the CELL+ connection. Connect to sense resistor.
SRP	A1	IA	Analog input pin connected to the internal coulomb counter where SRP is nearest the PACK+ connection. Connect to sense resistor.
VPWR	C1	P	Power input. Decouple with 0.1-µF ceramic capacitor to V_{SS}.
VSS	D1	P	Device ground
TS	E2	IA	Pack thermistor voltage sense (use 103AT-type thermistor). ADC input

(1) IO = Digital input-output, IA = Analog input, P = Power connection, O = Output

Table 1. Default Configuration

OVERVOLTAGE PROTECTION (V_{OVP})	UNDERVOLTAGE PROTECTION (V_{UVP})	OVERCURRENT IN DISCHARGE (V_{OCD})	OVERCURRENT IN CHARGE (V_{OCC})	SHORT CIRCUIT IN DISCHARGE (V_{scd})
4.390 V	2.407 V	34.4 mV	20 mV	74.6 mV

OVERVOLTAGE PROTECTION DELAY (t_{OVP})	UNDERVOLTAGE PROTECTION DELAY (t_{UVP})	OVERCURRENT IN DISCHARGE DELAY (t_{OCD})	OVERCURRENT IN CHARGE DELAY (t_{OCC})	SHORT CIRCUIT IN DISCHARGE DELAY (t_{scd})
1 s	31.25 ms	31.25 ms	7.8125 ms	312.5 µs

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{VPWR}	Power input	–0.3	5.5	V
V_{REG25}	Supply voltage	–0.3	2.75	V
V_{PACKP}	PACKP input pin	–0.3	5.5	V
	PACK+ input when external 2-kΩ resistor is in series with PACKP input pin (see (1))	–0.3	28	V
V_{OUT}	Voltage output pins (DSG, CHG)	–0.3	10	V
V_{IOD1}	Push-pull IO pins (RC2)	–0.3	2.75	V
V_{IOD2}	Open-drain IO pins (SDA, SCL, HDQ, NC)	–0.3	5.5	V
V_{BAT}	BAT input pin	–0.3	5.5	V
V_I	Input voltage to all other pins (SRP, SRN)	–0.3	5.5	V
V_{TS}	Input voltage for TS	–0.3	2.75	V
T_A	Operating free-air temperature	–40	85	°C
T_F	Functional temperature	–40	100	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

T_A = 25°C, C_{REG25} = 1.0 µF, and V_{VPWR} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
V_{VPWR}	Supply voltage	No operating restrictions	2.8		5	V
		No FLASH writes	2.45		2.8	
C_{VPWR}	External input capacitor for internal LDO between VPWR and V_{SS}	Nominal capacitor values specified. Recommend a 5% ceramic X5R type capacitor located close to the device.		0.1		µF
C_{REG25}	External output capacitor for internal LDO between REG25 and V_{SS}		0.47	1		µF
I_{CC}	Normal operating mode current(1)(2) (VPWR)	Fuel gauge in NORMAL mode. I_{LOAD} > ***Sleep Current*** with charge pumps on (FETs on)		167		µA
I_{SLP}	SLEEP mode current(1)(2) (VPWR)	Fuel gauge in SLEEP+ mode. I_{LOAD} < ***Sleep Current*** with charge pumps on (FETs on)		88		µA
$I_{FULLSLP}$	FULLSLEEP mode current(1)(2) (VPWR)	Fuel gauge in SLEEP mode. I_{LOAD} < ***Sleep Current*** with charge pumps on (FETs on)		40		µA
$I_{SHUTDOWN}$	Shutdown mode current(1)(2) (VPWR)	Fuel gauge in SHUTDOWN mode. UVP tripped with fuel gauge and protector turned off (FETs off) V_{VPWR} = 2.5 V T_A = 25°C		0.1	0.2	µA
		T_A = –40°C to 85°C			0.5	µA
V_{OL}	Output voltage low (SCL, SDA, HDQ, NC, RC2)	I_{OL} = 1 mA			0.4	V
$V_{OH(OD)}$	Output voltage high (SDA, SCL, HDQ, NC, RC2)	External pullup resistor connected to V_{REG25}	V_{REG25} – 0.5			V
V_{IL}	Input voltage low (SDA, SCL, HDQ, NC)		–0.3		0.6	V
$V_{IH(OD)}$	Input voltage high (SDA, SCL, HDQ, NC)		1.2		5.5	V
V_{A1}	Input voltage range (TS)		V_{SS} – 0.125		2	V
V_{A2}	Input voltage range (BAT)		V_{SS} – 0.125		5	V
V_{A3}	Input voltage range (SRP, SRN)		V_{VPWR} – 0.125		V_{VPWR} + 0.125	V
I_{lkg}	Input leakage current (I/O pins)				0.3	µA
t_{PUCD}	Power-up communication delay			250		ms

(1) All currents are specified as charge pump on (FETs on).
(2) All currents are continuous average over 5-second period.

7.4 Thermal Information

THERMAL METRIC(1)		bq27741-G1 YZF [DSBGA] 15 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17	
$R_{\theta JB}$	Junction-to-board thermal resistance	20	
ψ_{JT}	Junction-to-top characterization parameter	1	
ψ_{JB}	Junction-to-board characterization parameter	18	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Power-On Reset

T_A = 25°C, C_{REG25} = 1.0 µF, and V_{VPWR} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Increasing battery voltage input at V_{REG25}		2.09	2.20	2.31	V
V_{HYS}	Power-on reset hysteresis			115		mV

7.6 2.5-V LDO Regulator(1)

T_A = 25°C, C_{REG25} = 1.0 µF, and V_{VPWR} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REG25}	Regulator output voltage	2.8 V ≤ V_{VPWR} ≤ 4.5 V, I_{OUT}(1) ≤ 16 mA	T_A = –40°C to 85°C	2.3	2.5	2.6	V
		2.45 V ≤ V_{VPWR} < 2.8 V (low battery), I_{OUT}(1) ≤ 3 mA		2.3			V
I_{SHORT} (2)	Short-circuit current limit	V_{REG25} = 0 V	T_A = –40°C to 85°C			250	mA

(1) LDO output current, I_{OUT}, is the sum of internal and external load currents.
(2) Assured by characterization. Not production tested.

7.7 Charger Attachment and Removal Detection

T_A = 25°C, C_{REG25} = 1.0 µF, and V_{VPWR} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CHGATT}	Voltage threshold for charger attachment detection			2.7	3	V
V_{CHGREM}	Voltage threshold for charger removal detection		0.5	1		V

7.8 Voltage Doubler

T_A = 25°C, C_{REG25} = 1.0 µF, and V_{VPWR} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FETON}	CHG and DSG FETs on	I_L = 1 µA, T_A = –40°C to 85°C	2 × V_{VPWR} – 0.4	2 × V_{VPWR} – 0.2	2 × V_{VPWR}	V
V_{FETOFF}	CHG and DSG FETs off	T_A = –40°C to 85°C			0.2	V
$V_{FETRIPPLE}$(1)	CHG and DSG FETs on	I_L = 1 µA, T_A = –40°C to 85°C			0.1	V_{PP}
t_{FETON}	FET gate rise time (10% to 90%)	C_L = 4 nF, T_A = –40°C to 85°C, No series resistance	67	140	218	µs
t_{FETOFF}	FET gate fall time (90% to 10%)	C_L = 4 nF, T_A = –40°C to 85°C, No series resistance	10	30	60	µs

(1) Assured by characterization. Not production tested.

7.9 Overvoltage Protection (OVP)

T_A = 25°C and C_{REG25} = 1.0 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP}	OVP detection voltage threshold	T_A = 25°C	V_{OVP} – 0.006	V_{OVP}	V_{OVP} + 0.006	V
		T_A = 0°C to 25°C	V_{OVP} – 0.023	V_{OVP}	V_{OVP} + 0.020	
		T_A = 25°C to 50°C	V_{OVP} – 0.018	V_{OVP}	V_{OVP} + 0.014	
		T_A = –40°C to 85°C	V_{OVP} – 0.053	V_{OVP}	V_{OVP} + 0.035	
V_{OVPREL}	OVP release voltage	T_A = 25°C	V_{OVPREL} – 0.012	V_{OVP} – 0.215	V_{OVPREL} + 0.012	V
		T_A = 0°C to 25°C	V_{OVPREL} – 0.023	V_{OVP} – 0.215	V_{OVPREL} + 0.020	
		T_A = 25°C to 50°C	V_{OVPREL} – 0.018	V_{OVP} – 0.215	V_{OVPREL} + 0.014	
		T_A = –40°C to 85°C	V_{OVPREL} – 0.053	V_{OVP} – 0.215	V_{OVPREL} + 0.035	

Overvoltage Protection (OVP) (continued)

T_A = 25°C and C_{REG25} = 1.0 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVP}	OVP delay time	T_A = –40°C to 85°C	t_{OVP} – 5%	t_{OVP}	t_{OVP} + 5%	s

7.10 Undervoltage Protection (UVP)

T_A = 25°C and C_{REG25} = 1.0 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVP}	UVP detection voltage threshold	T_A = 25°C	V_{UVP} – 0.012	V_{UVP}	V_{UVP} + 0.012	V
		T_A = –5°C to 50°C	V_{UVP} – 0.020	V_{UVP}	V_{UVP} + 0.020	
		T_A = –40°C to 85°C	V_{UVP} – 0.040	V_{UVP}	V_{UVP} + 0.040	
V_{UVPREL}	UVP release voltage	T_A = 25°C	V_{UVPREL} – 0.012	V_{UVP} + 0.105	V_{UVPREL} + 0.012	V
		T_A = –5°C to 50°C	V_{UVPREL} – 0.020	V_{UVP} + 0.105	V_{UVPREL} + 0.020	
		T_A = –40°C to 85°C	V_{UVPREL} – 0.040	V_{UVP} + 0.105	V_{UVPREL} + 0.040	
t_{UVP}	UVP delay time	T_A = –40°C to 85°C	t_{UVP} – 5%	t_{UVP}	t_{UVP} + 5%	ms

7.11 Overcurrent in Discharge (OCD)

T_A = 25°C, C_{REG25} = 1.0 µF, and V_{VPWR} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OCD}	OCD detection voltage threshold	T_A = 25°C $V_{SRN} – V_{SRP}$	V_{OCD} – 3	V_{OCD}	V_{OCD} + 3	mV
		T_A = –20°C to 60°C $V_{SRN} – V_{SRP}$	V_{OCD} – 3.785	V_{OCD}	V_{OCD} + 3.785	
		T_A = –40°C to 85°C $V_{SRN} – V_{SRP}$	V_{OCD} – 4.16	V_{OCD}	V_{OCD} + 4.16	
t_{OCD}	OCD delay time	T_A = –40°C to 85°C	t_{OCD} – 5%	t_{OCD}	t_{OCD} + 5%	ms

7.12 Overcurrent in Charge (OCC)

T_A = 25°C, C_{REG25} = 1.0 µF, and V_{VPWR} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OCC}	OCC detection voltage threshold	T_A = 25°C $V_{SRP} – V_{SRN}$	V_{OCC} – 3	V_{OCC}	V_{OCC} + 3	mV
		T_A = –20°C to 60°C $V_{SRP} – V_{SRN}$	V_{OCC} – 3.49	V_{OCC}	V_{OCC} + 3.49	
		T_A = –40°C to 85°C $V_{SRP} – V_{SRN}$	V_{OCC} – 3.86	V_{OCC}	V_{OCC} + 3.86	
t_{OCC}	OCC delay time	T_A = –40°C to 85°C	t_{OCC} – 5%	t_{OCC}	t_{OCC} + 5%	ms

7.13 Short-Circuit in Discharge (SCD)

T_A = 25°C, C_{REG25} = 1.0 µF, and V_{VPWR} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SCD}	SCD detection voltage threshold	T_A = 25°C $V_{SRN} – V_{SRP}$	V_{SCD} – 3	V_{SCD}	V_{SCD} + 3	mV
		T_A = –20°C to 60°C $V_{SRN} – V_{SRP}$	V_{SCD} – 4.5	V_{SCD}	V_{SCD} + 4.5	
		T_A = –40°C to 85°C $V_{SRN} – V_{SRP}$	V_{SCD} – 4.9	V_{SCD}	V_{SCD} + 4.9	
t_{SCD}	SCD delay time	T_A = –40°C to 85°C	t_{SCD} – 10%	t_{SCD}	t_{SCD} + 10%	µs

7.14 Low-Voltage Charging

T_A = 25°C, C_{REG25} = 1.0 µF, and V_{VPWR} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LVDET}	Voltage threshold for low-voltage charging detection	T_A = –40°C to 85°C	1.4	1.55	1.7	V

7.15 Internal Temperature Sensor Characteristics

T_A = –40°C to 85°C, 2.4 V < V_{REG25} < 2.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$G_{(TEMP)}$	Temperature sensor voltage gain			–2		mV/°C

7.16 Internal Clock Oscillators

2.4 V < V_{REG25} < 2.6 V; typical values at T_A = 25°C and V_{REG25} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Operating frequency			8.389		MHz
$f_{(LOSC)}$	Operating frequency			32.768		kHz

7.17 Integrating ADC (Coulomb Counter) Characteristics

T_A = –40°C to 85°C, 2.4 V < V_{REG25} < 2.6 V; typical values at T_A = 25°C and V_{REG25} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SR_IN}	Input voltage range, V_{SRN} and V_{SRP}	V_{SR} = V_{SRN} – V_{SRP}	V_{VPWR} – 0.125		V_{VPWR} + 0.125	V
t_{SR_CONV}	Conversion time	Single conversion		1		s
	Resolution		14		15	bits
V_{SR_OS}	Input offset			10		µV
INL	Integral nonlinearity error			±0.007%	±0.034%	FSR
Z_{SR_IN}	Effective input resistance(1)		7			MΩ
I_{SR_LKG}	Input leakage current(1)				0.3	µA

(1) Assured by design. Not production tested.

7.18 ADC (Temperature and Cell Voltage) Characteristics

T_A = –40°C to 85°C, 2.4 V < V_{REG25} < 2.6 V; typical values at T_A = 25°C and V_{REG25} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ADC_IN}	Input voltage range (VBAT channel)		V_{SS} – 0.125		5	V
	Input voltage range (other channels)		V_{SS} – 0.125		1	V
t_{ADC_CONV}	Conversion time				125	ms
	Resolution		14		15	bits
V_{ADC_OS}	Input offset			1		mV
Z_{ADC1}	Effective input resistance (TS) (1)		55			MΩ
Z_{ADC2}	Effective input resistance (BAT)(1)	Not measuring cell voltage	55			MΩ
		Measuring cell voltage		100		kΩ
I_{ADC_LKG}	Input leakage current(1)				0.3	µA

(1) Assured by design. Not production tested.

7.19 Data Flash Memory Characteristics

T_A = –40°C to 85°C, 2.4 V < V_{REG25} < 2.6 V; typical values at T_A = 25°C and V_{REG25} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Data retention(1)		10			years
	Flash programming write-cycles (1)		20,000			cycles
$t_{WORDPROG}$	Word programming time(1)				2	ms
I_{CCPROG}	Flash-write supply current(1)			5	10	mA

(1) Assured by design. Not production tested.

7.20 I²C-Compatible Interface Timing Characteristics

T_A = –40°C to 85°C, 2.4 V < V_{REG25} < 2.6 V; typical values at T_A = 25°C and V_{REG25} = 2.5 V (unless otherwise noted)

		MIN	TYP	MAX	UNIT
t_R	SCL or SDA rise time			300	ns
t_F	SCL or SDA fall time			300	ns
$t_{w(H)}$	SCL pulse width (high)	600			ns
$t_{w(L)}$	SCL pulse width (low)	1.3			µs
$t_{su(STA)}$	Setup for repeated start	600			ns
$t_{d(STA)}$	Start to first falling edge of SCL	600			ns
$t_{su(DAT)}$	Data setup time	100			ns
$t_{h(DAT)}$	Data hold time	0			ns
$t_{su(STOP)}$	Setup time for stop	600			ns
t_{BUF}	Bus free time between stop and start	66			µs
f_{SCL}	Clock frequency			400	kHz

7.21 HDQ Communication Timing Characteristics

T_A = –40°C to 85°C, 2.4 V < V_{REG25} < 2.6 V; typical values at T_A = 25°C and V_{REG25} = 2.5 V (unless otherwise noted)

		MIN	TYP	MAX	UNIT
$t_{(CYCH)}$	Cycle time, host to fuel gauge	190			µs
$t_{(CYCD)}$	Cycle time, fuel gauge to host	190	205	250	µs
$t_{(HW1)}$	Host sends 1 to fuel gauge	0.5		50	µs
$t_{(DW1)}$	Fuel gauge sends 1 to host	32		50	µs
$t_{(HW0)}$	Host sends 0 to fuel gauge	86		145	µs
$t_{(DW0)}$	Fuel gauge sends 0 to host	80		145	µs
$t_{(RSPS)}$	Response time, fuel gauge to host	190		950	µs
$t_{(B)}$	Break time	190			µs
$t_{(BR)}$	Break recovery time	40			µs
$t_{(RST)}$	HDQ reset	1.8		2.2	s
$t_{(RISE)}$	HDQ line rise time to logic 1 (1.2 V)			950	ns
$t_{(TRND)}$	Turnaround time (time from the falling edge of the last transmitted bit of 8-bit data and the falling edge of the next Break signal)	210			µs

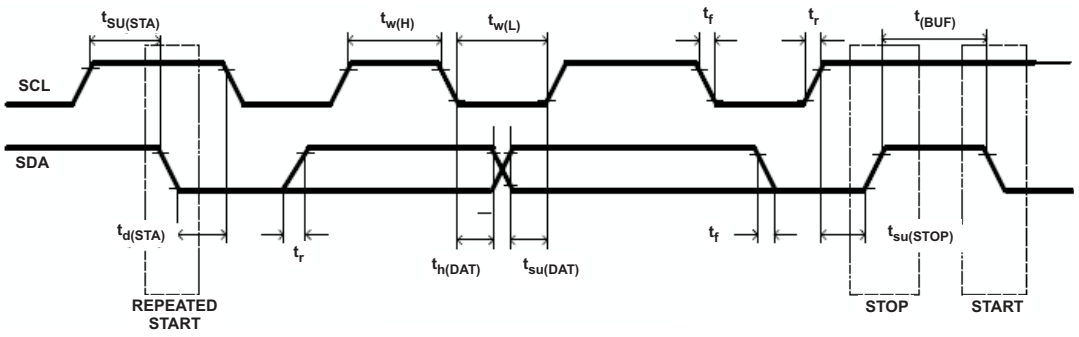
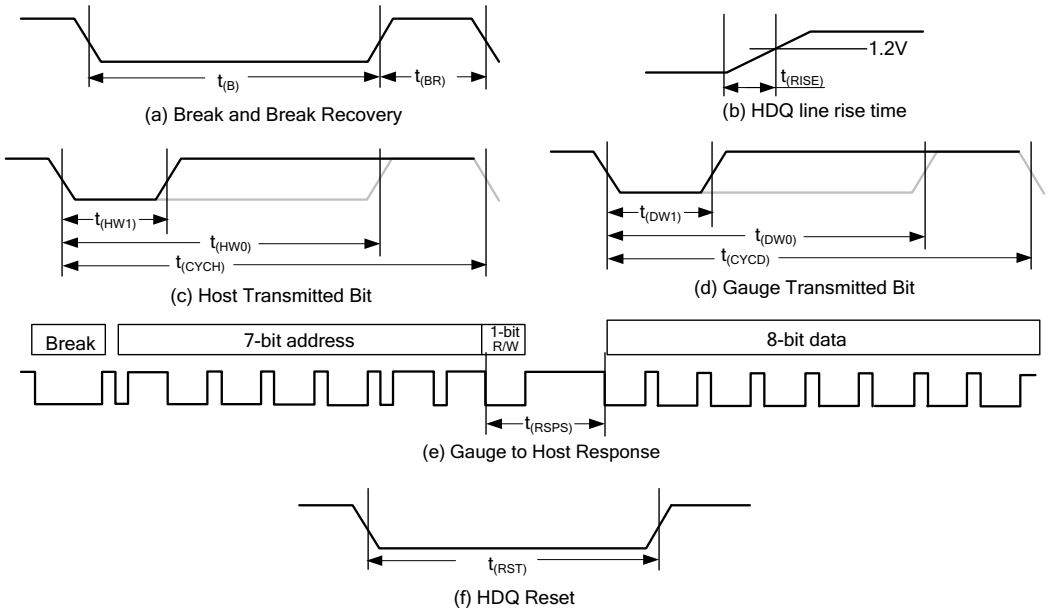


Figure 1. I²C-Compatible Interface Timing Diagrams



a. HDQ Breaking
b. Rise time of HDQ line
c. HDQ Host to fuel gauge communication
d. Fuel gauge to Host communication
e. Fuel gauge to Host response format
f. HDQ Host to fuel gauge

Figure 2. HDQ Timing Diagrams

7.22 Typical Characteristics

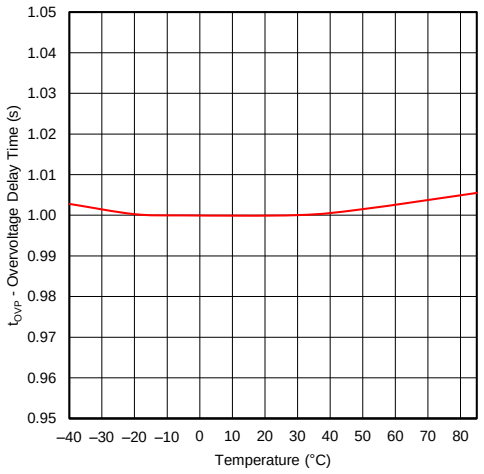


Figure 3. Overvoltage Delay Time

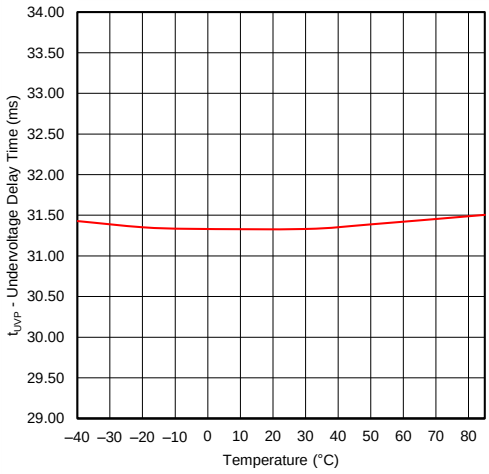


Figure 4. Undervoltage Delay Time

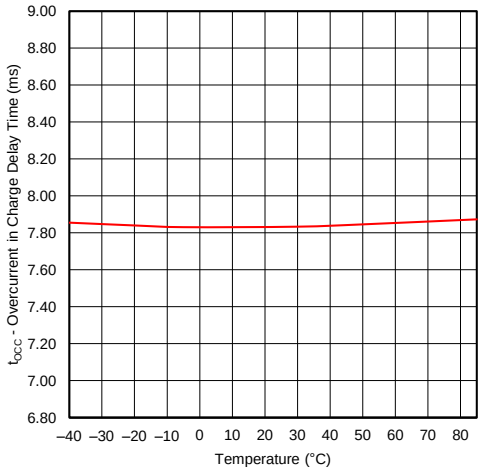


Figure 5. Overcurrent in Charge Delay Time

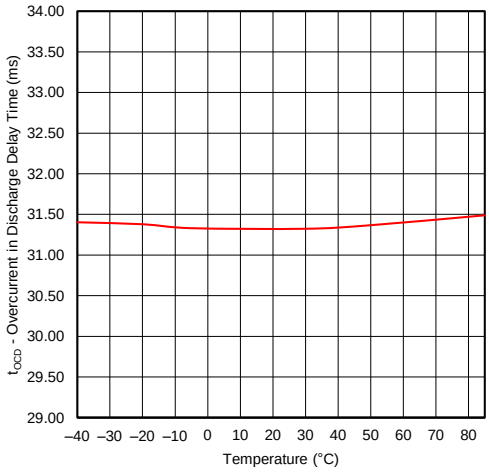


Figure 6. Overcurrent in Discharge Delay Time

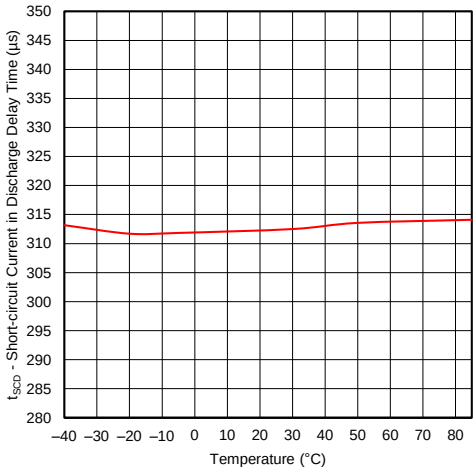


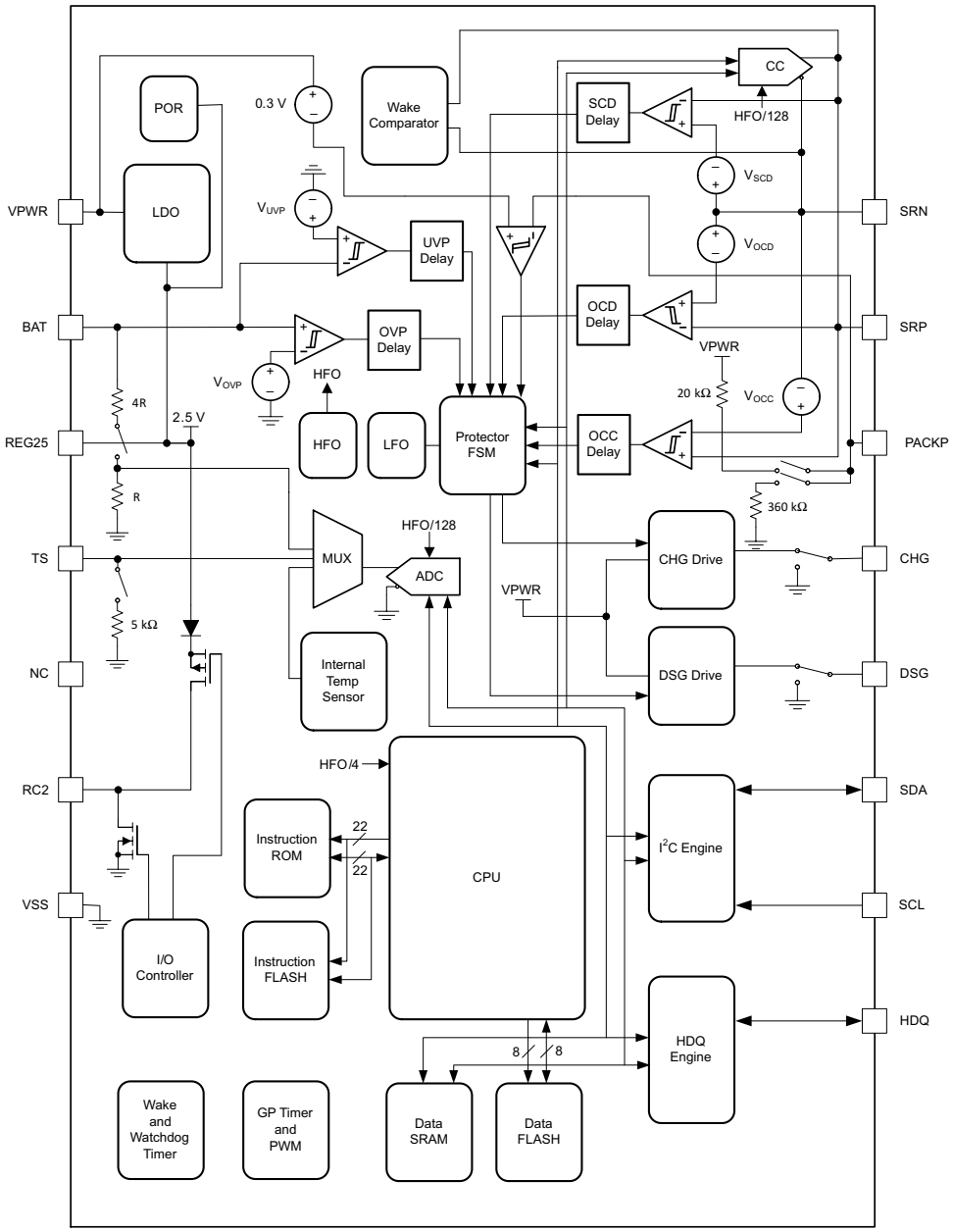
Figure 7. Short-Circuit Current in Discharge Delay Time

8 Detailed Description

8.1 Overview

The bq27741-G1 fuel gauge accurately predicts the battery capacity and other operational characteristics of a single Li-based rechargeable cell. It can be interrogated by a system processor to provide cell information, such as state-of-charge (SOC), time-to-empty (TTE), and time-to-full (TTF).

8.2 Functional Block Diagram



8.3 Feature Description

NOTE

Formatting Conventions in This Document:

Commands: *italics* with parentheses and no breaking spaces, for example, *RemainingCapacity()*.

Data Flash: *italics*, **bold**, and breaking spaces, for example, ***Design Capacity***.

Register Bits and Flags: brackets only, for example, [TDA]

Data Flash Bits: *italic* and **bold**, for example, ***[XYZ1]***

Modes and states: ALL CAPITALS, for example, UNSEALED mode.

8.3.1 Configuration

Cell information is stored in the fuel gauge in non-volatile flash memory. Many of these data flash locations are accessible during application development. They cannot, generally, be accessed directly during end-equipment operation. To access these locations, use individual commands, a sequence of data-flash-access commands, or the Battery Management Studio (bqStudio) Software. To access a desired data flash location, the correct data flash subclass and offset must be known. For more information on the data flash, see the *bq27741-G1 Pack-Side Impedance Track™ Battery Fuel Gauge With Integrated Protector and LDO User's Guide* (SLUUAA3).

The fuel gauge provides 96 bytes of user-programmable data flash memory, partitioned into two 64-byte blocks: ***Manufacturer Info Block A*** and ***Manufacturer Info Block B***. This data space is accessed through a data flash interface.

8.3.2 Fuel Gauging

The key to the high-accuracy gas gauging prediction is the Texas Instruments proprietary Impedance Track algorithm. This algorithm uses cell measurements, characteristics, and properties to create state-of-charge predictions that can achieve less than 1% error across a wide variety of operating conditions and over the lifetime of the battery.

See the *Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm Application Note* (SLUA364) for further details.

8.3.3 Wake-Up Comparator

The wake-up comparator indicates a change in cell current while the fuel gauge is in SLEEP mode. The wake comparator threshold can be configured in firmware and set to the thresholds in Table 2. An internal event is generated when the threshold is breached in either charge or discharge directions.

Table 2. I_{WAKE} Threshold Settings(1)

RSNS1	RSNS0	I_{WAKE}	Vth(SRP-SRN)
0	0	0	Disabled
0	0	1	Disabled
0	1	0	1 mV or –1 mV
0	1	1	2.2 mV or –2.2 mV
1	0	0	2.2 mV or –2.2 mV
1	0	1	4.6 mV or –4.6 mV
1	1	0	4.6 mV or –4.6 mV
1	1	1	9.8 mV or –9.8 mV

(1) The actual resistance value versus the setting of the sense resistor is not important—only the actual voltage threshold is important when calculating the configuration. The voltage thresholds are typical values under room temperature.

8.3.4 Battery Parameter Measurements

8.3.4.1 Charge and Discharge Counting

The integrating delta-sigma ADC gauges the charge or discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SRP and SRN pins. The integrating ADC measures bipolar signals and detects charge activity when $V_{SR} = V_{SRP} – V_{SRN}$ is positive and discharge activity when $V_{SR} = V_{SRP} – V_{SRN}$ is negative. The fuel gauge continuously integrates the signal over time using an internal counter.

8.3.4.2 Voltage

The fuel gauge updates cell voltages at 1-second intervals when in NORMAL mode. The internal ADC of the fuel gauge measures the voltage, and scales and calibrates it appropriately. Voltage measurement is automatically compensated based on temperature. This data is also used to calculate the impedance of the cell for Impedance Track fuel gauging.

8.3.4.3 Current

The fuel gauge uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a 5-mΩ to 20-mΩ typical sense resistor.

8.3.4.4 Auto-Calibration

The bq27741-G1 device provides an auto-calibration feature to cancel the voltage offset error across SRN and SRP for maximum charge measurement accuracy, and performs auto-calibration before entering the SLEEP mode.

8.3.4.5 Temperature

The fuel gauge external temperature sensing is optimized with the use of a high-accuracy negative temperature coefficient (NTC) thermistor with R25 = 10 kΩ ± 1% and B25/85 = 3435 kΩ ± 1% (such as Semitec 103AT for measurement). The fuel gauge can also be configured to use its internal temperature sensor. The fuel gauge uses temperature to monitor the battery-pack environment, which is used for fuel gauging and cell protection functionality.

8.3.5 Communications

8.3.5.1 HDQ Single-Pin Serial Interface

The HDQ interface is an asynchronous return-to-one protocol where a processor sends the command code to the fuel gauge. With HDQ, the least significant bit (LSB) of a data byte (command) or word (data) is transmitted first. The DATA signal on pin 12 is open-drain and requires an external pullup resistor. The 8-bit command code consists of two fields: the 7-bit HDQ command code (bits 0 through 6) and the 1-bit RW field (MSB bit 7). The RW field directs the fuel gauge to either one of the following:

- Store the next 8 bits of data to a specified register, or
- Output 8 bits of data from the specified register.

The HDQ peripheral can transmit and receive data as either an HDQ master or slave.

HDQ serial communication is normally initiated by the host processor sending a break command to the fuel gauge. A break is detected when the DATA pin is driven to a logic low state for a time $t_{(B)}$ or greater. The DATA pin then is returned to its normal ready logic high state for a time $t_{(BR)}$. The fuel gauge is now ready to receive information from the host processor.

The fuel gauge is shipped in the I^2C mode. TI provides tools to enable the HDQ peripheral.

8.3.5.2 HDQ Host Interruption

The default fuel gauge behaves as an HDQ slave-only device. If the HDQ interrupt function is enabled, the fuel gauge is capable of mastering and also communicating to a HDQ device. There is no mechanism for negotiating which is to function as the HDQ master, and care must be taken to avoid message collisions. The interrupt is signaled to the host processor with the fuel gauge mastering an HDQ message. This message is a fixed message that signals the interrupt condition. The message itself is 0x80 (slave write to register 0x00) with no data byte being sent as the command is not intended to convey any status of the interrupt condition. The HDQ interrupt function is not public and is only enabled by command.

When the SET_HDQINTEN subcommand is received, the fuel gauge detects any of the interrupt conditions and asserts the interrupt at 1-s intervals until either:

- The *CLEAR_HDQINTEN* subcommand is received, or
- The number of tries for interrupting the host has exceeded a predetermined limit. After the interrupt event, interrupts are automatically disabled. To re-enable interrupts, SET_HDQINTEN needs to be sent.

8.3.5.2.1 Low Battery Capacity

This feature works identically to SOC1. It uses the same data flash entries as SOC1 and triggers interrupts as long as SOC1 = 1 and HDQIntEN = 1.

8.3.5.2.2 Temperature

This feature triggers an interrupt based on the OTC (Overtemperature in Charge) or OTD (Overtemperature in Discharge) condition being met. It uses the same data flash entries as OTC or OTD and triggers interrupts as long as either the OTD or OTC condition is met and HDQIntEN = 1. (See details in *HDQ Host Interruption*.)

8.3.5.3 I²C Interface

The fuel gauge supports the standard I²C read, incremental read, one-byte write quick read, and functions. The 7-bit device address (ADDR) is the most significant 7 bits of the hex address and is fixed as 1010101. The 8-bit device address is therefore 0xAA or 0xAB for write or read, respectively.

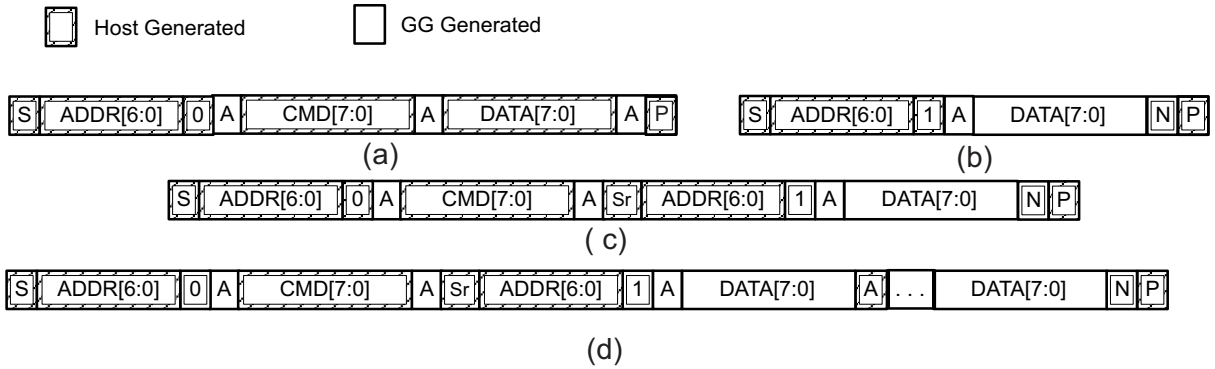
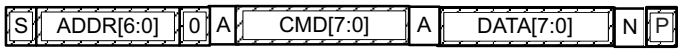


Figure 8. Supported I²C Formats

(a) 1-byte write
(b) Quick read
(c) 1-byte read
(d) Incremental read (S = Start, Sr = Repeated Start, A = Acknowledge, N = No Acknowledge, and P = Stop).

The quick read returns data at the address indicated by the address pointer. The address pointer, a register internal to the I²C communication engine, increments whenever data is acknowledged by the fuel gauge or the I²C master. Quick writes function in the same manner and are a convenient means of sending multiple bytes to consecutive command locations (such as two-byte commands that require two bytes of data).

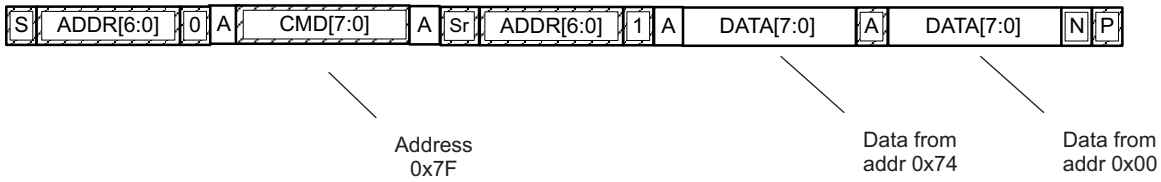
Attempt to write a read-only address (NACK after data sent by master):



Attempt to read an address above 0x7F (NACK command):

Attempt at incremental writes (NACK all extra data bytes sent):

Incremental read at the maximum allowed read address:



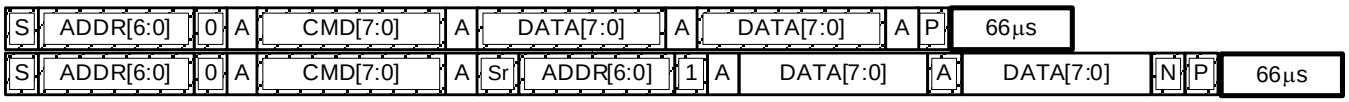
The I²C engine releases both SDA and SCL if the I²C bus is held low for $t_{(BUSERR)}$. If the fuel gauge was holding the lines, releasing them frees the master to drive the lines. If an external condition is holding either of the lines low, the I²C engine enters the low-power SLEEP mode.

8.3.5.3.1 I²C Time Out

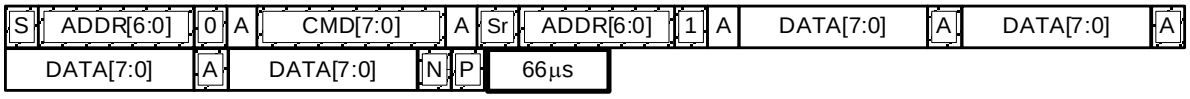
The I²C engine releases both SDA and SCL lines if the I²C bus is held low for about 2 seconds. If the fuel gauge was holding the lines, releasing them frees the master to drive the lines.

8.3.5.3.2 I²C Command Waiting Time

To ensure the correct results of a command with the 400-kHz I²C operation, a proper waiting time must be added between issuing a command and reading the results. For subcommands, the following diagram shows the waiting time required between issuing the control command and reading the status with the exception of the checksum command. A 100-ms waiting time is required between the checksum command and reading the result. For read-write standard commands, a minimum of 2 seconds is required to get the result updated. For read-only standard commands, there is no waiting time required, but the host must not issue any standard command more than two times per second. Otherwise, the gauge could result in a reset issue due to the expiration of the watchdog timer.



Waiting time between control subcommand and reading results



Waiting time between continuous reading results

Figure 9. I²C Command Waiting Time

The I²C clock stretch could happen in a typical application. A maximum 80-ms clock stretch could be observed during the flash updates. There is up to a 270-ms clock stretch after the OCV command is issued.

8.4 Device Functional Modes

To minimize power consumption, the fuel gauge has three power modes: NORMAL, SLEEP, and FULLSLEEP. The fuel gauge passes automatically between these modes, depending upon the occurrence of specific events, though a system processor can initiate some of these modes directly.

Device Functional Modes (continued)

8.4.1 NORMAL Mode

The fuel gauge is in NORMAL mode when not in any other power mode. During this mode, *AverageCurrent()*, *Voltage()*, and *Temperature()* measurements are taken, and the interface data set is updated. Decisions to change states are also made. This mode is exited by activating a different power mode.

Because the fuel gauge consumes the most power in NORMAL mode, the Impedance Track algorithm minimizes the time the fuel gauge remains in this mode.

8.4.2 SLEEP Mode

SLEEP mode performs *AverageCurrent()*, *Voltage()*, and *Temperature()* less frequently, which results in reduced power consumption. SLEEP mode is entered automatically if the feature is enabled (***Pack Configuration [SLEEP]*** = 1) and *AverageCurrent()* is below the programmable level ***Sleep Current***. Once entry into SLEEP mode has been qualified, but prior to entering it, the fuel gauge performs an ADC autocalibration to minimize offset.

During the SLEEP mode, the fuel gauge periodically takes data measurements and updates its data set. However, a majority of its time is spent in an idle condition.

The fuel gauge exits SLEEP if any entry condition is broken, specifically when either:

- *AverageCurrent()* rises above ***Sleep Current***, or
- A current in excess of I_{WAKE} through R_{SENSE} is detected.

8.4.3 FULLSLEEP Mode

FULLSLEEP mode turns off the high-frequency oscillator and performs *AverageCurrent()*, *Voltage()*, and *Temperature()* less frequently, which results in power consumption that is lower than that of the SLEEP mode.

FULLSLEEP mode can be enabled by two methods:

- Setting the ***[FULLSLEEP]*** bit in the Control Status register using the FULL_SLEEP subcommand and ***Full Sleep Wait Time (FS Wait)*** in data flash is set as 0.
- Setting the ***Full Sleep Wait Time (FS Wait)*** in data flash to a number larger than 0. This method is disabled when the ***FS Wait*** is set as 0.

FULLSLEEP mode is entered automatically when it is enabled by one of the methods above. When the first method is used, the gauge enters the FULLSLEEP mode when the fuel gauge is in SLEEP mode. When the second method is used, the FULLSLEEP mode is entered when the fuel gauge is in SLEEP mode and the timer counts down to 0.

The fuel gauge exits the FULLSLEEP mode when there is any communication activity. Therefore, the execution of SET_FULLSLEEP sets the ***[FULLSLEEP]*** bit. The FULLSLEEP mode can be verified by measuring the current consumption of the gauge.

During FULLSLEEP mode, the fuel gauge periodically takes data measurements and updates its data set. However, a majority of its time is spent in an idle condition.

The fuel gauge exits SLEEP if any entry condition is broken, specifically when either:

- *AverageCurrent()* rises above ***Sleep Current***, or
- A current in excess of I_{WAKE} through R_{SENSE} is detected.

While in FULLSLEEP mode, the fuel gauge can suspend serial communications by as much as 4 ms by holding the comm line(s) low. This delay is necessary to correctly process host communication, because the fuel gauge processor is mostly halted in SLEEP mode.

8.4.4 Battery Protector Description

The battery protector controls two external high-side N-channel FETs in a back-to-back configuration for battery protection. The protector uses two voltage doublers to drive the CHG and DSG FETs on.

Device Functional Modes (continued)

8.4.4.1 High-Side N-Channel FET Charge and Discharge FET Drive

The CHG or DSG FET is turned on by pulling the FET gate input up to V_{FETON}. The FETs are turned off by pulling the FET gate input down to V_{SS}. These FETs are automatically turned off by the protector based on the detected protection faults, or when commanded to turn off via the *FETTest*(0x74/0x75) extended command. Once the protection fault(s) is cleared, the FETs may be turned on again.

8.4.4.2 Operating Modes

The battery protector has several operating modes:

- Virtual SHUTDOWN mode
  - ANALOG SHUTDOWN
  - Low voltage charging
- UVP fault (POR state)
- NORMAL mode
- SHUTDOWN WAIT
- OCD or SCD FAULT mode
- OCC FAULT mode
- OVP FAULT mode

The relationships among these modes are shown in Figure 10.

Device Functional Modes (continued)

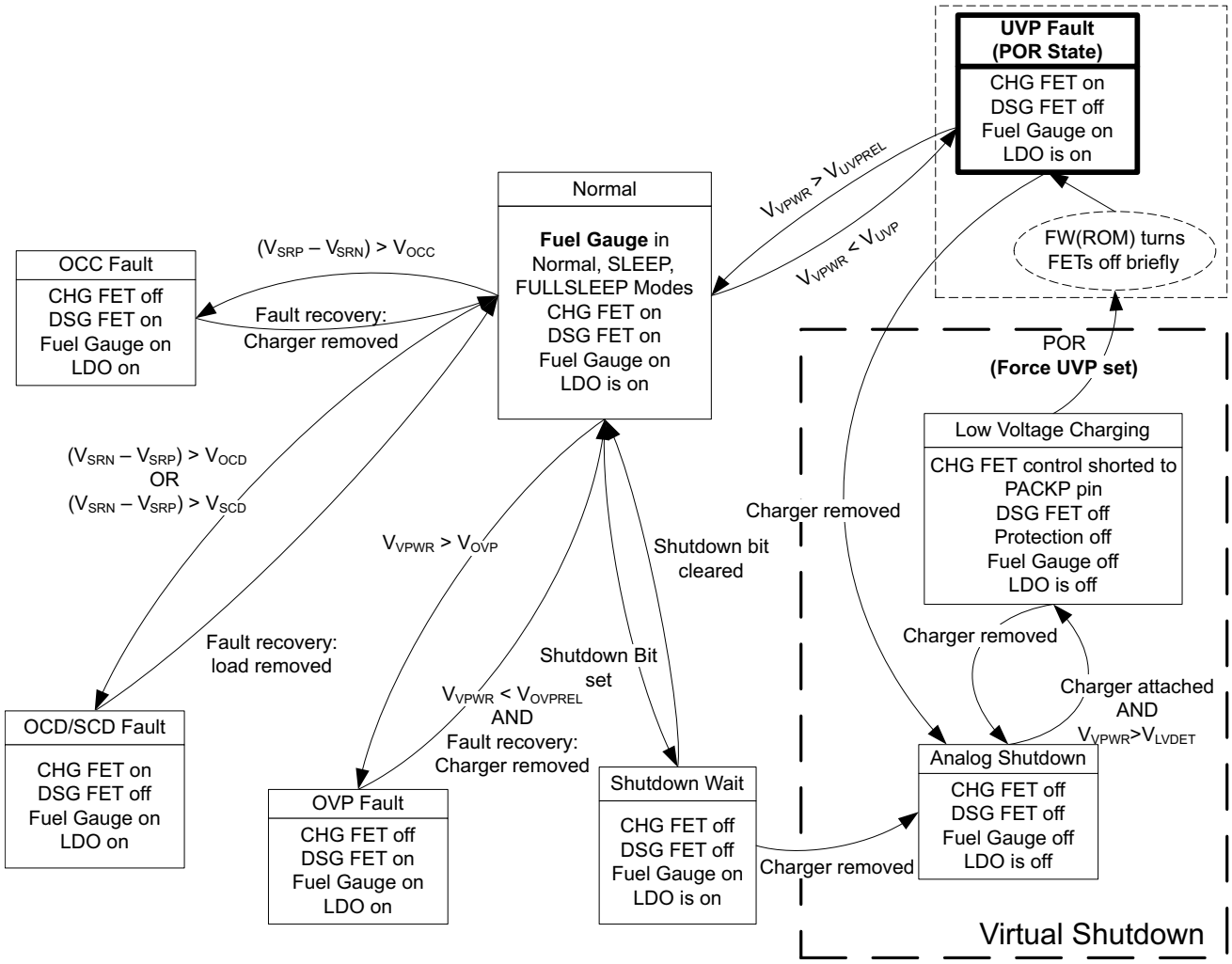


Figure 10. Operating Modes

8.4.4.2.1 VIRTUAL SHUTDOWN Mode

In this mode, the fuel gauge is not functional and only certain portions of analog circuitry are running to allow device wakeup from shutdown and low voltage charging.

8.4.4.2.1.1 ANALOG SHUTDOWN Mode

In this mode, the fuel gauge is not functional. Once the charger is connected, the fuel gauge determines if low voltage charging is allowed and then transitions to low voltage charging.

8.4.4.2.1.2 LOW-VOLTAGE CHARGING Mode

In this mode, the fuel gauge closes the CHG FET by shorting the gate to the PACKP pin. Low voltage charging continues until the cell voltage (V_{VPWR}) rises above the POR threshold.

8.4.4.2.2 UNDERVOLTAGE FAULT Mode

In this mode, the voltage on VPWR pin is below V_{UVP} and the charger is connected. As soon as the charger disconnects, the fuel gauge transitions into ANALOG SHUTDOWN mode to save power.

Device Functional Modes (continued)

The fuel gauge can enter this mode from LOW VOLTAGE CHARGING mode when the battery pack is being charged from a deeply discharged state or from NORMAL mode when the battery pack is being discharged below the allowed voltage.

When the battery pack is charged above V_{UVPREL}, the fuel gauge transitions to NORMAL mode.

8.4.4.2.3 NORMAL Mode

In this mode, the protector is fully powered and operational. Both CHG and DSG FETs are closed, while further operation is determined by the firmware. The protector is continuously checking for all faults.

The CHG or DSG FET may be commanded to be opened via the protector register by the firmware, but it does not affect protector operation or change the mode of operation.

Firmware can also command the fuel gauge to go into SHUTDOWN mode based on the command from the host. In this case, firmware sets the shutdown bit to indicate intent to go into SHUTDOWN mode. The fuel gauge then transitions to SHUTDOWN WAIT mode.

8.4.4.2.4 SHUTDOWN WAIT Mode

In this mode, the shutdown bit was set by the firmware and the fuel gauge initiated the shutdown sequence.

The shutdown sequence is as follows:

1. Open both CHG and DSG FETs.
2. Determine if any faults are set. If any faults are set, then go back to NORMAL mode.
3. Wait for charger removal. Once the charger is removed, turn off the LDO, which puts the fuel gauge into ANALOG SHUTDOWN mode.

8.4.4.2.5 OVERCURRENT IN DISCHARGE (OCD) and SHORT-CIRCUIT IN DISCHARGE (SCD) FAULT Mode

In this mode, a short-circuit in discharge (SCD) or overcurrent in discharge (OCD) protection fault is detected when the voltage across the sense resistor continuously exceeds the configured V_{OCD} or V_{SCD} thresholds for longer than the configured delay.

The fuel gauge enables the fault removal detection circuitry, which monitors load removal. A special high resistance load is switched on to monitor load presence. The OCD/SCD fault is cleared when the load is removed, which causes the fuel gauge to transition into NORMAL mode.

8.4.4.2.6 OVERCURRENT IN CHARGE (OCC) FAULT Mode

In this mode, an overcurrent in charge (OCC) protection fault is detected when the voltage across the sense resistor continuously exceeds the configured V_{OCC} for longer than the configured delay.

The fuel gauge enables the fault removal detection circuitry, which monitors the charger removal. The OCC fault is cleared once the charger voltage drops below the cell voltage by more than 300 mV, which causes the fuel gauge to transition to NORMAL mode.

8.4.4.2.7 OVERVOLTAGE PROTECTION (OVP) FAULT Mode

In this mode, an OVERVOLTAGE PROTECTION (OVP) fault mode is entered when the voltage on VPWR pin continuously exceeds the configured V_{OVP} threshold for longer than the configured delay.

The fuel gauge enables the fault removal detection circuitry, which monitors the charger removal. The OVP fault is cleared once the charger voltage drops below the cell voltage by more than 300 mV and the cell voltage drops below V_{OVPREL}, which causes the fuel gauge to transition to NORMAL mode.

8.4.4.3 Firmware Control of Protector

The firmware has control to open the CHG FET or DSG FET independently by overriding hardware control. However, it has no control to close the CHG FET or DSG FET and can only disable the FET override.

Device Functional Modes (continued)

8.4.5 OVERTEMPERATURE FAULT Mode

Overtemperature protection is implemented in firmware. Gauging firmware monitors temperature every second and opens the CHG and DSG FETs if *Temperature() > OT Prot Threshold* for *OT Prot Delay*. The CHG and DSG FETs override will be released when *Temperature() < OT Prot Recover*.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq27741-G1 device is a single-cell fuel gauge with integrated Li-Ion protection circuitry for highly accurate detection of overvoltage, undervoltage, overcurrent in charge, overcurrent in discharge, and short-circuit in discharge fault conditions. If the detected fault continues to be present for a specific delay time (pre-configured in the device), the protection front-end will disable the applicable charge pump circuit, resulting in opening of the FET until the provoking safety condition resolves. The integrated 16-bit delta-sigma converters provide accurate, high precision measurements for voltage, current, and temperature in order to accomplish effective battery monitoring, protection, and gauging. To allow for optimal performance in the end application, special considerations must be taken to ensure minimization of measurement error through proper printed circuit board (PCB) layout and correct configuration of battery characteristics in the fuel gauge data flash. Such requirements are detailed in *Design Requirements*.

9.2 Typical Applications

9.2.1 Pack-Side, Single-Cell Li-Ion Fuel Gauge and Protector

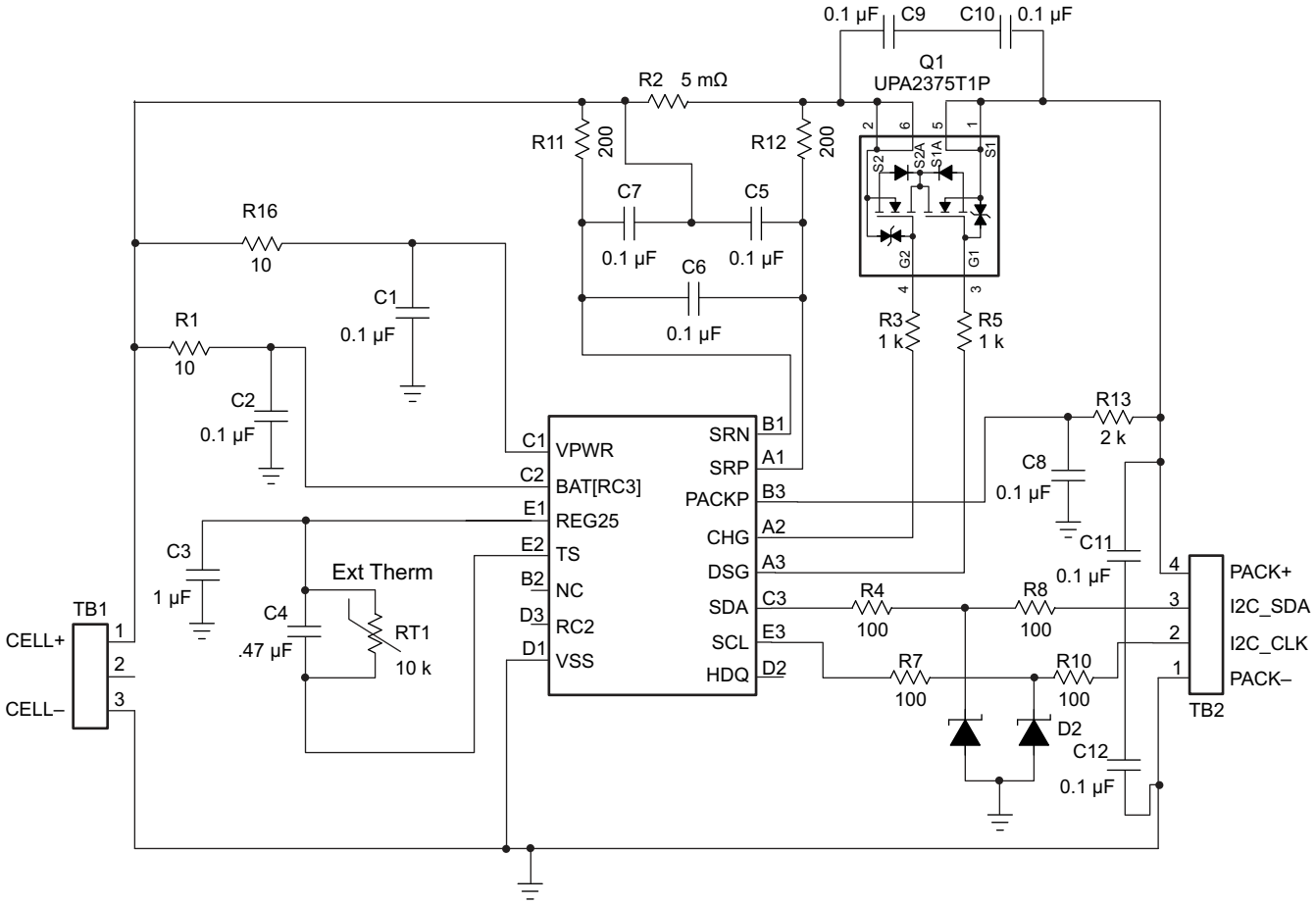


Figure 11. Typical Application Schematic, I²C Mode

Typical Applications (continued)

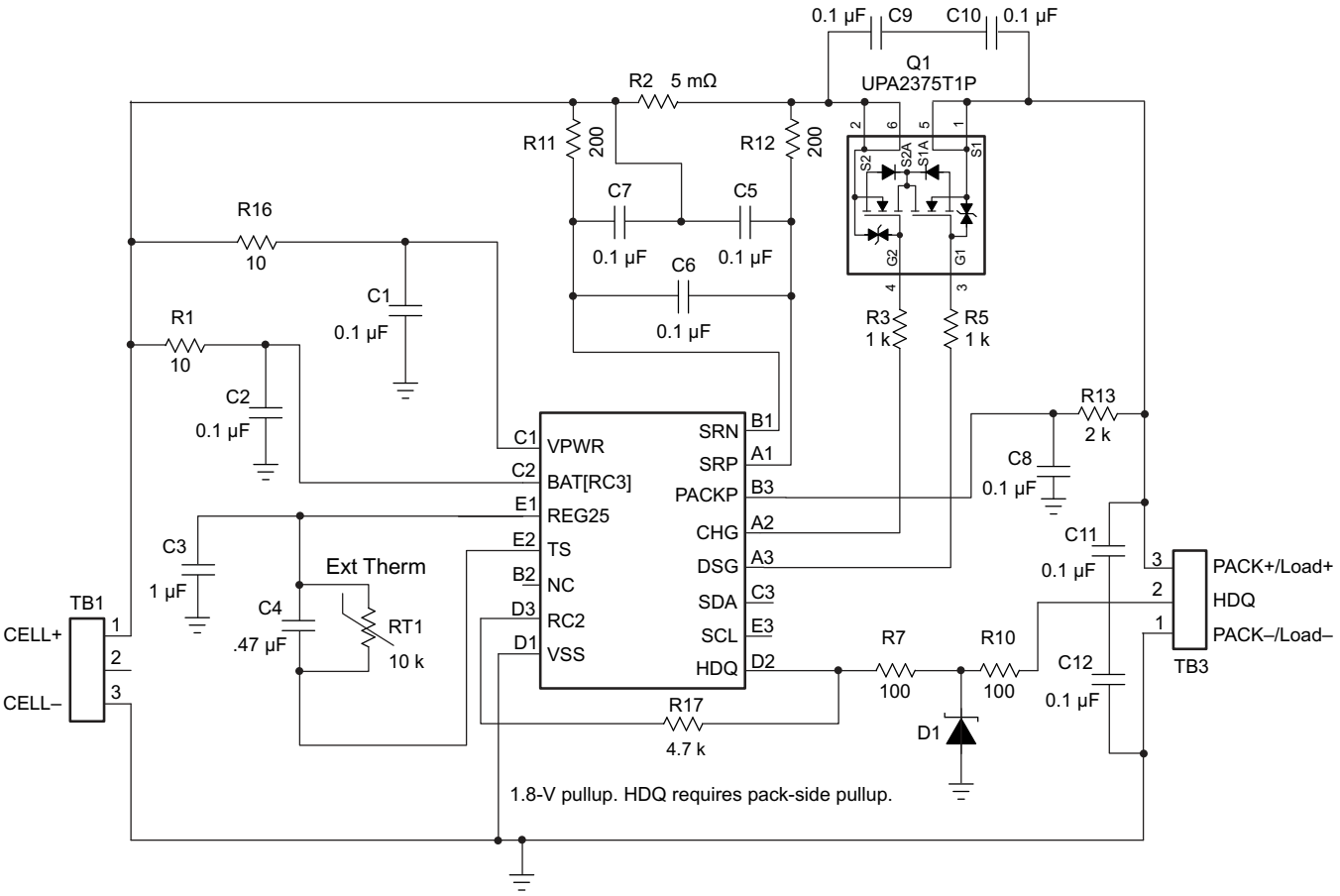


Figure 12. Typical Application Schematic, HDQ Mode

9.2.1.1 Design Requirements

Several key parameters must be updated to align with a given application's battery characteristics. For highest accuracy gauging, it is important to follow-up this initial configuration with a learning cycle to optimize resistance and maximum chemical capacity (Qmax) values prior to sealing and shipping packs to the field. Successful and accurate configuration of the fuel gauge for a target application can be used as the basis for creating a "golden" file that can be written to all production packs, assuming identical pack design and Li-Ion cell origin (chemistry, lot, and so on). Calibration data can be included as part of this golden file to cut down on battery pack production time. If using this method, it is recommended to average the calibration data from a large sample size and use these in the golden file.

NOTE

It is recommended to calibrate all packs individually as this will lead to the highest performance and lowest measurement error in the end application on a per-pack basis. In addition, the integrated protection functionality should be correctly configured to ensure activation based on the fault protection needs of the target pack design, or else accidental trip could be possible if using defaults.

Table 3 shows the items that should be configured to achieve reliable protection and accurate gauging with minimal initial configuration.

Typical Applications (continued)

Table 3. Key Data Flash Parameters for Configuration

NAME	DEFAULT	UNIT	RECOMMENDED SETTING
Design Capacity	1000	mAh	Set based on the nominal pack capacity as shown in the cell manufacturer's data sheet. If multiple parallel cells are used, should be set to N × Cell Capacity.
Design Energy	3800	mWh	Set based on the nominal pack energy (nominal cell voltage × nominal cell capacity) as shown in the cell manufacturer's data sheet. If multiple parallel cells are used, should be set to N × Cell Energy.
Design Energy Scale	1	—	Set to 10 to convert all power values to cWh or to 1 for mWh. ***Design Energy*** is divided by this value.
Reserve Capacity	0	mAh	Set to desired runtime remaining (in seconds/3600) × typical applied load between reporting 0% SOC and reaching ***Terminate Voltage***, if needed.
Design Voltage	3800	mV	Set to nominal cell voltage per manufacturer data sheet.
Cycle Count Threshold	900	mAh	Set to 90% of configured ***Design Capacity.***
Device Chemistry	0354	hex	Should be configured using TI-supplied Battery Management Studio (bqStudio) software. Default open-circuit voltage and resistance tables are also updated in conjunction with this step. Do not attempt to manually update reported Device Chemistry as this does not change all chemistry information. Always update chemistry using the appropriate software tool (that is, bqStudio).
Load Mode	1	—	Set to applicable load model, 0 for constant current or 1 for constant power.
Load Select	1	—	Set to load profile which most closely matches typical system load.
Qmax Cell 0	1000	mAh	Set to initial configured value for Design Capacity. The gauge will update this parameter automatically after the optimization cycle and for every regular Qmax update thereafter.
V at Chg Term	4350	mV	Set to nominal cell voltage for a fully charged cell. The gauge will update this parameter automatically each time full charge termination is detected.
Terminate Voltage	3000	mV	Set to empty point reference of battery based on system needs. Typical is between 3000 and 3200 mV.
Ra Max Delta	43	mΩ	Set to 15% of Cell0 R_a 4 resistance after an optimization cycle is completed.
Charging Voltage	4350	mV	Set based on nominal charge voltage for the battery in normal conditions (25°C, and so on). Used as the reference point for offsetting by ***Taper Voltage*** for full charge termination detection.
Taper Current	100	mA	Set to the nominal taper current of the charger + taper current tolerance to ensure that the gauge will reliably detect charge termination.
Taper Voltage	100	mV	Sets the voltage window for qualifying full charge termination. Can be set tighter to avoid or wider to ensure possibility of reporting 100% SOC in outer JEITA temperature ranges that use derated charging voltage.
Dsg Current Threshold	60	mA	Sets threshold for gauge detecting battery discharge. Should be set lower than minimal system load expected in the application and higher than ***Quit Current***.
Chg Current Threshold	75	mA	Sets the threshold for detecting battery charge. Can be set higher or lower depending on typical trickle charge current used. Also should be set higher than ***Quit Current***.
Quit Current	40	mA	Sets threshold for gauge detecting battery relaxation. Can be set higher or lower depending on typical standby current and exhibited in the end system.
Avg I Last Run	–299	mA	Current profile used in capacity simulations at onset of discharge or at all times if ***Load Select*** = 0. Should be set to nominal system load. Is automatically updated by the gauge every cycle.
Avg P Last Run	–1131	mW	Power profile used in capacity simulations at onset of discharge or at all times if ***Load Select*** = 0. Should be set to nominal system power. Is automatically updated by the gauge every cycle.
Sleep Current	15	mA	Sets the threshold at which the fuel gauge enters SLEEP mode. Take care in setting above typical standby currents else entry to SLEEP may be unintentionally blocked.
Shutdown V	0	mV	If auto-shutdown of fuel gauge is required prior to protect against accidental discharge to undervoltage condition, set this to desired voltage threshold for completely powering down the fuel gauge. Recovery occurs when a charger is connected.
OT Chg	55	°C	Set to desired temperature at which charging is prohibited to prevent cell damage due to excessive ambient temperature.

Typical Applications (continued)

Table 3. Key Data Flash Parameters for Configuration (continued)

NAME	DEFAULT	UNIT	RECOMMENDED SETTING
OT Chg Time	5	s	Set to desired time before CHG FET is disabled based on overtemperature. Since temperature changes much more slowly than other fault conditions, the default setting is sufficient for most application.
OT Chg Recovery	50	°C	Set to the temperature threshold at which charging is no longer prohibited.
OT Dsg	60	°C	Set to desired temperature at which discharging is prohibited to prevent cell damage due to excessive ambient temperature.
OT Dsg Time	5	s	Set to desired time before DSG FET is disabled based on overtemperature. Since temperature changes much more slowly than other fault conditions, the default setting is sufficient for most application.
OT Dsg Recovery	55	°C	Set to the temperature threshold at which cell discharging is no longer prohibited.
CC Gain	5	mΩ	Calibrate this parameter using TI-supplied bqStudio software and calibration procedure in the TRM. Determines conversion of coulomb counter measured sense resistor voltage to current.
CC Delta	5.074	mΩ	Calibrate this parameter using TI-supplied bqStudio software and calibration procedure in the TRM. Determines conversion of coulomb counter measured sense resistor voltage to passed charge.
CC Offset	6.874	mA	Calibrate this parameter using TI-supplied bqStudio software and calibration procedure in the TRM. Determines native offset of coulomb counter hardware that should be removed from conversions.
Board Offset	0.66	µA	Calibrate this parameter using TI-supplied bqStudio software and calibration procedure in the TRM. Determines native offset of the printed circuit board parasitics that should be removed from conversions.
Pack V Offset	0	mV	Calibrate this parameter using TI-supplied bqStudio software and calibration procedure in the TRM. Determines voltage offset between cell tab and ADC input node to incorporate back into or remove from measurement, depending on polarity.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 BAT Voltage Sense Input

A ceramic capacitor at the input to the BAT pin is used to bypass AC voltage ripple to ground, greatly reducing its influence on battery voltage measurements. It is most effective in applications with load profiles that exhibit high frequency current pulses (that is, cell phones), but is recommended for use in all applications to reduce noise on this sensitive high impedance measurement node.

The series resistor between the battery and the BAT input is used to limit current that could be conducted through the chip-scale package's solder bumps in the event of an accidental short during the board assembly process. The resistor is not likely to survive a sustained short condition (depends on power rating); however, it damages the much cheaper resistor component over suffering damage to the fuel gauge die itself.

9.2.1.2.2 SRP and SRN Current Sense Inputs

The filter network at the input to the coulomb counter is intended to improve differential mode rejection of voltage measured across the sense resistor. These components should be placed as close as possible to the coulomb counter inputs and the routing of the differential traces length-matched in order to best minimize impedance mismatch-induced measurement errors. The single-ended ceramic capacitors should be tied to the battery voltage node (preferably to a large copper pour connected to the SRN side of the sense resistor) in order to further improve common-mode noise rejection. The series resistors between the CC inputs and the sense resistor should be at least 200 Ω in order to mitigate SCR-induced latch-up due to possible ESD events.

9.2.1.2.3 Sense Resistor Selection

Any variation encountered in the resistance present between the SRP and SRN pins of the fuel gauge will affect the resulting differential voltage and derived current it senses. As such, it is recommended to select a sense resistor with minimal tolerance and temperature coefficient of resistance (TCR) characteristics. The standard recommendation based on best compromise between performance and price is a 1% tolerance, 50-ppm drift sense resistor with a 1-W power rating.

9.2.1.2.4 TS Temperature Sense Input

Similar to the BAT pin, a ceramic decoupling capacitor for the TS pin is used to bypass AC voltage ripple away from the high-impedance ADC input, minimizing measurement error. Another helpful advantage is that the capacitor provides additional ESD protection since most thermistors are handled and manually soldered to the PCB as a separate step in the factory production flow. It should be placed as close as possible to the respective input pin for optimal filtering performance.

9.2.1.2.5 Thermistor Selection

The fuel gauge temperature sensing circuitry is designed to work with a negative temperature coefficient-type (NTC) thermistor with a characteristic 10-kΩ resistance at room temperature (25°C). The default curve-fitting coefficients configured in the fuel gauge specifically assume a 103AT-2 type thermistor profile and so that is the default recommendation for thermistor selection purposes. Moving to a separate thermistor resistance profile (for example, JT-2 or others) requires an update to the default thermistor coefficients in data flash to ensure highest accuracy temperature measurement performance.

9.2.1.2.6 VPWR Power Supply Input Filtering

A ceramic capacitor is placed at the input to the fuel gauge's internal LDO in order to increase power supply rejection (PSR) and improve effective line regulation. It ensures that voltage ripple is rejected to ground instead of coupling into the device's internal supply rails.

9.2.1.2.7 REG25 LDO Output Filtering

A ceramic capacitor is also needed at the output of the internal LDO to provide a current reservoir for fuel gauge load peaks during high peripheral utilization. It acts to stabilize the regulator output and reduce core voltage ripple inside of the device.

9.2.1.2.8 Communication Interface Lines

A protection network composed of resistors and zener diodes is recommended on each of the serial communication inputs to protect the fuel gauge from serious ESD transients. The Zener should be selected to break down at a voltage larger than the typical pullup voltage for these lines but less than the internal diode clamp breakdown voltage of the device inputs (approximately 6 V). A zener voltage of 5.6 V is typically recommended. The series resistors are used to limit the current into the Zener diode and prevent component destruction due to thermal strain once it goes into breakdown. 100 Ω is typically recommended for these resistance values.

9.2.1.2.9 PACKP Voltage Sense Input

Inclusion of a 2-kΩ series resistor on the PACKP input allows it to tolerate a charger overvoltage event up to 28 V without device damage. The resistor also protects the device in the event of a reverse polarity charger input, since the substrate diode will be forward biased and attempt to conduct charger current through the fuel gauge (as well as the high FETs). An external reverse charger input FET clamp can be added to short the DSG FET gate to its source terminal, forcing the conduction channel off when negative voltage is present at PACK+ input to the battery pack and preventing large battery discharge currents. A ceramic capacitor connected at the PACKP pin helps to filter voltage into the comparator sense lines used for checking charger and load presence. In addition, in the LOW VOLTAGE CHARGING state, the minimal circuit elements that are operational are powered from this input pin and require a stable supply.

9.2.1.2.10 CHG and DSG Charge Pump Voltage Outputs

The series resistors used at the DSG and CHG output pins serve to protect them from damaging ESD events or breakdown conditions, allowing the resistors to be damaged in place of the fuel gauge itself. An added bonus is that they also help to limit in-rush currents due to use of FETs with large gate capacitance, allowing a smooth ramp of power-path connection turn-on to the system.

9.2.1.2.11 N-Channel FET Selection

The selection of N-channel FETs for a single-cell battery pack design depends on a variety of factors including package type, size, and device cost as well as performance metrics such as drain-to-source resistance (rDS(on)), gate capacitance, maximum current and power handling, and similar. At a minimum, it is recommended that the selected FETs have a drain-to-source voltage (VDS) and gate-to-source (VGS) voltage tolerance of 12 V. Some FETs are designed to handle as much as 24 V between the drain and source terminals and this would provide an increased safety margin for the pack design. Additionally, the DC current rating should be high enough to safely handle sustained current in charge or discharge direction just below the maximum threshold tolerances of the configured OCC and OCD protections and the lowest possible sense resistance value based on tolerance and TCR considerations, or vice-versa. This ensures that there is sufficient power dissipation margin given a worst-case scenario for the fault detections. In addition, striving for minimal FET resistance at the expected gate bias as well as lowest gate capacitance will help reduce conduction losses and increase power efficiency as well as achieve faster turn-on and turn-off times for the FETs. Many of these FETs are now offered as dual, back-to-back N-channel FETs in wafer-chip scale (WCSP) packaging, decreasing both BOM count and shrinking necessary board real estate to accommodate the components. Finally, refer to the safe operating area (SOA) curves of the target FETs to ensure that the boundaries are never violated based on all possible load conditions in the end application. The CSD83325L is an excellent example of a FET solution that meets all of the aforementioned criteria, offering rDS(on) of 10.3 mΩ and VDS of 12 V with back-to-back N-channel FETs in a chip-scale package, a perfect fit for battery pack designs.

9.2.1.2.12 Additional ESD Protection Components

The additional capacitors placed across the CHG and DSF FET source pins as well as between PACK+ and ground help to bolster and greatly improve the ESD robustness of the pack design. The former components shunt damaging transients around the FETs and the latter components attempt to bypass such pulses to PACK– before they couple further into the battery pack PCB. Two series capacitors are used for each of these protection areas to prevent a battery short in the event of a single capacitor failure.

9.2.1.3 Application Curves

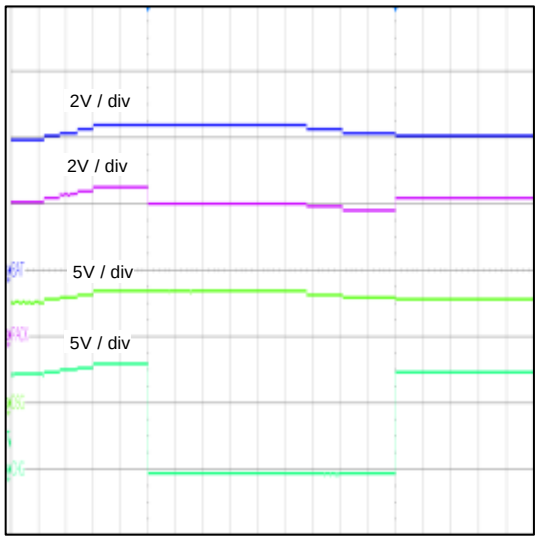


Figure 13. Overvoltage Protection Set and Clear

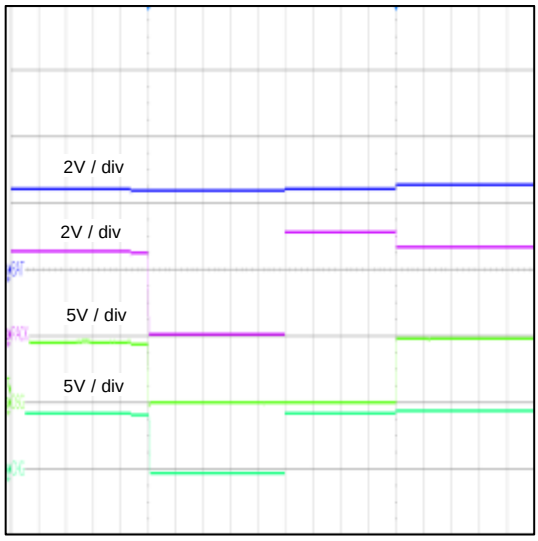


Figure 14. Undervoltage Protection Set and Clear

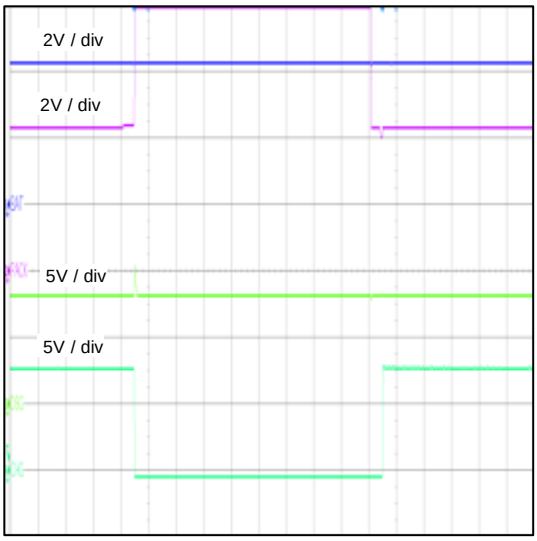


Figure 15. Overcurrent in Charge Protection Set and Clear

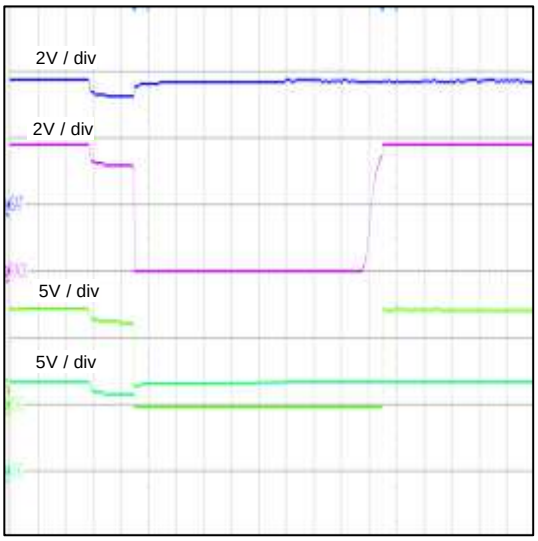


Figure 16. Overcurrent in Discharge Protection Set and Clear

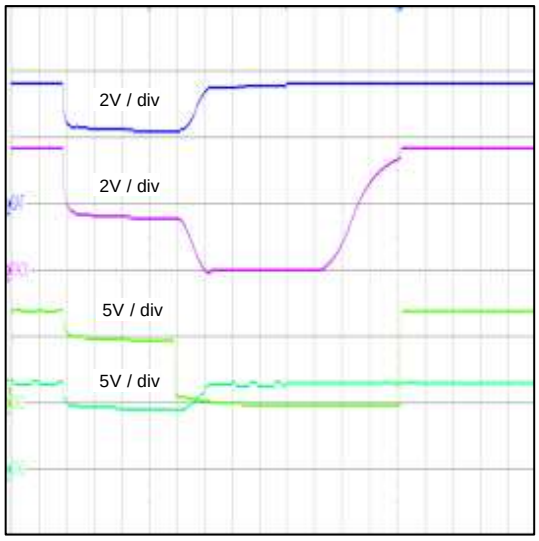


Figure 17. Short-Circuit in Discharge Protection Set and Clear

10 Power Supply Recommendations

10.1 Power Supply Decoupling

The VPWR input pin and the REG25 output pin require low equivalent series resistance (ESR) ceramic capacitors placed as closely as possible to the respective pins to optimize ripple rejection and to provide a stable and dependable power rail that is resilient to line transients. A 0.1-µF capacitor at the VPWR and a 1-µF capacitor at REG25 suffice for satisfactory device performance.

11 Layout

11.1 Layout Guidelines

11.1.1 Li-Ion Cell Connections

For the highest voltage measurement accuracy, it is important to connect the BAT pin directly to the battery terminal PCB pad. This avoids measurement errors caused by IR drops when high charge or discharge currents are flowing. Connecting directly at the positive battery terminal with a Kelvin connection ensures the elimination of parasitic resistance between the point of measurement and the actual battery terminal. Likewise, the low current ground return for the fuel gauge and all related passive components should be star-connected precisely at the negative battery terminal. This technique minimizes measurement error due to current-induced ground offsets and also improves noise performance through prevention of ground bounce that could occur with high current and low current returns intersecting ahead of the battery ground. The bypass capacitor for this sense line needs to be placed as close as possible to the BAT input pin.

11.1.2 Sense Resistor Connections

Kelvin connections at the sense resistor are as critical as those for the battery terminals themselves. The differential traces should be connected at the inside of the sense resistor pads and not anywhere along the high current trace path in order to prevent false increases to measured current that could result when measuring between the sum of the sense resistor and trace resistance between the tap points. In addition, the routing of these leads from the sense resistor to the input filter network and finally into the SRP and SRN pins needs to be as closely matched in length as possible or an additional measurement offset may occur. It is further recommended to add copper trace or pour-based "guard rings" around the perimeter of the filter network and coulomb counter inputs to shield these sensitive pins from radiated EMI into the sense nodes. This prevents differential voltage shifts that could be interpreted as real current change to the fuel gauge. All of the filter components need to be placed as close as possible to the coulomb counter inputs pins.

Layout Guidelines (continued)

11.1.3 Thermistor Connections

The thermistor sense input should include a ceramic bypass capacitor placed as close to the TS input pin as possible. The capacitor helps to filter measurements of any stray transients as the voltage bias circuit pulses periodically during temperature sensing windows.

11.1.4 FET Connections

The battery current transmission path through the FETs should be routed with large copper pours to provide the lowest resistance path possible to the system. Depending on package type, thermal vias can be placed in the package land pattern's thermal pad to reduce thermal impedance and improve heat dissipation from the package to the board, protecting the FETs during high system loading conditions. In addition, it is preferable to locate the FETs and other heat generating components away from the low power pack electronics to reduce the chance of temperature drift and associated impacts to data converter measurements. In the event of FET overheating, keeping reasonable distance between the most critical components, such as the fuel gauge, and the FETs helps to decrease the risk of thermal breakdown to the more fragile components.

11.1.5 ESD Component Connections

The ESD components included in the reference design that connect across the back-to-back FETs as well as from PACK+ to ground require trace connections that are as wide and short as possible in order to minimize loop inductance in their return path. This ensures impedance is lowest at the AC loop through the series capacitors and makes this route most attractive for ESD transients such that they are conducted away from the vulnerable low voltage, low power fuel gauge and passive components. The series resistors and Zener diodes connected to the serial communications lines should be placed as close as possible to the battery pack connector to keep large ESD currents confined to an area distant from the fuel gauge electronics. Further, all ESD components referred to ground should be single-point connected to the PACK– terminal if possible. This reduces the possibility of ESD coupling into other sensitive nodes well ahead of the PACK– ground return.

11.1.6 High Current and Low Current Path Separation

For best possible noise performance, it is important to separate the low current and high current loops to different areas of the board layout. The fuel gauge and all support components should be situated on one side of the board and tap off of the high current loop (for measurement purposes) at the sense resistor. Routing the low current ground around instead of under high current traces further helps to improve noise rejection. Finally, the high current path should be confined to a small loop from the battery, through the FETs, into the PACK connector, and back.

11.2 Layout Example

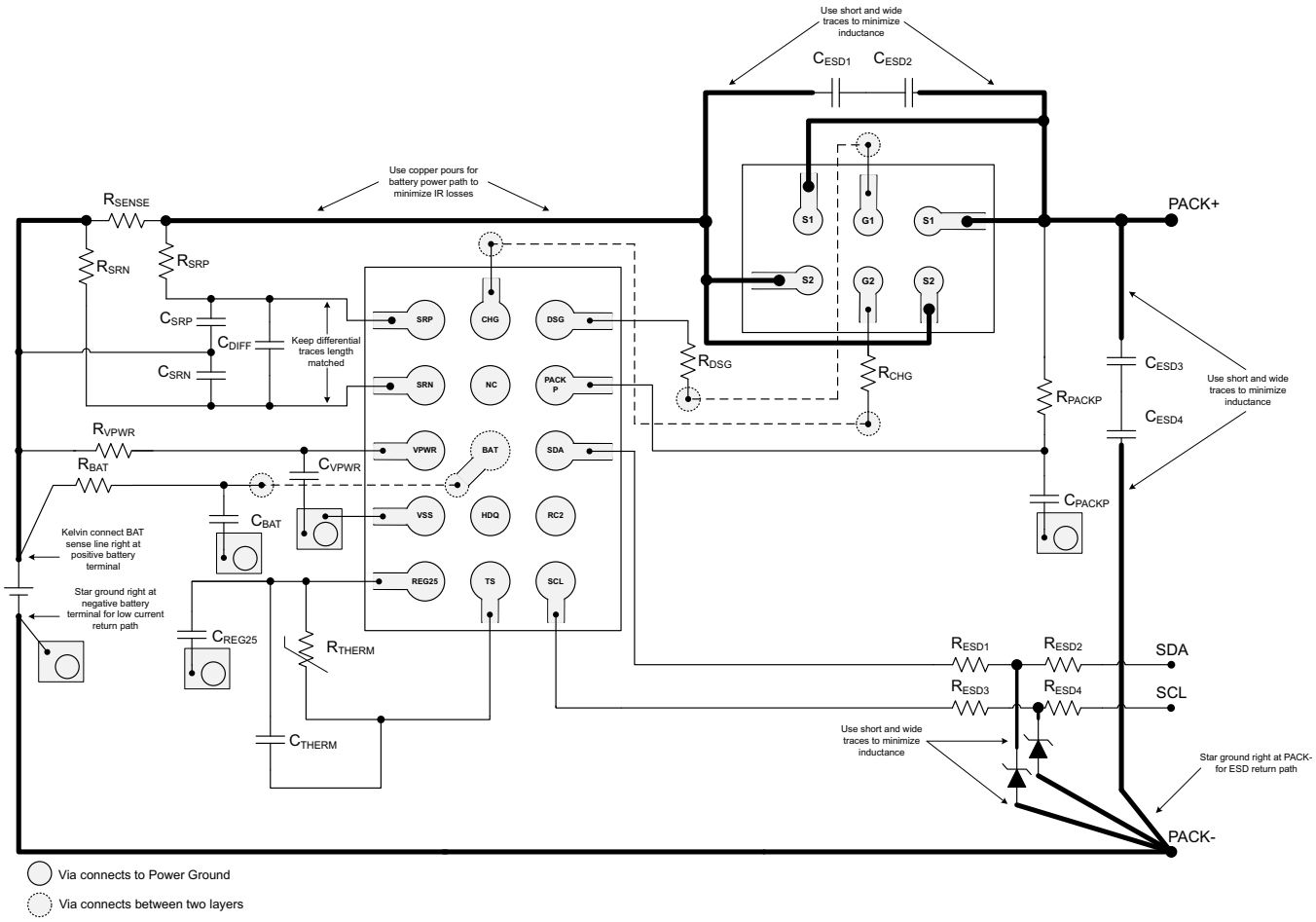


Figure 18. bq27741-G1 Board Layout

12 Device and Documentation Support

12.1 Device Support

For the Battery Management Studio (bqStudio) Software, go to http://www.ti.com/tool/bqstudio.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- *bq27741-G1 Pack-Side Impedance Track™ Battery Fuel Gauge with Integrated Protector and LDO User's Guide* (SLUUAA3)
- *bq27741 EVM Single Cell Impedance Track™ Technology Evaluation Module User's Guide* (SLUUAH1)

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

Impedance Track, NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ27741YZFR-G1	ACTIVE	DSBGA	YZF	15	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ27741-G1	Samples
BQ27741YZFT-G1	ACTIVE	DSBGA	YZF	15	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ27741-G1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

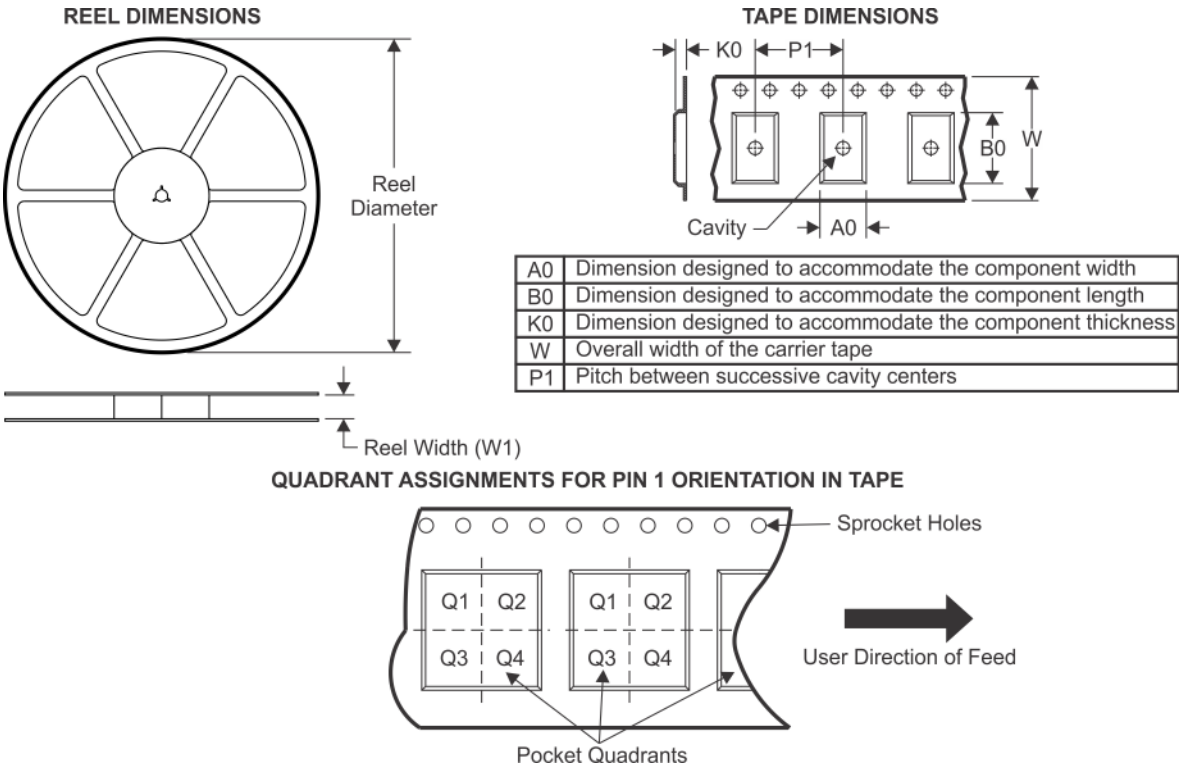
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

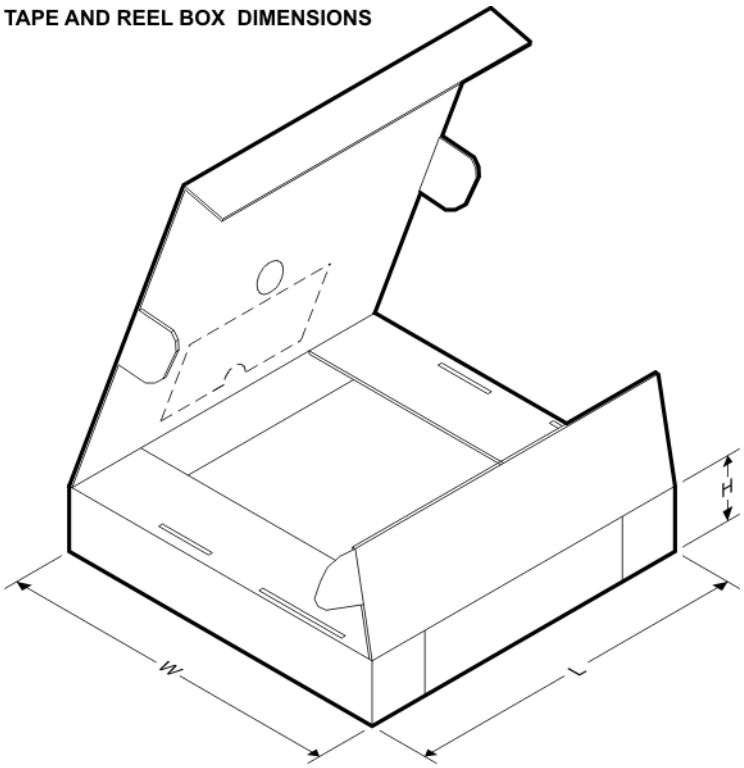


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ27741YZFR-G1	DSBGA	YZF	15	3000	180.0	8.4	2.06	2.88	0.69	4.0	8.0	Q1
BQ27741YZFT-G1	DSBGA	YZF	15	250	180.0	8.4	2.06	2.88	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

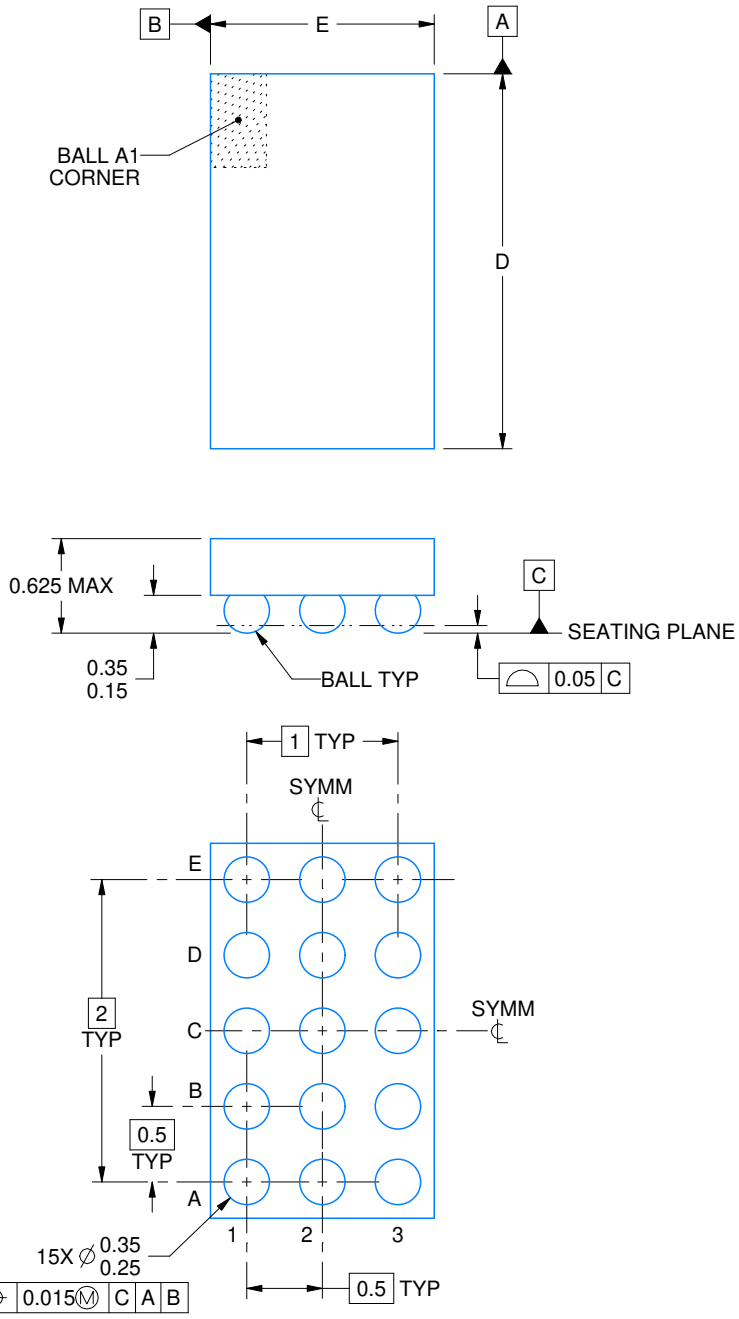
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ27741YZFR-G1	DSBGA	YZF	15	3000	182.0	182.0	20.0
BQ27741YZFT-G1	DSBGA	YZF	15	250	182.0	182.0	20.0

PACKAGE OUTLINE

YZF0015

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



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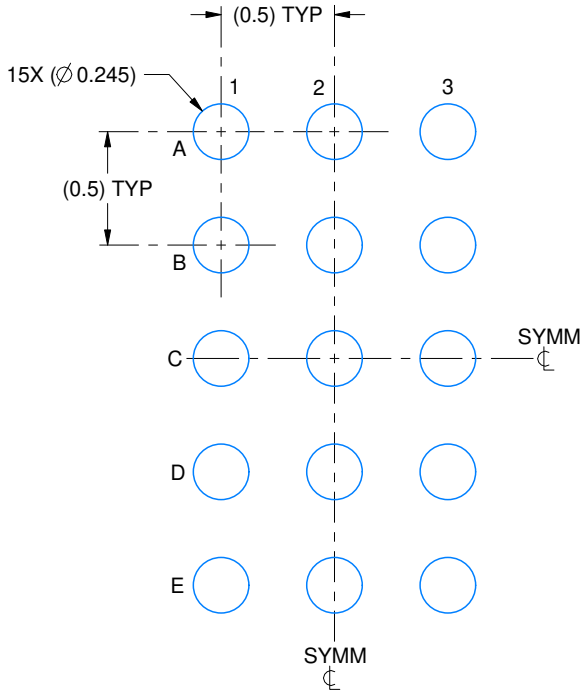
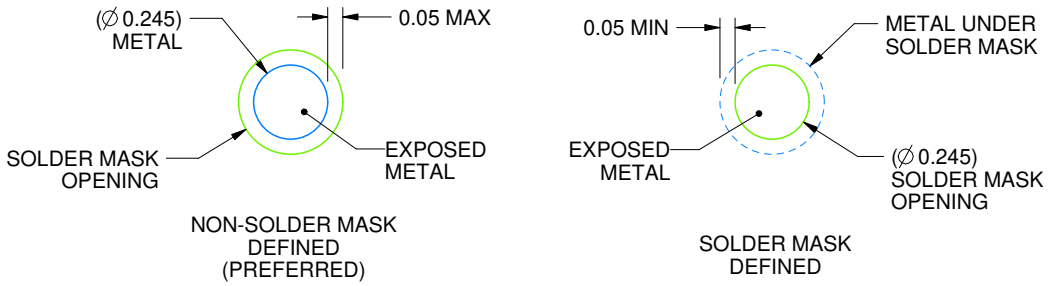
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

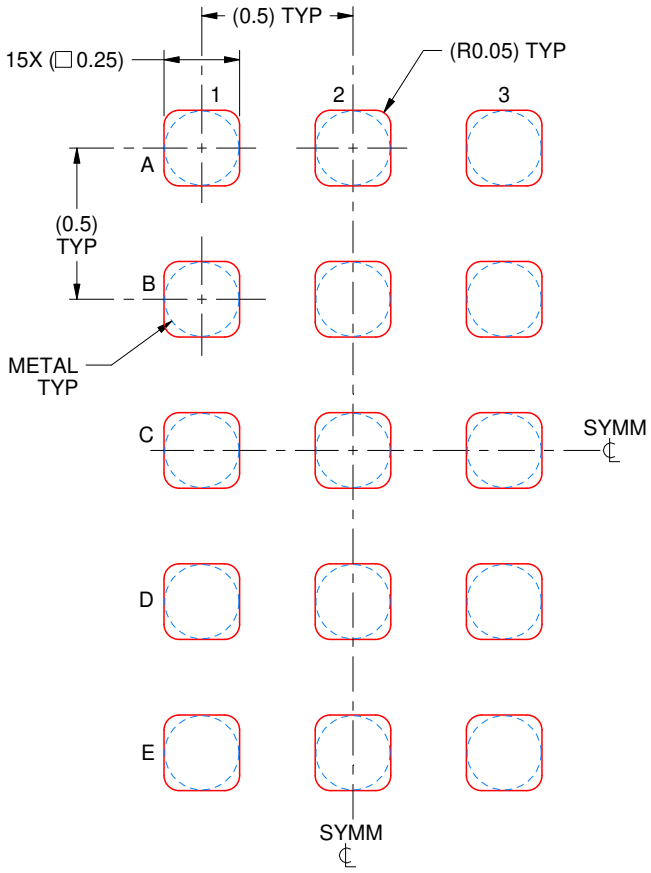
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZF0015

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219381/A 02/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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