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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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**SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE**

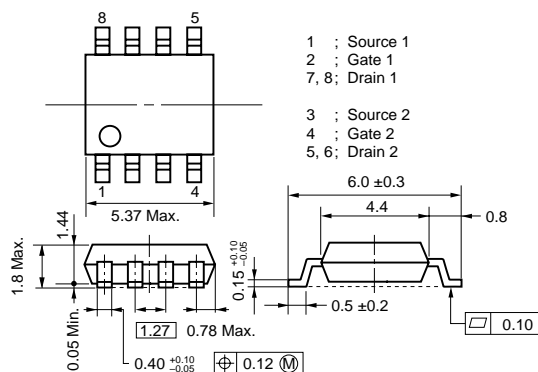
DESCRIPTION

The μPA1760 is N-Channel MOS Field Effect Transistor designed for DC/DC Converters and power management application of notebook computers.

FEATURES

- Dual Chip Type
- Low On-Resistance
 $R_{DS(on)1} = 26.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 4.0 \text{ A)}$
 $R_{DS(on)2} = 36.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 4.0 \text{ A)}$
 $R_{DS(on)3} = 42.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_D = 4.0 \text{ A)}$
- Low C_{iss} : $C_{iss} = 760 \text{ pF TYP.}$
- Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

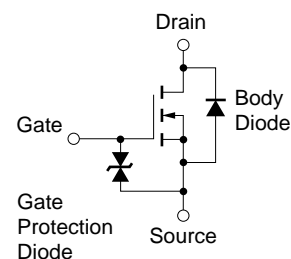
PACKAGE DRAWING (Unit : mm)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	30	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC)	I _{D(DC)}	±8.0	A
Drain Current (Pulse) ^{Note1}	I _{D(pulse)}	±32	A
Total Power Dissipation (1 unit) ^{Note2}	P _T	1.7	W
Total Power Dissipation (2 unit) ^{Note2}	P _T	2.0	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	-55 to + 150	°C
Single Avalanche Current ^{Note3}	I _{AS}	8	A
Single Avalanche Energy ^{Note3}	E _{AS}	6.4	mJ

**EQUIVALENT CIRCUIT
(1/2 Circuit)**



- Notes**
1. $PW \leq 10 \mu s$, Duty cycle $\leq 1\%$
 2. T_A = 25°C, Mounted on ceramic substrate of 2000 mm² x 1.6 mm
 3. Starting T_{ch} = 25°C, R_G = 25 Ω, V_{GS} = 20 V → 0 V

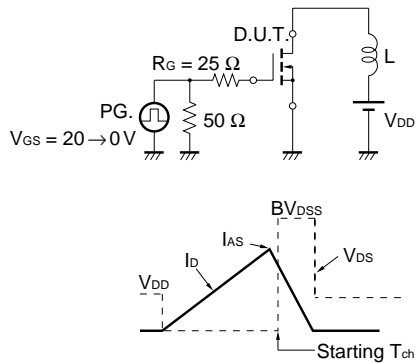
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage Exceeding the rated voltage may be applied to this device.

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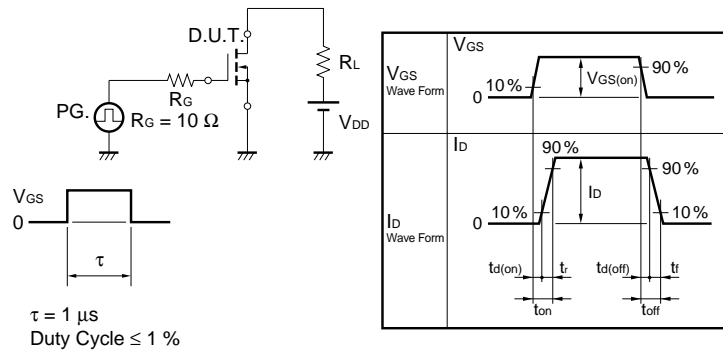
ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 4.0 A		20.5	26.0	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 4.0 A		27.0	36.0	mΩ
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 4.0 A		31.0	42.0	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.1	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 4.0 A	3.0	7.5		S
Drain Leakage Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±16 V, V _{DS} = 0 V			±10	μA
Input Capacitance	C _{iSS}	V _{DS} = 10 V		760		pF
Output Capacitance	C _{oSS}	V _{GS} = 0 V		250		pF
Reverse Transfer Capacitance	C _{rSS}	f = 1 MHz		95		pF
Turn-on Delay Time	t _{d(on)}	I _D = 4.0 A		20		ns
Rise Time	t _r	V _{GS(on)} = 10 V		140		ns
Turn-off Delay Time	t _{d(off)}	V _{DD} = 15 V		50		ns
Fall Time	t _f	R _G = 10 Ω		30		ns
Total Gate Charge	Q _G	I _D = 8.0 A		14		nC
Gate to Source Charge	Q _{GS}	V _{DD} = 24 V		2.0		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = 10 V		5.0		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 8.0 A, V _{GS} = 0 V		0.86		V
Reverse Recovery Time	t _{rr}	I _F = 8.0 A, V _{GS} = 0 V		30		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs		20		nC

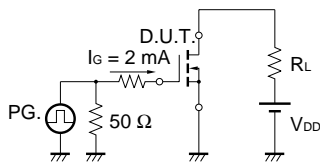
TEST CIRCUIT 1 AVALANCHE CAPABILITY



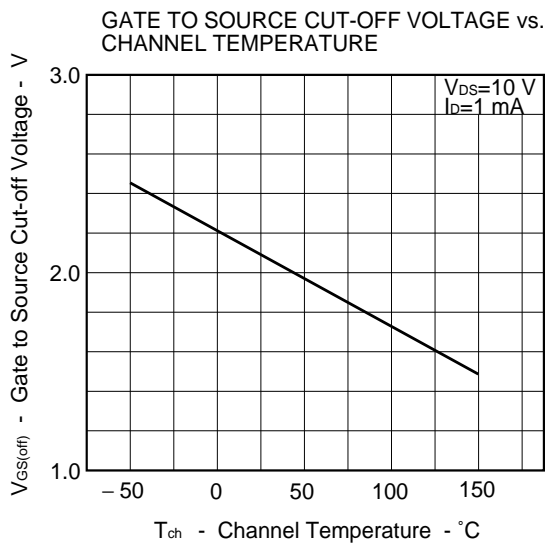
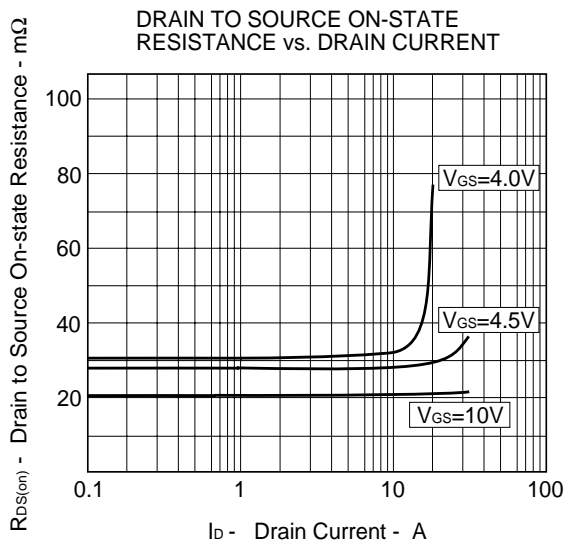
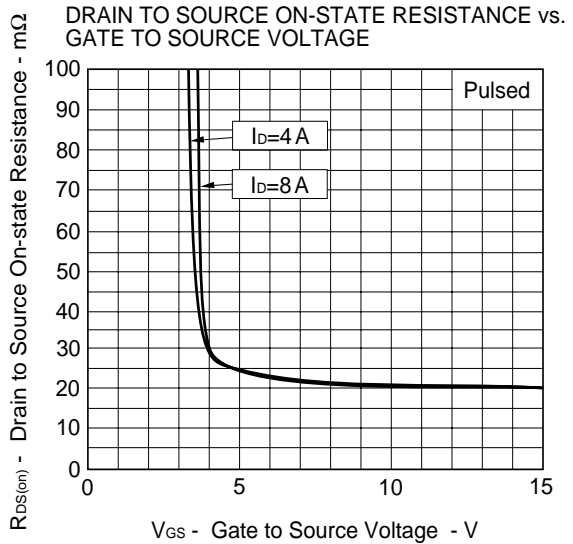
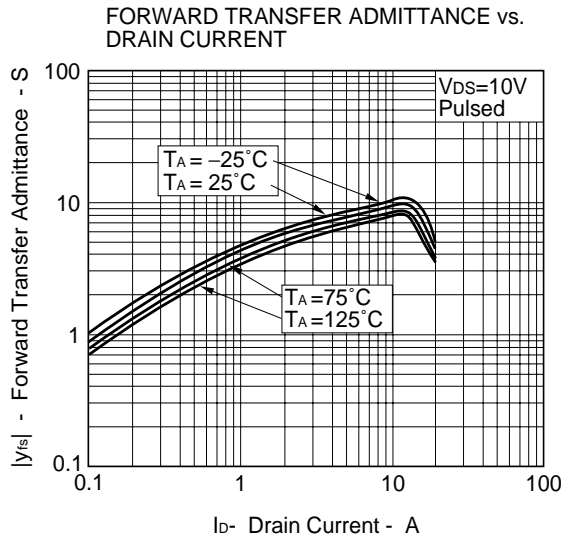
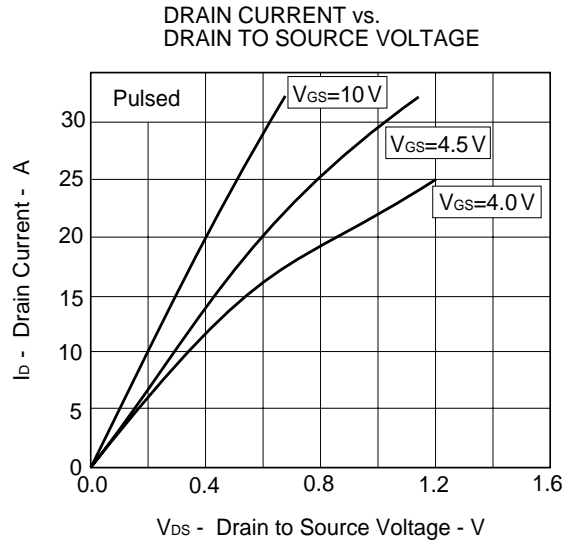
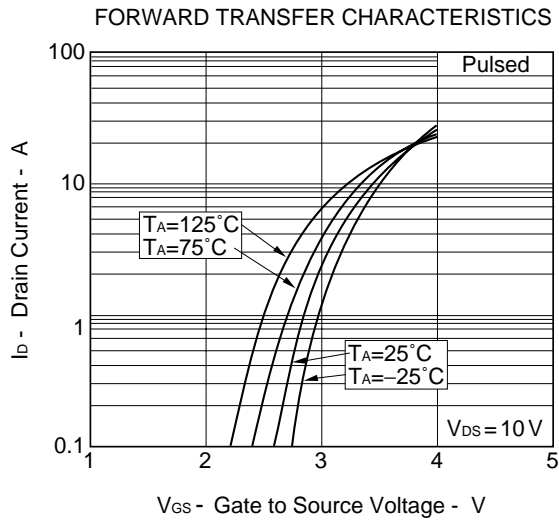
TEST CIRCUIT 2 SWITCHING TIME



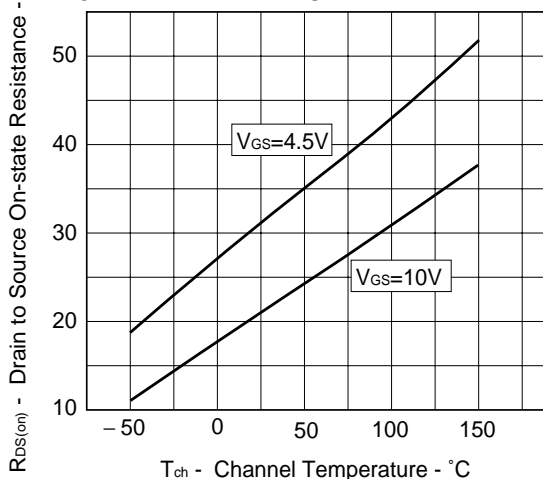
TEST CIRCUIT 3 GATE CHARGE



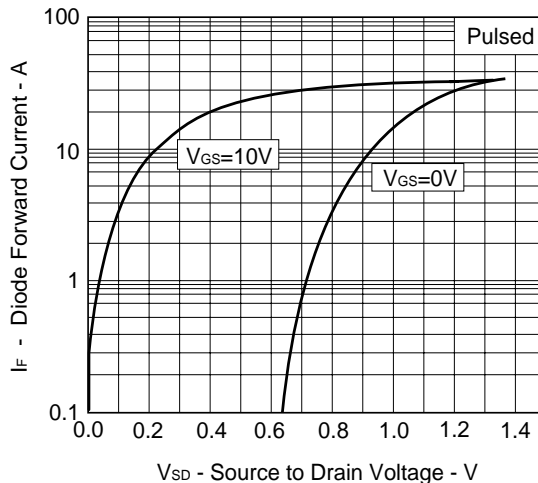
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)



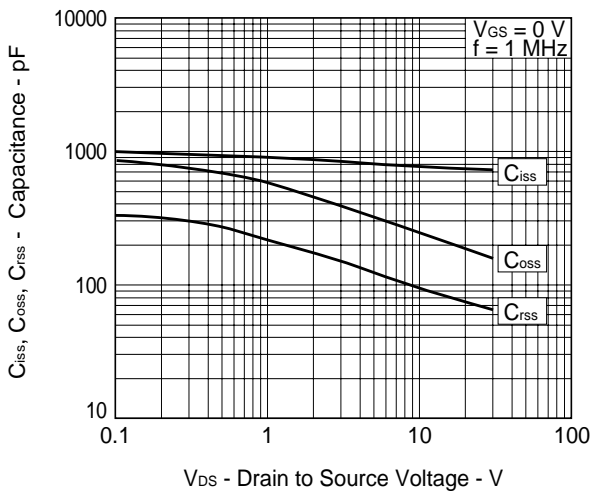
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



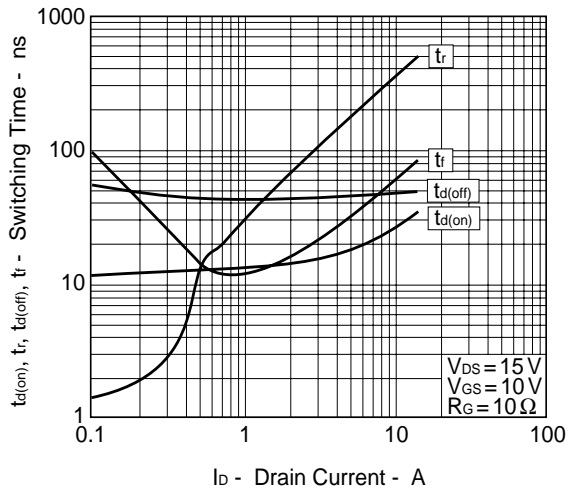
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



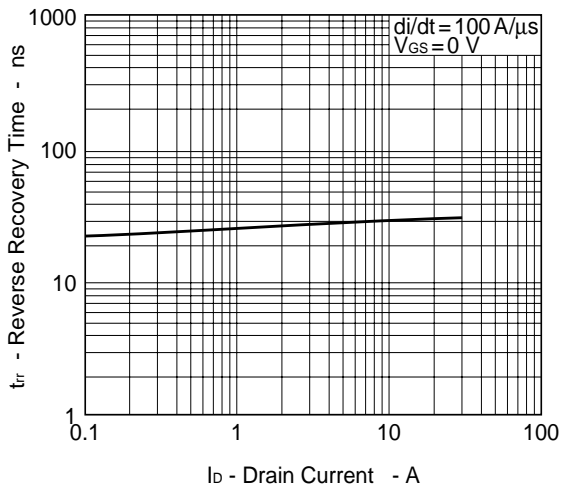
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



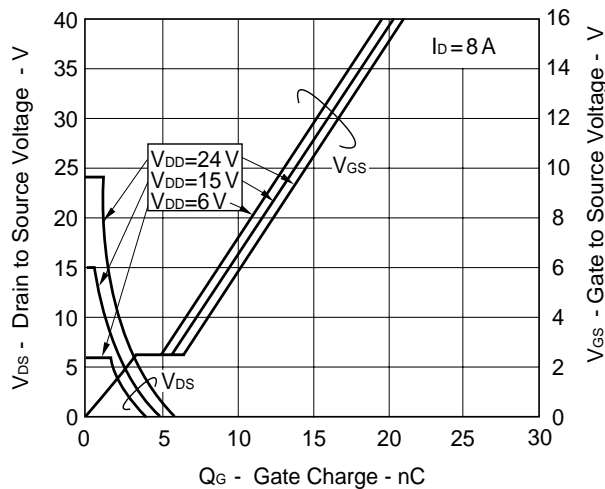
SWITCHING CHARACTERISTICS



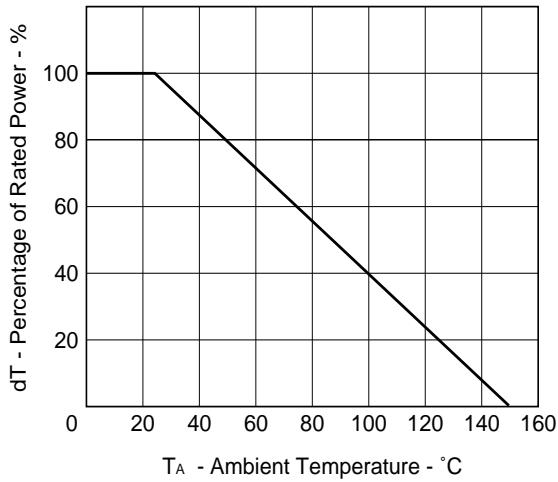
REVERSE RECOVERY TIME vs. DRAIN CURRENT



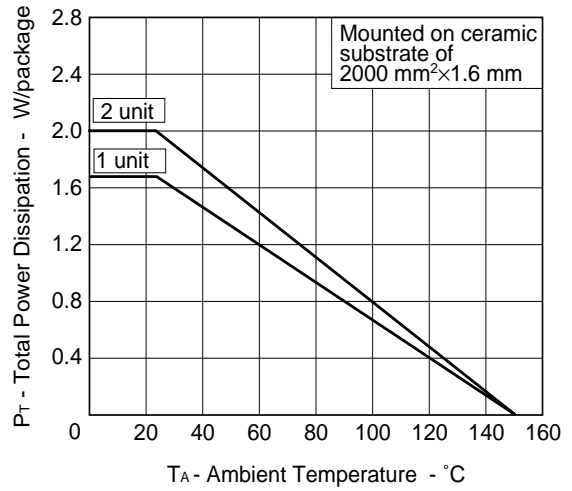
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



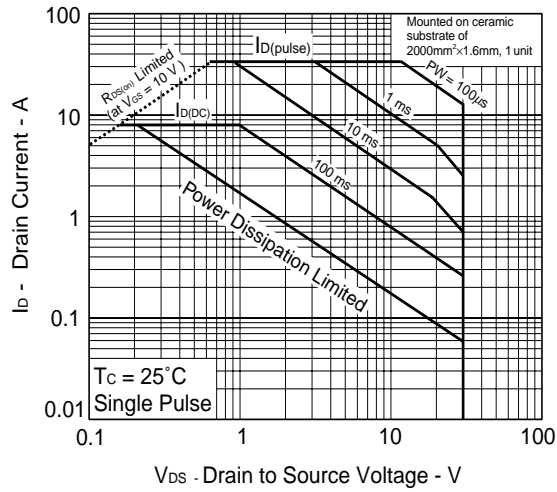
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



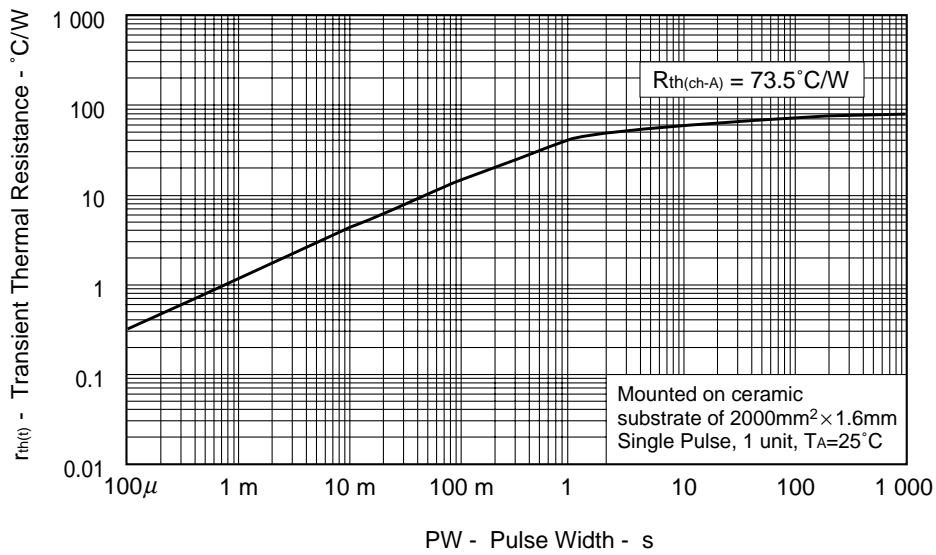
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE

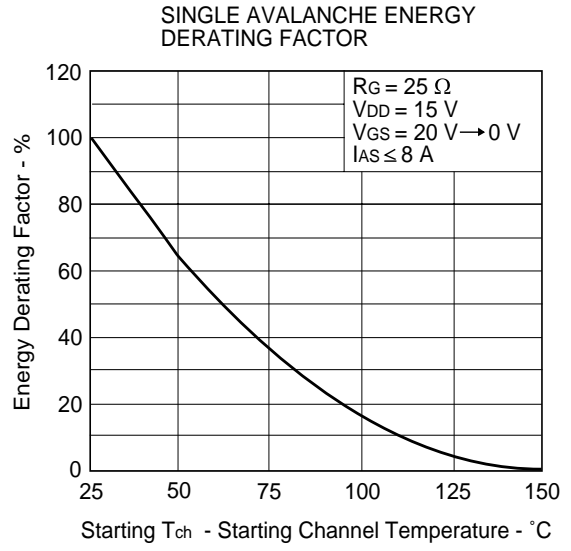
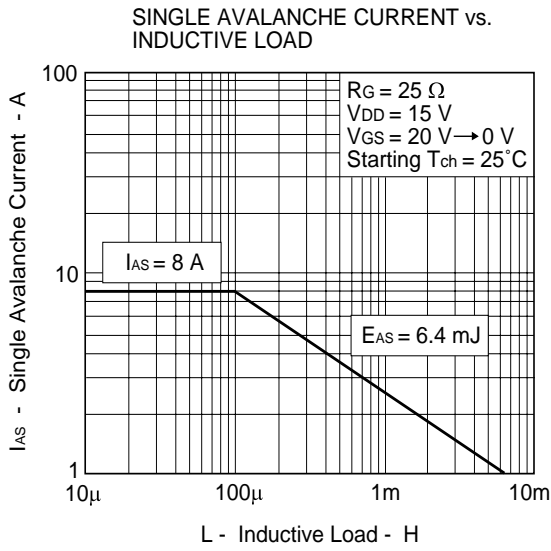


★ FORWARD BIAS SAFE OPERATING AREA



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH





[MEMO]

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