*Click **here** to ask an associate for production status of specific part numbers.*

MAX14829

Low-Power IO-Link Device Transceiver with Dual Drivers

General Description

The MAX14829 integrates the high-voltage functions commonly found in industrial sensors. The MAX14829 features two ultra low-power drivers with active reverse- polarity protection and is specified for operation with supply voltages from 9V to 60V. The high-voltage tolerance of the MAX14829 allows for the use of micro-TVS, simplifying transient protection.

Pins are used to configure and monitor the device. Driver overload and supply monitor outputs are available. Pin-control allows for operation with switching sensors that do not use a microcontroller.

Two integrated linear regulators (3.3V and 5V) provide low-noise analog and logic supply rails for the device or external circuits.

The MAX14829 is available in a (4mm x 4mm) 24-pin TQFN package and is specified over the extended -40°C to +125°C temperature range.

Applications

- Industrial Sensors
- IO-Link® Sensors and Actuators
- Safety Applications

Benefits and Features

- Low Power Dissipation Reduces the Thermal Footprint for Small Sensors
  - 2.3Ω/2.7Ω (typ) Driver On-Resistance
  - 60mW (typ) Operating Power Dissipation
- Configurability and Integration Reduce SKUs
  - Auxiliary 24V Digital Output (DO) and Input (DI)
  - Selectable Driver Current: 100mA to 330mA
  - Pin-Control Interface for Configuration and Monitoring
  - 3.3V and 5V Low-Noise Linear Regulators
  - Optional External Transistor Supports Higher Regulator Load Capability
  - Supervisors Monitor 24V Supply
- Selectable Driver Integrated Protection Enables Robust Communication
  - 65V Absolute Maximum Ratings on Interface and Supply Pins Allows for Flexible TVS Protection
  - 9V to 60V Specified Operation
  - Glitch Filters for Improved Burst and Noise Resilience
  - Thermal Shutdown Autoretry Cycling
  - Hot-Plug V_{24} Supply Protection
  - Reverse Polarity Protection of All Sensor Interface Inputs/Outputs
  - -40°C to +125°C Operating Temperature Range

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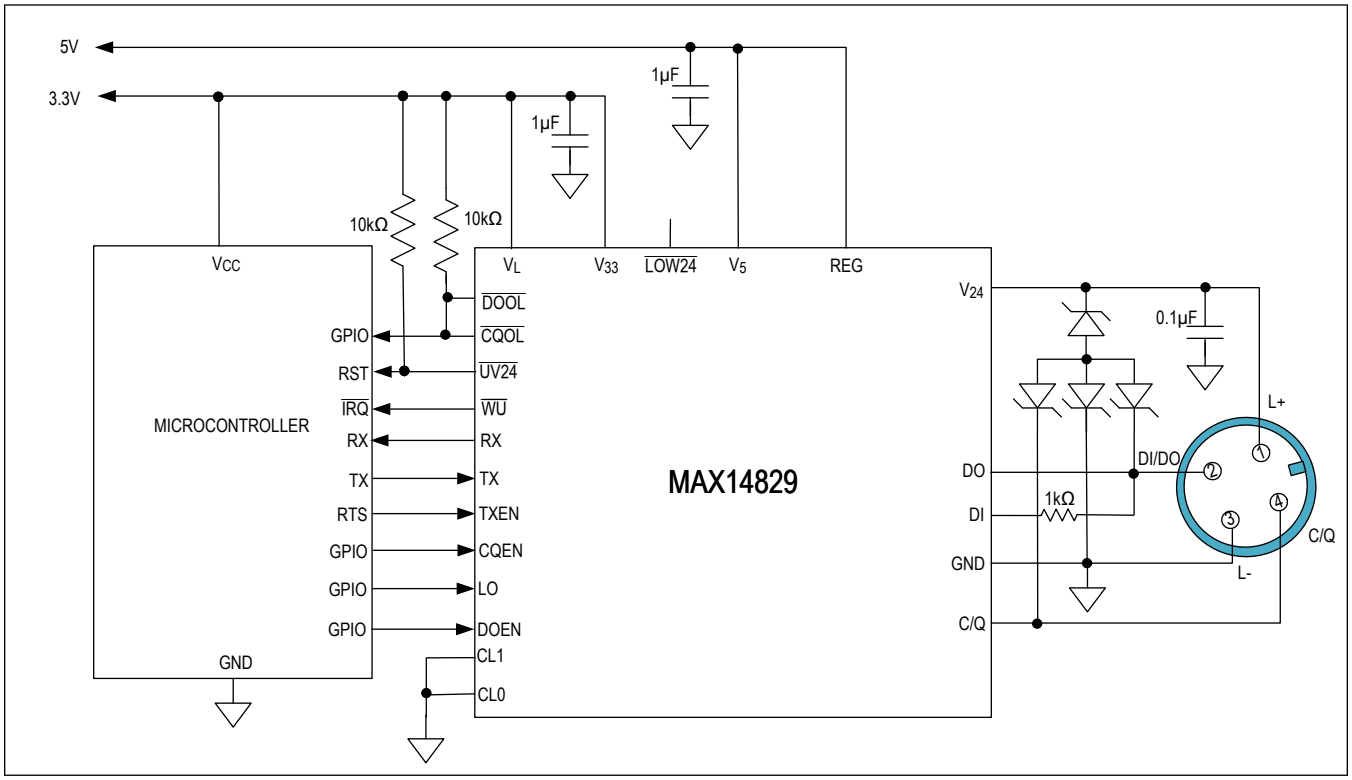
***Ordering Information** appears at end of data sheet.*

19-100654; Rev 3; 10/21

Typical Operating Circuit



Absolute Maximum Ratings

(All voltages referenced to GND, unless otherwise noted.).....
V_{24}..... -70V to +65V
REG.....-0.3V to (V_5 + 16V)
V_5, V_L ..... -0.3V to +6V
V_{33}..... -0.3V to (V5 + 0.3V)
C/Q, DO, DI ..... max(-70V, V_{24} - 70V) to min(+70V, V_{24} + 70V)
Logic Inputs:
CL0, CL1, TXEN, TX, LO,CQEN, ...
DOEN (Note 1).....-0.3V to (V_L + 0.3V)
Logic Outputs:
RX, LI, WU.....-0.3V to (V_L + 0.3V)
LOW24, UV24, CQOL, DOOL ..... -0.3V to +6V

Continuous Current Into GND and V_{24}.....±1A
Continuous Current Into C/Q and DO.....±500mA
Continuous Current Into V_5 and REG.....±100mA
Continuous Current Into Any Other Pin .....±50mA
Continuous Power Dissipation
TQFN (derate 27.8mW/°C above +70°C).....2222mW
Operating Temperature Range .....-40°C to +125°C
Maximum Junction Temperature .....Internally Limited
Storage Temperature Range .....-65ºC to +150ºC
Soldering Temperature
Soldering, 10s ..... +300ºC
Reflow ..... +260ºC

Note 1: CQEN is connected to V_5 with an internal diode. Connecting CQEN to a voltage higher than V_5 can result in a large current sink until V_5 rises above CQEN.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

24 TQFN

Package Code	T2444+4C
Outline Number	21-0139
Land Pattern Number	90-0022
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	3°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

DC Electrical Characteristics

(V_{24} = 9V to 60V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{GND} = 0V; REG unconnected, all logic inputs at V_L or GND; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{24} Supply Voltage	V_{24}		9		60	V
V_{24} Undervoltage Lockout Threshold	V_{24UVLO}	V_{24} rising	6	7.8	9	V
		V_{24} falling	6	7.2	9	
V_{24} Undervoltage Lockout Threshold Hysteresis	V_{24UVLO_HYST}			570		mV

DC Electrical Characteristics (continued)

(V_{24} = 9V to 60V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{GND} = 0V; REG unconnected, all logic inputs at V_L or GND; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{24} Supply Current	I_{24}	V_5 powered externally, REG is unconnected	C/Q and DO disabled (CQEN = Low, DOEN = Low)		0.14	0.5	mA
			C/Q and DO high, CL0 = CL1 = High, no load on C/Q or DO		0.96	1.35	
			C/Q and DO low, CL0 = CL1 = High, no load on C/Q or DO		0.98	1.35	
V_{24} Low-Voltage Warning Threshold	V_{24W}			14.5	16.5	18	V
V_5 Supply Voltage				4.5		5.5	V
V_5 Undervoltage-Lockout Threshold	V_{5UVLO}	V_5 rising		2.8	3.5	4.5	V
		V_5 falling		2.8	3.45	4.5	
V_5 Supply Current	I_{5_IN}	External 5V applied to V_5, REG is unconnected.	C/Q and DO disabled (CQEN = Low, DOEN = Low)		0.66	1.0	mA
			C/Q and DO high, CL0 = CL1 = High, no load on C/Q, DO, or V_{33}		1.42	1.85	
			C/Q and DO low, CL0 = CL1 = High, no load on C/Q, DO, or V_{33}		1.56	2.0	
V_L Logic-Level Supply Voltage	V_L			2.5		5.5	V
V_L Undervoltage Threshold	V_{LUVLO}			0.9	1.7	2.4	V
V_L Logic-Level Supply Current	I_L	All logic inputs at V_L or GND, all logic outputs unconnected			0.25	3	µA
5V LINEAR REGULATOR (V_5)							
V_5 Output Voltage	V_5	REG = V_5, no load on V_5, 9V ≤ V_{24} ≤ 60V		4.75	5.00	5.25	V
Load Regulation	ΔV_{5_LDR}	REG = V_5, 0mA ≤ I_{LOAD} ≤ 30mA, V_{24} = 24V			0.02	0.2	%
Line Regulation	ΔV_{5_LNR}	REG = V_5, I_{LOAD} = 1mA, V_{24} from 9V to 60V			0.01	4	mV/V
REG Output Current	I_{REG}	Internal regulator or external NPN				30	mA
V_{24} to REG Dropout Voltage	ΔV_{REG}	V_{24} = 9V, V_5 = 4.5V, I_{REG} = 5mA			2.35		V
REG Open Voltage	V_{REG_OPN}	V_{24} = 60V, V_5 = 4.5V, no load on REG		10	13	16	V

DC Electrical Characteristics (continued)

(V_{24} = 9V to 60V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{GND} = 0V; REG unconnected, all logic inputs at V_L or GND; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_5 Capacitance	CV_5	Allowed capacitance on V_5, REG connected to V_5 (Note 3)		0.8	1	2	µF
3.3V LINEAR REGULATOR (V_{33})							
V_{33} Output Voltage	V_{33}	No load on V_{33}		3.1	3.3	3.5	V
V_{33} Load Regulation	V_{33_LDR}	0mA ≤ I_{LOAD} ≤ 30mA		0	0.4	0.8	%
V_{33} Capacitance	CV_{33}	Allowed capacitance on V_{33} (Note 3)		0.8	1		µF
C/Q, DO DRIVER							
Driver On-Resistance	R_{OH}	High-side enabled, V_{24} = 24V, CL1 = CL0 = High, I_{LOAD} = 200mA (Note 3)			2.65	4.6	Ω
	R_{OL}	Low-side enabled, V_{24} = 24V, CL1 = CL0 = High, I_{SINK} = 200mA (Note 3)			2.3	4.45	
Driver Current Limit	I_{CL}	V_{DRIVER} = (V_{24} – 3V) or 3V	CL0 = Low, CL1 = Low	100	125	155	mA
			CL0 = High, CL1 = Low	210	252	295	
			CL0 = Low, CL1 = High	270	316	365	
			CL0 = High CL1 = High	330	380	430	
Driver Peak Current	I_{CL_PEAK}	DC current, CL1 = high or low, CL0 = high or low				490	mA
C/Q Leakage Current	I_{LEAK_CQ}	C/Q driver is disabled (CQEN = Low), V_{24} = 24V, (V_{24} - 65V) ≤ $V_{C/Q}$ ≤ +60V		-70		+10	µA
		C/Q driver is disabled (CQEN = Low), V_{24} = 30V, 0 ≤ $V_{C/Q}$ ≤ (V_{24} - 0.5V) (Note 3)		-2.5		+2.5	
DO Leakage Current	I_{LEAK_DO}	DO driver is disabled (DOEN = Low), V_{24} = 24V, (V_{24} - 65V) ≤ V_{DO} ≤ +60V		-10		+10	µA
		DO driver is disabled (DOEN = Low), V_{24} = 30V, 0 ≤ V_{DO} ≤ (V_{24} - 0.5V) (Note 3)		-2.5		+2.5	
C/Q Output Reverse Current	I_{REV_CQ}	C/Q driver enabled (CQEN = High, TXEN = High), V_{24} = 30V, $V_{C/Q}$ = (V_{24} + 5V) or -5V		-60		+1000	µA
DO Output Reverse Current	I_{REV_DO}	DO driver enabled (DOEN = High), V_{24} = 30V, V_{DO} = (V_{24} + 5V) or - 5V		-60		+1000	µA
C/Q, DI RECEIVER							
Input Voltage Range	V_{IN}	For valid RX/LI logic		V_{24} - 65		+65	V
C/Q, DI Input Threshold High	V_{TH}	CQEN = High, TXEN = Low	V_{24} > 18V	11	11.8	12.5	V
			V_{24} < 18V	59	65.5	72	% of V_{24}

DC Electrical Characteristics (continued)

(V_{24} = 9V to 60V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{GND} = 0V; REG unconnected, all logic inputs at V_L or GND; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
C/Q, DI Input Threshold Low	V_{TL}	CQEN = High, TXEN = Low	V_{24} > 18V	9	9.8	10.5	V
			V_{24} < 18V	45	54.5	63	% of V_{24}
C/Q, DI Input Hysteresis	V_{HYS_CQ}	CQEN = High, TXEN = Low	V_{24} > 18V		2		V
			V_{24} < 18V		11		% of V_{24}
C/Q Input Capacitance	C_{IN_CQ}	CQEN = High, TXEN = Low, f = 100kHz			50		pF
DI Input Capacitance	C_{IN_DI}	f = 100kHz			10		pF
DI Input Current	I_{IN_DI}	V_{24} = 24V	-5V ≤ V_{DI} ≤ (V_{24} + 5V)	-10		+35	µA
			(V_{24} - 65V) ≤ V_{DI} ≤ +60V	-40		+200	
LOGIC INPUTS (CL0, CL1, TXEN, TX, LO, CQEN, DOEN)							
Logic Input Voltage Low	V_{IL}					0.2 x V_L	V
Logic Input Voltage High	V_{IH}			0.8 x V_L			V
Logic Input Leakage Current	I_{LEAK}	Logic input = GND or VL		-1		+1	µA
LOGIC OUTPUTS (RX, LI, $\overline{WU}$, $\overline{LOW24}$, $\overline{UV24}$, $\overline{CQOL}$, $\overline{DOOL}$)							
Logic Output Voltage Low	V_{OL}	I_{SINK} = 5mA				0.4	V
Logic Output Voltage High	V_{OH}	I_{SOURCE} = 5mA		V_L - 0.4			V
$\overline{LOW24}$, $\overline{UV24}$, $\overline{CQOL}$, $\overline{DOOL}$ Open-Drain Leakage Current	I_{LK_OD}	$\overline{LOW24}$, $\overline{UV24}$, $\overline{CQOL}$, $\overline{DOOL}$ high impedance		-1		+1	µA
THERMAL MANAGEMENT							
C/Q and DO Driver Thermal Shutdown Temperature	T_{SHUT_D}	Driver temperature rising, driver is turned off			+160		°C
C/Q and DO Driver Thermal Shutdown Temperature Hysteresis	T_{SHUT_DHYS}	Driver temperature falling, driver is reenabled			15		°C
IC Thermal Shutdown	T_{SHUT_IC}	Die temperature rising			+170		°C
IC Thermal Shutdown Hysteresis	T_{SHUT_ICHYS}	Die temperature falling			15		°C

AC Electrical Characteristics

(V_{24} = 18V to 30V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{GND} = 0V, REG unconnected, all logic inputs at V_L or GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
C/Q, DO DRIVER						
Driver Low-to-High Propagation Delay	t_{PDLH}	TXEN = High, Figure 1		0.49	0.75	µs
Driver High-to-Low Propagation Delay	t_{PDHL}	TXEN = High, Figure 1		0.61	0.95	µs
Driver Skew	t_{DSKEW}	$\lvert t_{PDLH} - t_{PDHL} \rvert$, TXEN = High, Figure 1	-0.4		+0.4	µs
Driver Rise Time	t_{RISE}	TXEN = High, Figure 1		0.54	1	µs
Driver Fall Time	t_{FALL}	TXEN = High, Figure 1		0.63	1	µs
Driver Enable Time High	t_{ENH}	TXEN = High, Figure 3		0.46	0.9	µs
Driver Enable Time Low	t_{ENL}	TXEN = High, Figure 2		0.52	0.9	µs
Driver Disable Time High	t_{DISH}	TXEN = High, Figure 2		2.1	3	µs
Driver Disable Time Low	t_{DISL}	TXEN = High, Figure 3		1.5	3	µs
C/Q, DI RECEIVER (Figure 4)						
C/Q Receiver Low-to-High Propagation Delay	t_{PRLH_CQ}		0.825	1.56	2.25	µs
C/Q Receiver High-to-Low Propagation Delay	t_{PRHL_CQ}		0.825	1.37	2.25	µs
C/Q Receiver Propagation Delay Skew	t_{RSKEW}	$t_{PRLH\_CQ} - t_{PRHL\_CQ}$		0.19		µs
DI Receiver Low-to-High Propagation Delay	t_{PRLH_DI}		1.3	2.2	3.7	µs
DI Receiver High-to-Low Propagation Delay	t_{PRHL_DI}		1.3	2.2	3.7	µs
DRIVER CURRENT LIMITING						
Blanking Time	t_{ARBL}	AR = High or low		500		µs
Autoretry Period	t_{ARP}	AR = High		50		ms
WAKE-UP DETECTION (Figure 5)						
Wake-Up Input Minimum Pulse Width	t_{WUMIN}	C_L = 3nF	55	66	75	µs
Wake-Up Input Maximum Pulse Width	t_{WUMAX}		85	95	110	µs
$\overline{WU}$ Output Low Time	t_{WUL}	Valid wake-up condition on C/Q	100	200	300	µs

Note 2: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 3: Not production tested. Guaranteed by design.

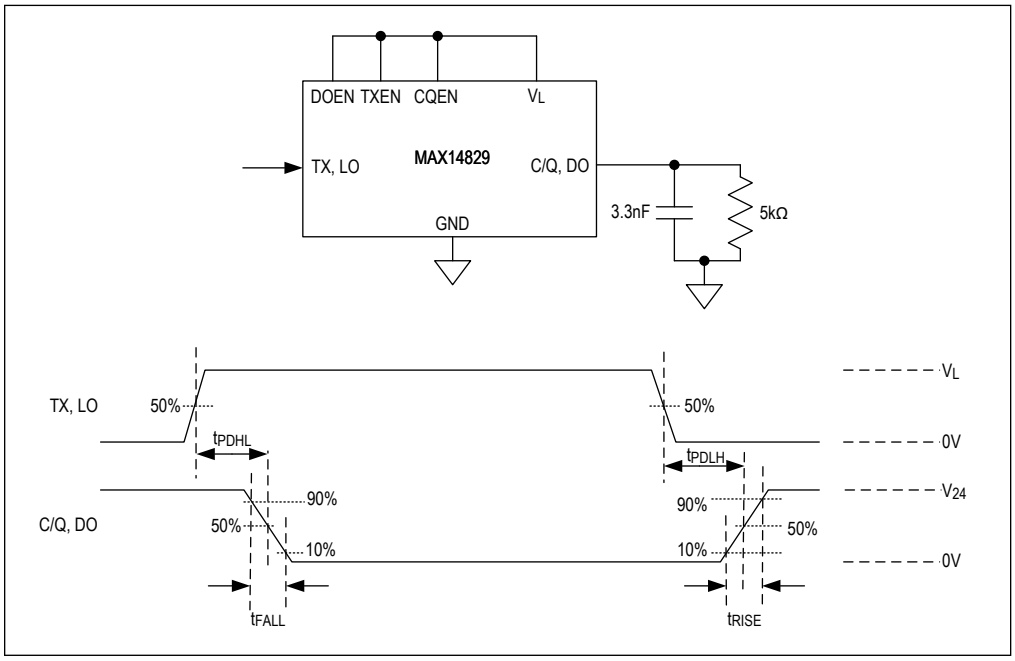


Figure 1. C/Q and LO Driver Propagation Delays and Rise/Fall Times

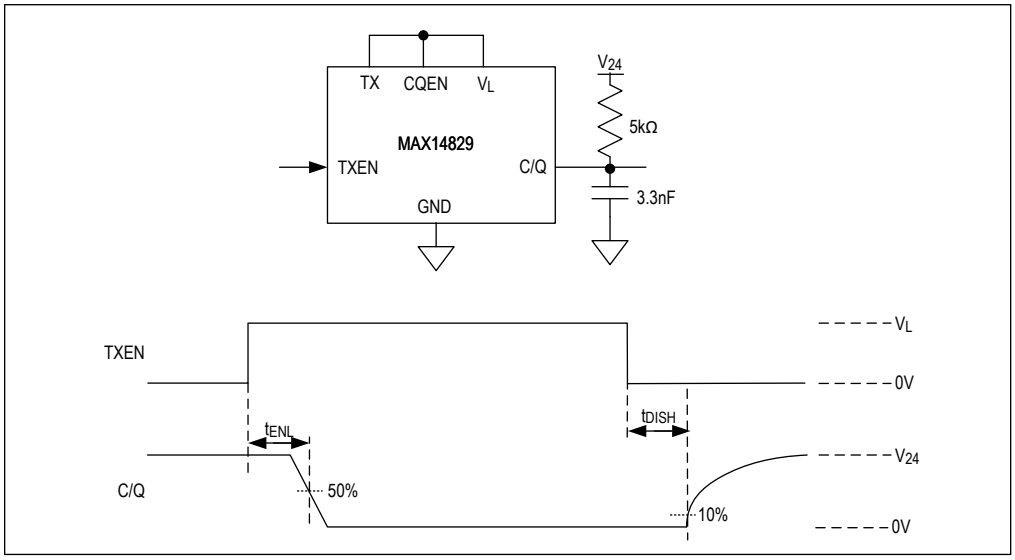


Figure 2. C/Q Driver Enable Low and Disable High Timing with External Pullup Resistor

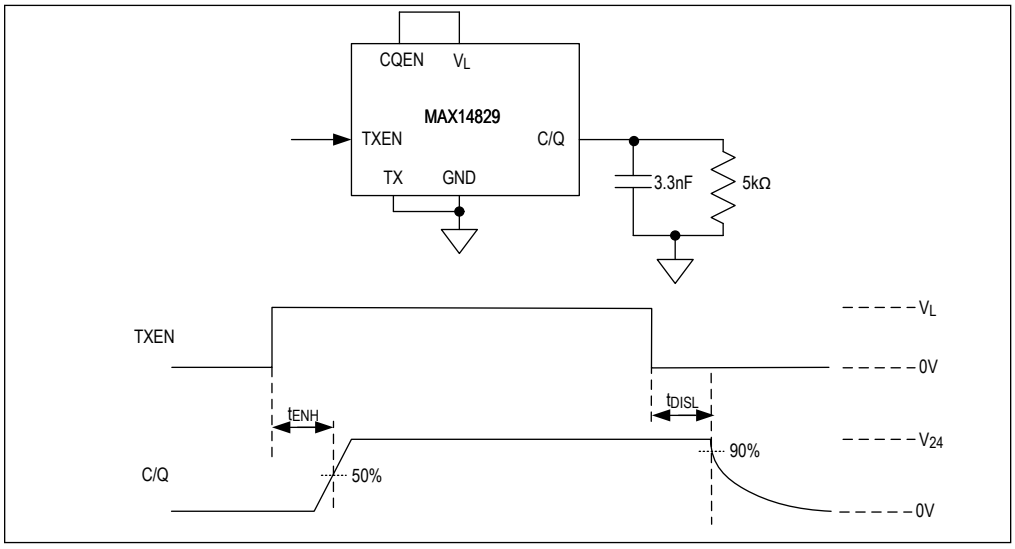


Figure 3. C/Q Driver Enable High and Disable Low Timing

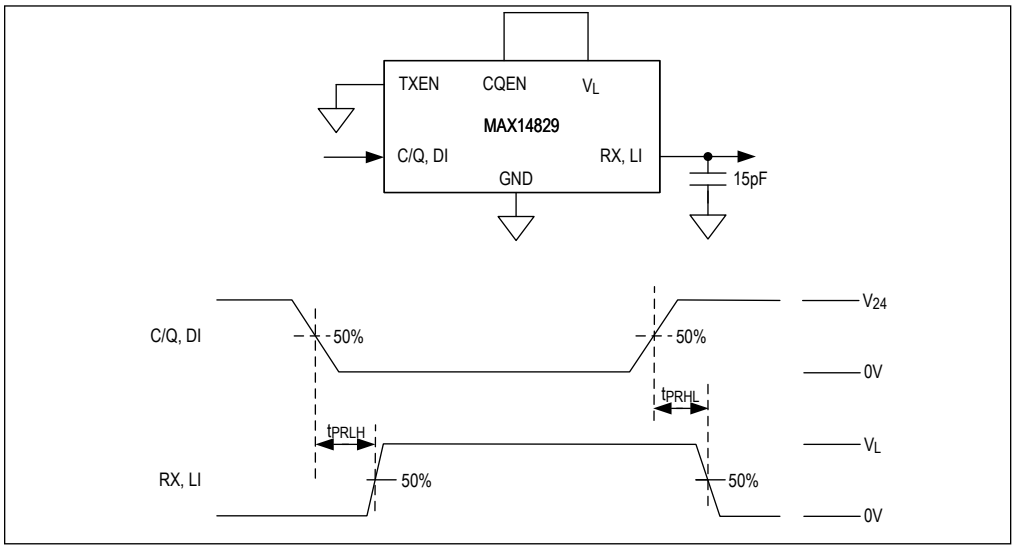
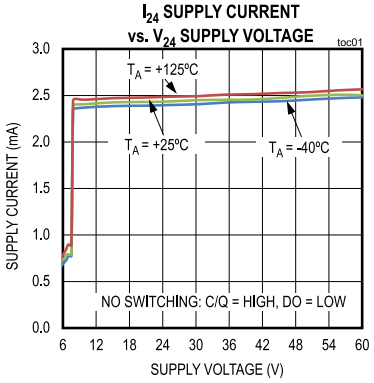
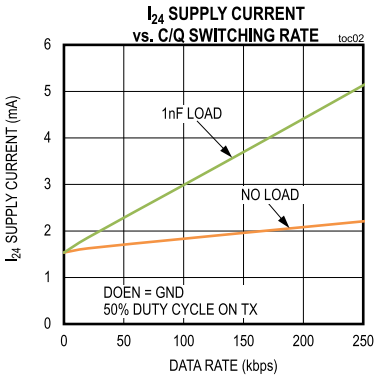


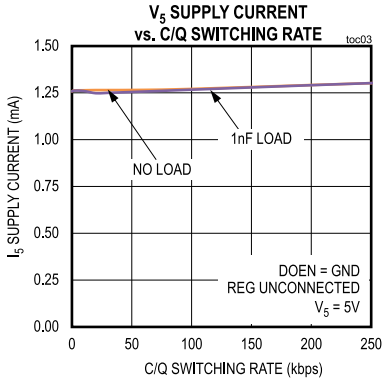
Figure 4. C/Q and DI Receiver Propagation Delays

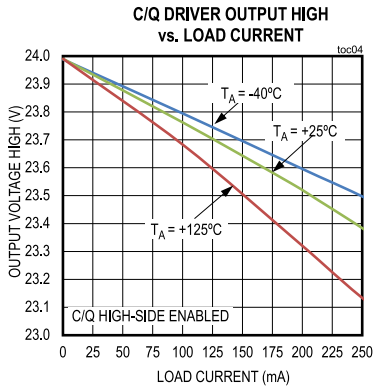
Typical Operating Characteristics

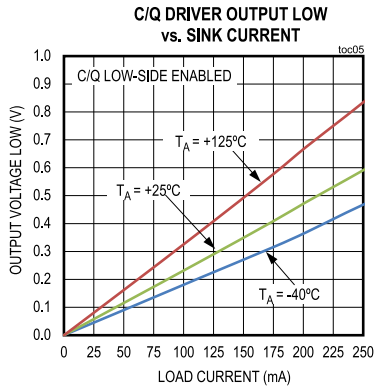
(V_{24} = 24V, V_L = V_{33}, REG is shorted to V_5, CQEN = V_L, DOEN = V_L, T_A = +25°C, unless otherwise noted.)

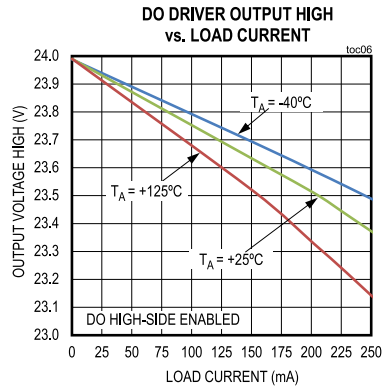


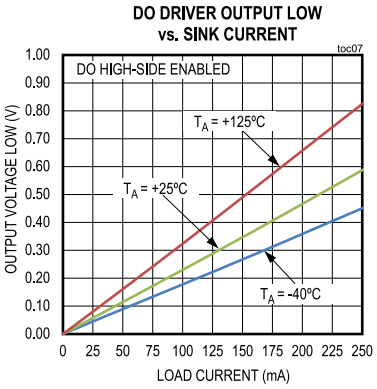


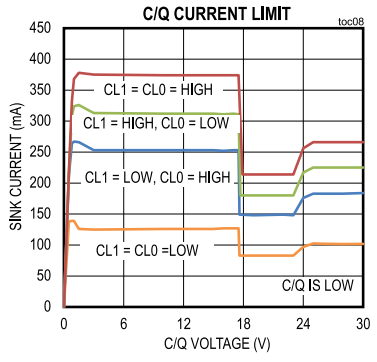


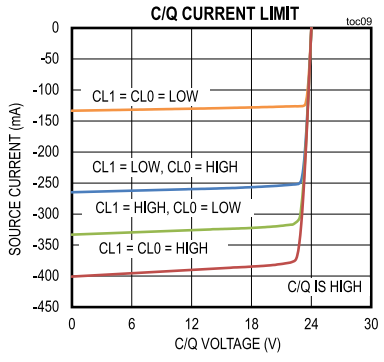








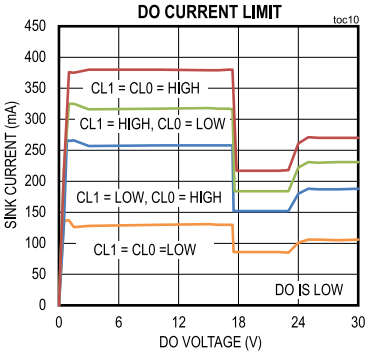




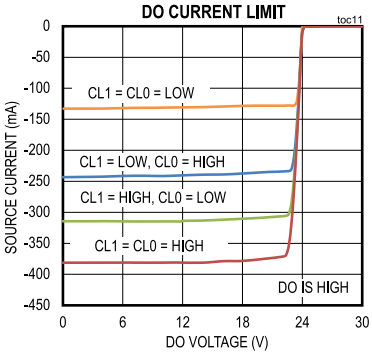
Typical Operating Characteristics (continued)

(V_{24} = 24V, V_L = V_{33}, REG is shorted to V_5, CQEN = V_L, DOEN = V_L, T_A = +25°C, unless otherwise noted.)

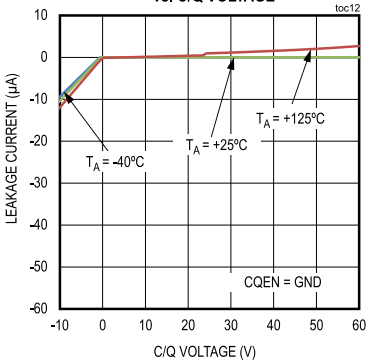
DO CURRENT LIMIT



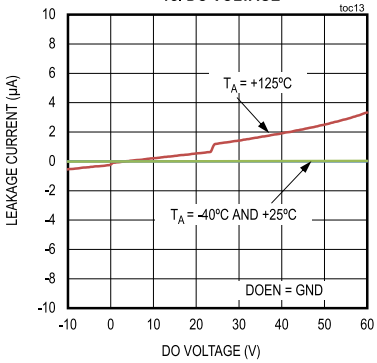
DO CURRENT LIMIT



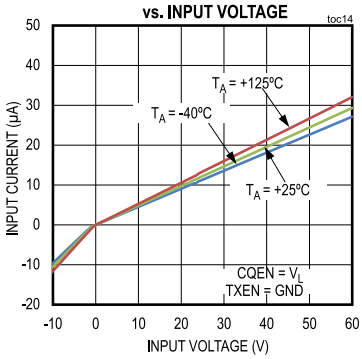
C/Q DRIVER LEAKAGE CURRENT vs. C/Q VOLTAGE



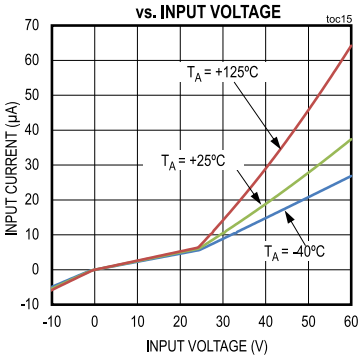
DO DRIVER LEAKAGE CURRENT vs. DO VOLTAGE



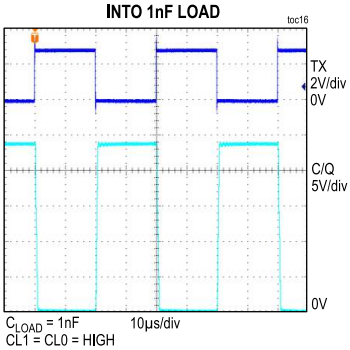
C/Q RECEIVER INPUT CURRENT vs. INPUT VOLTAGE



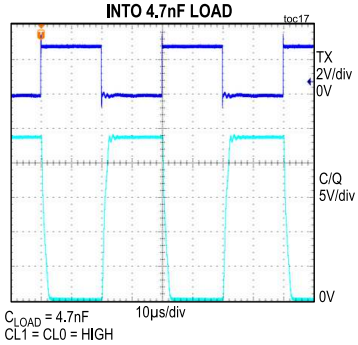
DI RECEIVER INPUT CURRENT vs. INPUT VOLTAGE



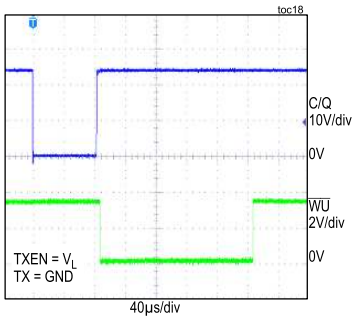
C/Q DRIVER SWITCHING INTO 1nF LOAD



C/Q DRIVER SWITCHING INTO 4.7nF LOAD

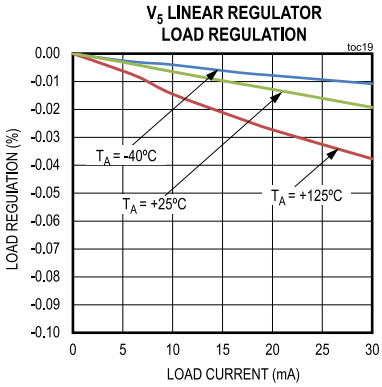


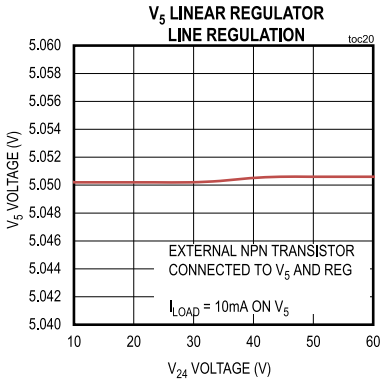
WAKE-UP DETECTION

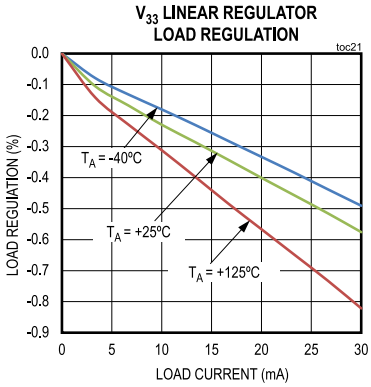


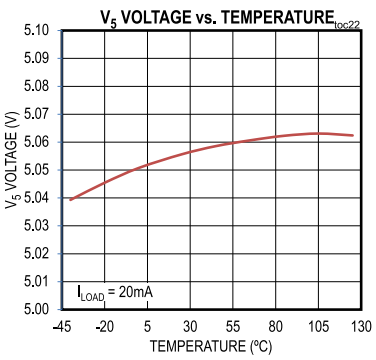
Typical Operating Characteristics (continued)

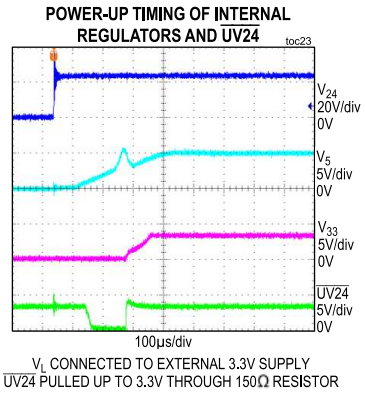
(V_{24} = 24V, V_L = V_{33}, REG is shorted to V_5, CQEN = V_L, DOEN = V_L, T_A = +25°C, unless otherwise noted.)





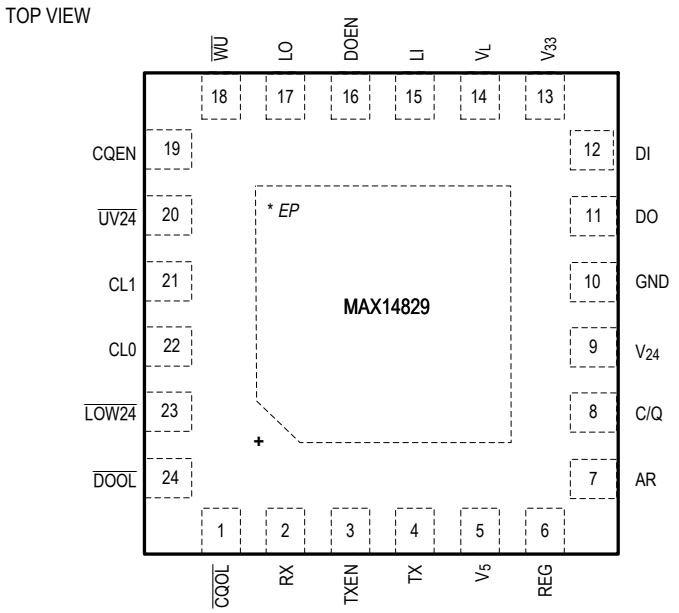






Pin Configuration

Pin Configuration



TQFN
4mm x 4mm

Pin Description

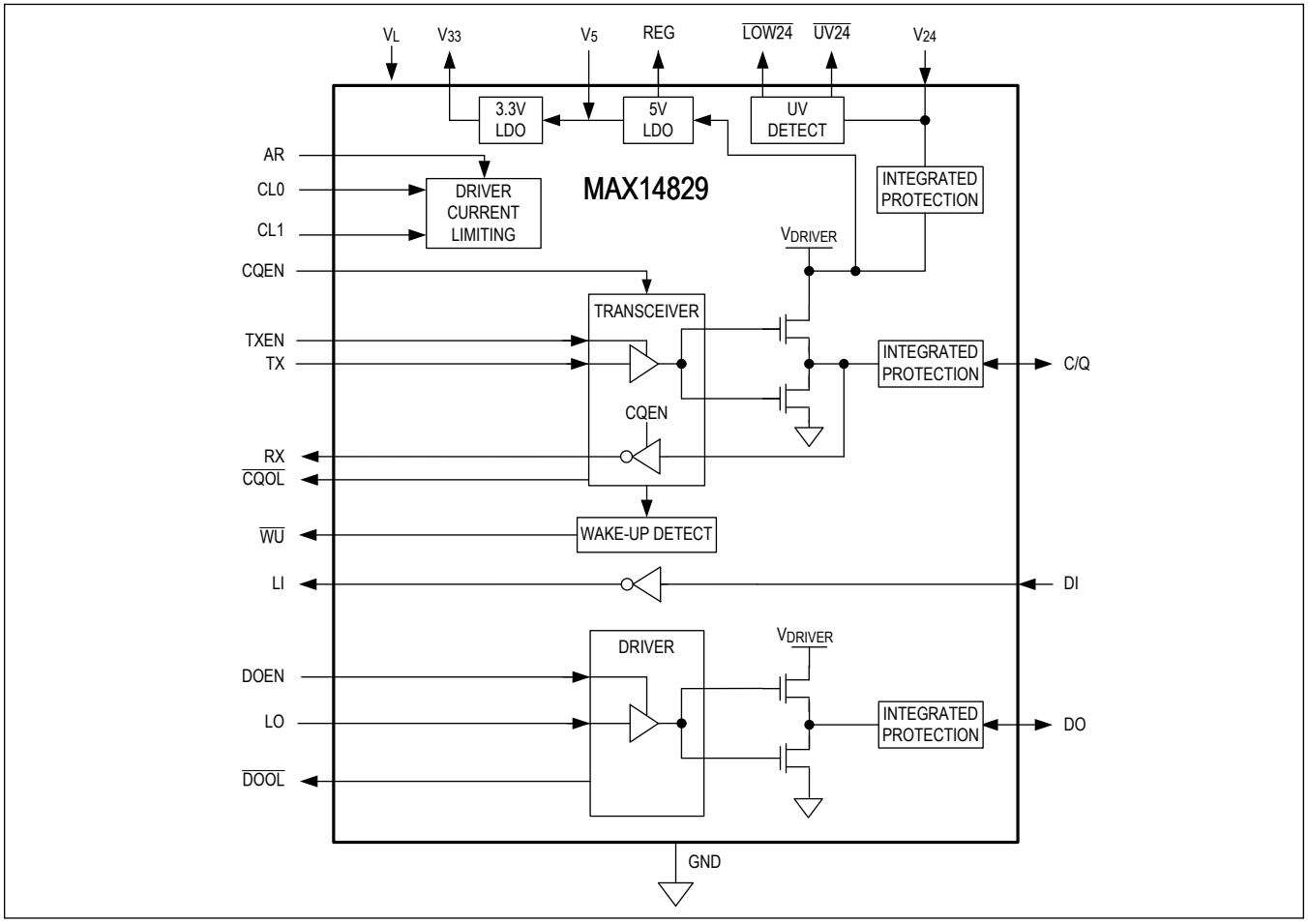
PIN	NAME	FUNCTION
1	$\overline{CQOL}$	Open-Drain C/Q Driver Fault Output. $\overline{CQOL}$ asserts low when a current overload condition is detected on C/Q for longer than the blanking time, or when the C/Q driver goes into driver thermal shutdown.
2	RX	C/Q Receiver Logic Output. RX is the logic inverse of C/Q. Connect RX to the RX input of a UART for IOLink communication. RX is disabled and forced low when CQEN is low.
3	TXEN	C/Q Driver Enable Logic Input. Drive TXEN high to enable the C/Q driver. Drive TXEN low to disable the C/Q driver. Connect TXEN to the RTS output of a microcontroller for IO-Link communication.
4	TX	C/Q Driver Logic Input. C/Q is the logic inverse of the signal on TX when TXEN is high. Connect TX to the TX output of a UART for IO-Link communication.
5	V_5	5V Linear Regulator Output/Supply Input. Bypass V_5 to GND with a 1µF capacitor. V_5 can be supplied by the internal 5V linear regulator or by an external regulator. To use the internal regulator, connect V_5 to REG, or to the emitter of an external NPN transistor. To bypass the internal regulator, leave REG unconnected and connect an external 5V supply directly to V_5. 5V must be present on V_5 for normal operation.
6	REG	5V Regulator Control. To use the internal 5V linear regulator, connect REG to V_5 or connect REG to the base of an external NPN pass transistor. Leave REG unconnected and connect V_5 to an external 5V supply to bypass the internal regulator. 5V must be present on V_5 for normal operation.
7	AR	Autoretry Enable Logic Input. Drive AR high to enable autoretry overload cycling. Drive AR low to disable autoretry overload cycling.

Pin Description (continued)

PIN	NAME	FUNCTION
8	C/Q	C/Q Transceiver Input/Output. Drive CQEN and TXEN high to enable the C/Q driver. The logic on the C/Q output is the logic inverse of the signal on TX. C/Q is high impedance when CQEN is low.
9	V_{24}	Power Supply Input. Bypass V_{24} to GND with a 0.1µF ceramic capacitor as close to the device as possible.
10	GND	Ground
11	DO	DO Driver Output. Drive DOEN high to enable the DO driver. DO is the logic inverse of the LO input. Drive DOEN low to disable the driver. DO is high impedance when DOEN is low.
12	DI	DI Receiver Input. LI is the logic inverse of the signal on the DI input. The DI receiver is always enabled.
13	V_{33}	3.3V Linear Regulator Output. Bypass V_{33} to GND with a 1µF capacitor as close to the IC as possible. V_{33} is not required for normal operation. Connect V_{33} to V_5 to disable the 3.3V linear regulator.
14	V_L	Logic-Level Supply Input. V_L defines the logic levels of the logic I/Os. Bypass V_L to GND with a 0.1µF ceramic capacitor. Apply a voltage from 2.5V to 5.5V to V_L for normal operation.
15	LI	DI Receiver Logic Output. LI is the logic inverse of the signal on the DI input. LI is always enabled.
16	DOEN	DO Driver Enable Logic Input. Drive DOEN high to enable the DO output. DO is high impedance when DOEN is low.
17	LO	DO Driver Logic Input. DO is the logic inverse of the signal on LO when DOEN is high.
18	$\overline{WU}$	Push-Pull Wake-Up Detection Output. $\overline{WU}$ asserts low for 200µs (typ) when a valid IO-Link wake-up is detected on the C/Q line.
19	CQEN	C/Q Driver Enable Logic Input. Drive CQEN high to power the C/Q driver and receiver. C/Q is high impedance when CQEN is low. The C/Q driver and receiver are disabled when CQEN is low.
20	$\overline{UV24}$	Open-Drain V_{24} Supply Undervoltage Indicator Output. $\overline{UV24}$ asserts low when V_{24} falls below the 7.2V (typ) undervoltage lockout (UVLO) threshold. $\overline{UV24}$ deasserts when V_{24} rises above the 7.8V (typ) UVLO threshold.
21	CL1	Driver Current Limit Setting Inputs. Connect CL0 and CL1 high or low to set the maximum load current for the C/Q and DO driver outputs. See the Table 3 and *Electrical Characteristics* table for more information.
22	CL0	Driver Current Limit Setting Inputs. Connect CL0 and CL1 high or low to set the maximum load current for the C/Q and DO driver outputs. See the Table 3 and *Electrical Characteristics* table for more information.
23	$\overline{LOW24}$	Open-Drain V_{24} Supply Warning Voltage Indicator Output. $\overline{LOW24}$ asserts low when V_{24} falls below the 16.5V (typ) warning voltage threshold. LOW24 deasserts when V_{24} rises above 16.5V (typ).
24	$\overline{DOOL}$	Open-Drain DO Driver Fault Output. $\overline{DOOL}$ asserts low when a current overload condition is detected on DO for longer than the blanking time, or when the DO driver goes into driver thermal shutdown
EP	EP	Exposed pad. Connect to ground. Not intended as the main ground connection.

Functional Diagram

Functional Diagram



Detailed Description

The MAX14829 is an industrial sensor output driver/IO-Link device transceiver. The IC integrates the high voltage functions commonly found in sensors, including two 24V line drivers (C/Q and DO) and two on-board linear regulators (LDOs). The integrated 3.3V and 5V LDOs provide the low-noise power needed for analog and logic supply rails.

The MAX14829 provides pins to configure and monitor device operation.

24V Interface (V_{24}, C/Q, DO, DI, GND)

The MAX14829 features an IO-Link transceiver interface capable of operating with voltages up to 60V. This is the 24V interface and includes the C/Q input/output, the logic-level digital output (DO), the logic-level digital input (DI), the V_{24} supply, and ground. The MAX14829 features switching drivers at C/Q and DO.

C/Q and DO Configurable Drivers

The C/Q and DO drivers are push-pull (Table 1 and Table 2). Toggle CQEN, TXEN, TX, DOEN, and LO to switch the C/Q and DO outputs and to operate C/Q and DO as NPN and PNP outputs.

C/Q and DO Driver Enable/Disable

The C/Q driver is enabled/disabled with the TXEN and CQEN inputs. Drive CQEN high to enable the C/Q transceiver and drive TXEN high to enable the C/Q driver. C/Q is the logic inverse of the TX input.

The DO driver is enabled/disabled with the DOEN input. Drive DOEN high to enable the DO driver. DO is the logic inverse of the LO input.

Table 1. C/Q Driver Control

CQEN	TXEN	TX	C/Q DRIVER	
			LOW SIDE	HIGH SIDE
L	X	X	Driver and Receiver are disabled	
H	L	X	OFF	OFF
H	H	L	OFF	ON
H	H	H	ON	OFF

Table 2. DO Control

DOEN	LO	DO	
		LOW SIDE	HIGH SIDE
L	X	OFF	OFF
H	L	OFF	ON
H	H	ON	OFF

C/Q and DO Driver Current Limit

The C/Q and DO drivers are optimized for driving large capacitive loads and dynamic impedances like incandescent lamps. The C/Q and DO driver current limit thresholds are selectable by setting the CL1 and CL0 pins (Table 3). When a load attempts to draw more current than the current limit threshold set by CL1 and CL0, the driver actively limits the load current so a higher current does not flow. If the overcurrent condition persists longer than the blanking time, the driver enters fault mode. See the *C/Q and DO Driver Fault Protection* section for more information.

Table 3. Driver Current Limit Setting

CL1	CL0	C/Q AND DO CURRENT LIMIT (mA)
L	L	125
L	H	252

Table 3. Driver Current Limit Setting (continued)

CL1	CL0	C/Q AND DO CURRENT LIMIT (mA)
H	L	316
H	H	380

C/Q and DO Driver Fault Protection

The MAX14829 features two management functions to allow the C/Q and DO drivers to drive large loads: the blanking time, and autoretry.

Set AR high to enable autoretry cycling when an overcurrent condition occurs. In this mode, the driver is disabled after the 500µs (typ) blanking time and the driver fault indicator ($\overline{CQOL}$ or $\overline{DOOL}$) asserts low. The driver is reenabled after the 50ms (typ) autoretry time. If the overcurrent condition is still present, the driver is again disabled after the blanking time and the cycle continues. The driver operates normally and the driver fault indicator deasserts within 50ms (typ) after the fault is removed.

Set AR low to disable autoretry cycling when an overcurrent occurs. In this mode, the driver fault indicator ($\overline{CQOL}$ or $\overline{DOOL}$) asserts low if the overcurrent condition is present for longer than 500µs (typ). If the driver temperature exceeds the driver thermal shutdown threshold, the driver is disabled. When the driver temperature then falls by the 15°C (typ) thermal shutdown hysteresis, the driver automatically is reenabled and the fault indicator pin deasserts. This thermal cycling repeats until the fault is removed.

C/Q Receiver Output (RX)

RX is the output of the C/Q receiver. RX is the inverse logic of the C/Q input. The C/Q transceiver is disabled and RX is low when CQEN is driven low.

C/Q and DI Receiver Threshold

The IO-Link standard defines device operation with a sensor supply between 18V and 30V. Industrial sensors, however, commonly operate with supply voltages as low as 9V. The MAX14829 C/Q and DI receivers support operation with lower supply voltages by scaling the receiver thresholds when V_{24} is less than 18V (V_{24} < 18V).

Reverse-Polarity Protection

The MAX14829 is protected against reverse-polarity connections on V_{24}, C/Q, DO, DI, and GND. Any combination of these pins can be connected to DC voltages up to 65V (max), resulting in a current flow of less than 1mA.

Ensure that the maximum voltage between any of these pins does not exceed the limits in the *Absolute Maximum Ratings* section.

5V and 3.3V Linear Regulators

The MAX14829 includes two internal regulators to generate 5V (V_5) and 3.3V (V_{33}).

The V_5 regulator is capable of driving external loads up to 30mA, including the device and 3.3V LDO current consumption. To drive larger loads, use an external pass transistor to generate the required 5V. When using an external transistor, connect REG to the base of the transistor to regulate the voltage and connect V_5 to the emitter (Figure 7).

When the internal 5V linear regulator is not used, V5 is the supply input for the internal analog and digital functions and must be supplied externally.

The MAX14829 requires a V_5 supply for normal operation

The 3.3V regulator is capable of driving external loads up to 30mA. V_5 and V_{33} are not protected against short circuits.

Power Up

The C/Q and DO driver outputs are high-impedance when V_{24}, V_5, and V_L are below their respective undervoltage thresholds during power up.

The drivers are automatically disabled if any of the V_{24}, V_5, or V_L supplies falls below its threshold.

Low Voltage and Undervoltage Detection

The device monitors the V_{24} supply for low-voltage and undervoltage lockout (UVLO) conditions. $\overline{LOW24}$ asserts low when the V_{24} supply falls below the 16.5V (typ) warning threshold.

$\overline{UV24}$ asserts when the V_{24} supply falls below the 7.2V (typ) UVLO threshold. The C/Q and DO outputs are disabled, and the C/Q and DI receivers are disabled when V_{24} falls below the UVLO threshold.

$\overline{LOW24}$ and $\overline{UV24}$ are open-drain outputs that are active when the V_5 supply voltage is higher than 1.5V (typ). $\overline{LOW24}$ and $\overline{UV24}$ do not depend on the presence of the V_{33} or V_L supplies. If the V_5 supply is powered by the integrated regulator (REG = V_5), the V_5 voltage rises to 1.5V (typ) in 130µs (typ), based on a 1µF load on V_5. Connect $\overline{LOW24}$ and $\overline{UV24}$ to a pullup voltage, typically V_L, up to 6V. $\overline{LOW24}$ and $\overline{UV24}$ can be left unconnected if not used. Low-voltage and UVLO monitoring cannot be disabled. Refer to Table 4 and Table 5.

Table 4. V_{24} Voltage Detection ($\overline{UV24}$ Output)

V_5 VOLTAGE (V)	V_{24} VOLTAGE (V)	$\overline{UV24}$ OUTPUT
$1.5V < V_5 < V_{5UVLO}$	$-70V \le V_{24} \le +65V$	Low
$V_{5UVLO} \le V_5$	$V_{24} < V_{24UVLO}$	Low
	$V_{24UVLO} \le V_{24} \le +65V$	High-Impedance

Table 5. V_{24} Voltage Detection ($\overline{LOW24}$ Output)

V_5 VOLTAGE (V)	V_{24} VOLTAGE (V)	$\overline{LOW24}$ OUTPUT
$1.5V < V_5 < V_{5UVLO}$	$-70V \le V_{24} \le +65V$	Low
$V_{5UVLO} \le V_5$	$V_{24} < V_{24W}$	Low
	$V_{24W} \le V_{24} \le +65V$	High-Impedance

Wake-Up Detection

The MAX14829 detects an IO-Link wake-up condition on the C/Q line in all states (push-pull, NPN, and PNP). A wake-up condition is detected when the C/Q output is shorted for 80µs (typ). $\overline{WU}$ pulses low for 200µs (typ) when the device detects a wake-up pulse on C/Q (Figure 5).

The device includes a wake-up detection algorithm to avoid false wake-up detection on C/Q. No wake-up event is detected within 500µs (typ) after the C/Q driver changes state.

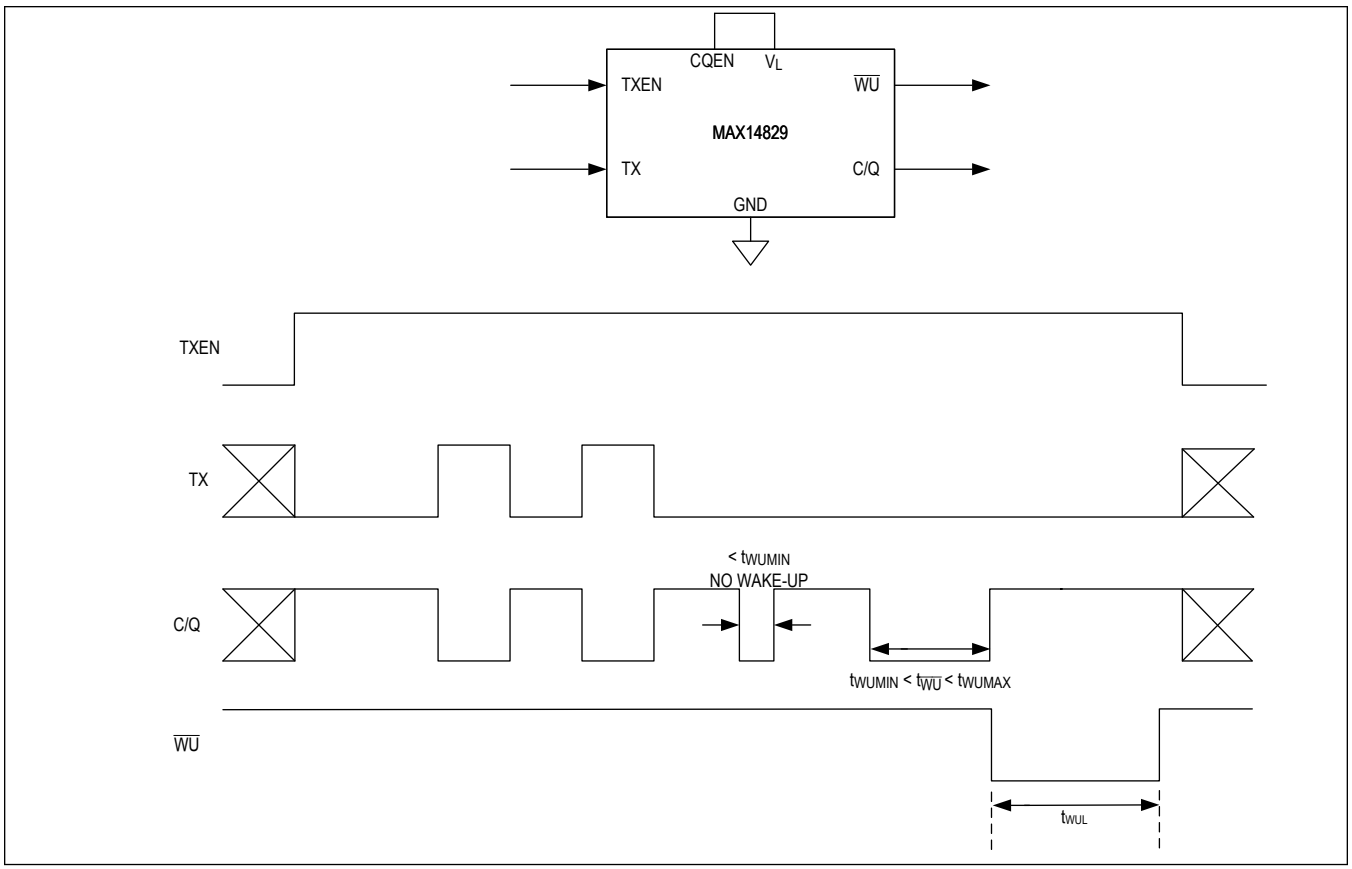


Figure 5. Wake-Up Detection Timing

Thermal Protection and Considerations

The internal LDOs can dissipate a large amount of power when driving external loads. Ensure that the LDO and driver power dissipation is less than the package can dissipate. Total power dissipation for the device is calculated using the following equation:

$$P_{TOTAL} = P_{C/Q} + P_{DO} + P_{V5} + P_{33} + P_{24}$$

where:

$P_{C/Q}$ = Power dissipated by the C/Q driver,

P_{DO} = Power dissipated by the DO driver,

P_{V5} and P_{V33} = Power dissipated by the LDOs,

P_{24} = Quiescent power dissipated by the device,

Ensure that the total power dissipation is less than the limits listed in the *Absolute Maximum Ratings* section.

Use the following to calculate the power dissipation (in mW) due to the C/Q driver:

$$P_{C/Q} = [I_{C/Q}(max)]^2 \times R_O$$

where R_O driver on-resistance. Calculate the internal power dissipation of the DO driver using the following equation:

$$P_{DO} = [I_{DO}(max)]^2 \times R_O$$

where R_O driver on-resistance.

Calculate the power dissipation in the 5V LDO, V_5, using the following equation:

$$P_5 = (V_{24} - V_5) \times I_5$$

where I_5 includes the I_{33} current sourced from V_{33}. Calculate the power dissipated in the 3.3V LDO, V_{33}, using the following equation:

$$P_{33} = 1.7V \times I_{LOAD33}$$

Calculate the quiescent power dissipation in the device using the following equation:

$$P_{24} = I_{24(max)} \times V_{24(max)}$$

IC Thermal Shutdown

The C/Q and DO drivers, and the V_5 and V_{33} regulators are automatically switched off when the junction temperature exceeds the +170°C (typ) thermal shutdown threshold. Regulators are automatically switched on when the internal die temperature falls below the thermal shutdown threshold plus hysteresis.

Applications Information

Microcontroller Interfacing

The logic levels of the interface I/Os are defined by the logic level supply, V_L. Apply a voltage from 2.5V to 5.5V to V_L for normal operation. Logic outputs are supplied by V_L. Connect a UART to TXEN, TX, and RX for IO-Link communication.

Transient Protection

Inductive load switching, ESD, bursts, and surges create high transient voltages. V_{24}, C/Q, DI, and DO should be protected against high overvoltage and undervoltage transients. Positive voltage transients on V_{24}, C/Q, DO, and DI must be limited to +70V relative to GND. Negative voltage transients must be limited to -70V relative to V_{24}. Use protection diodes on C/Q, DO, and DI as shown in Figure 6.

For the standard ESD and burst protection required by the IO-Link specification, small package TVS can be used (like the DFN6-36 or the SPT01-335). If higher level surge ratings need to be achieved (IEC 61000-4-5 ±1kV/42Ω), PDFN3-32 or SMM4F33 TVS protectors can also be used. Cost effective protection for ±1kV/500Ω surge can also be achieved using varistors like the VC060326A580D. Because varistors have bipolar clamping, one varistor must be connected between each of the connector pins. This results in more varistors being required than if using unidirectional TVS protection.

Improved EFT/Burst Resilience

To improve data errors during EFT/burst testing, Maxim recommends adding a 390pF (typ) capacitor from C/Q to GND and from C/Q to V_{24}.

Using an External Transistor with the 5V Regulator

The internal 5V regulator (V_5) can provide up to 30mA of total load current (including any load on the V_{33} regulator) when V_5 is connected to REG. To achieve larger load currents or to shunt power dissipation away from the MAX14829, an external NPN transistor can be connected as shown in Figure 7.

Select an NPN transistor with high V_{CE} voltage to support the max L+ supply voltage. In order to protect the NPN transistor against reverse polarity of the L+/L- supply terminals, connect a silicon or a Schottky diode in series with the NPN transistor collector that has a reverse voltage capability large enough for reverse connected L+/L-. A 1µF capacitor on V_5 is required for stability.

Using a Step-Down Regulator to Power V_5

To decrease power dissipation in the MAX14829, V_5 can be powered by an external step-down regulator. Leave REG unconnected and connect the output of the external regulator to the V_5 input (Figure 8).

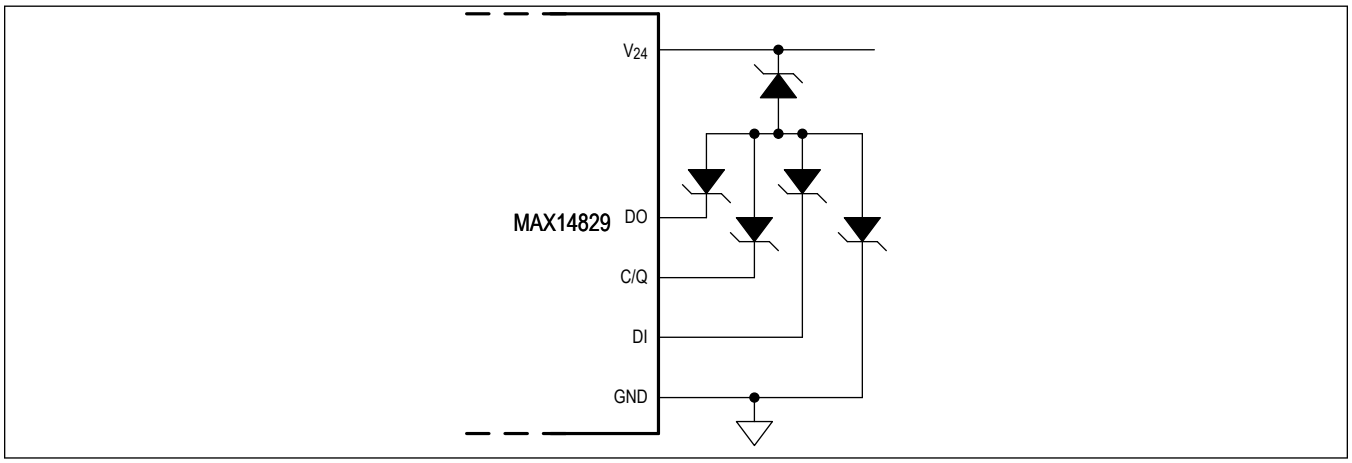


Figure 6. MAX14829 Operating Circuit with TVS Protection

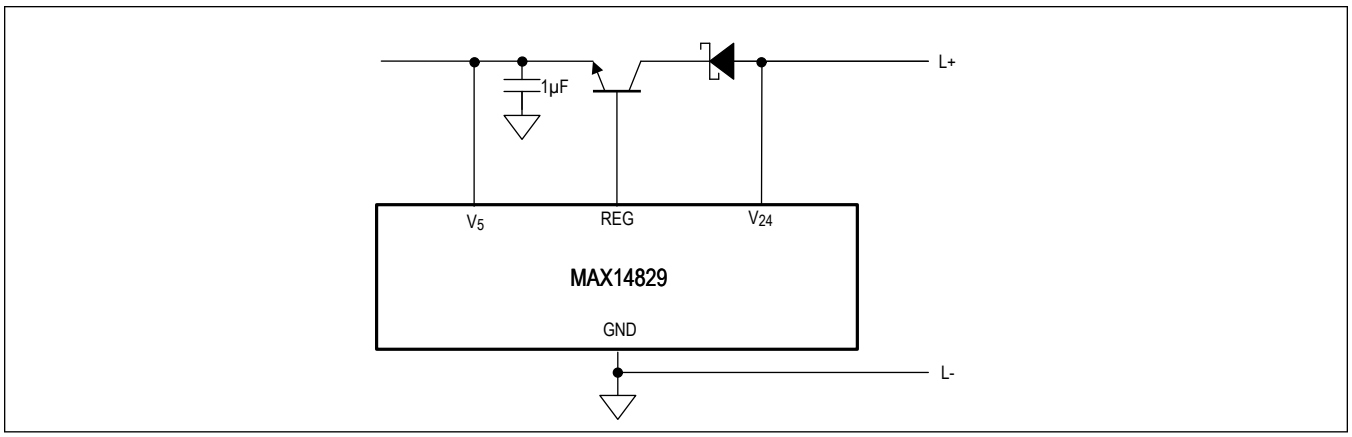


Figure 7. Using an External NPN Transistor with the 5V Regulator

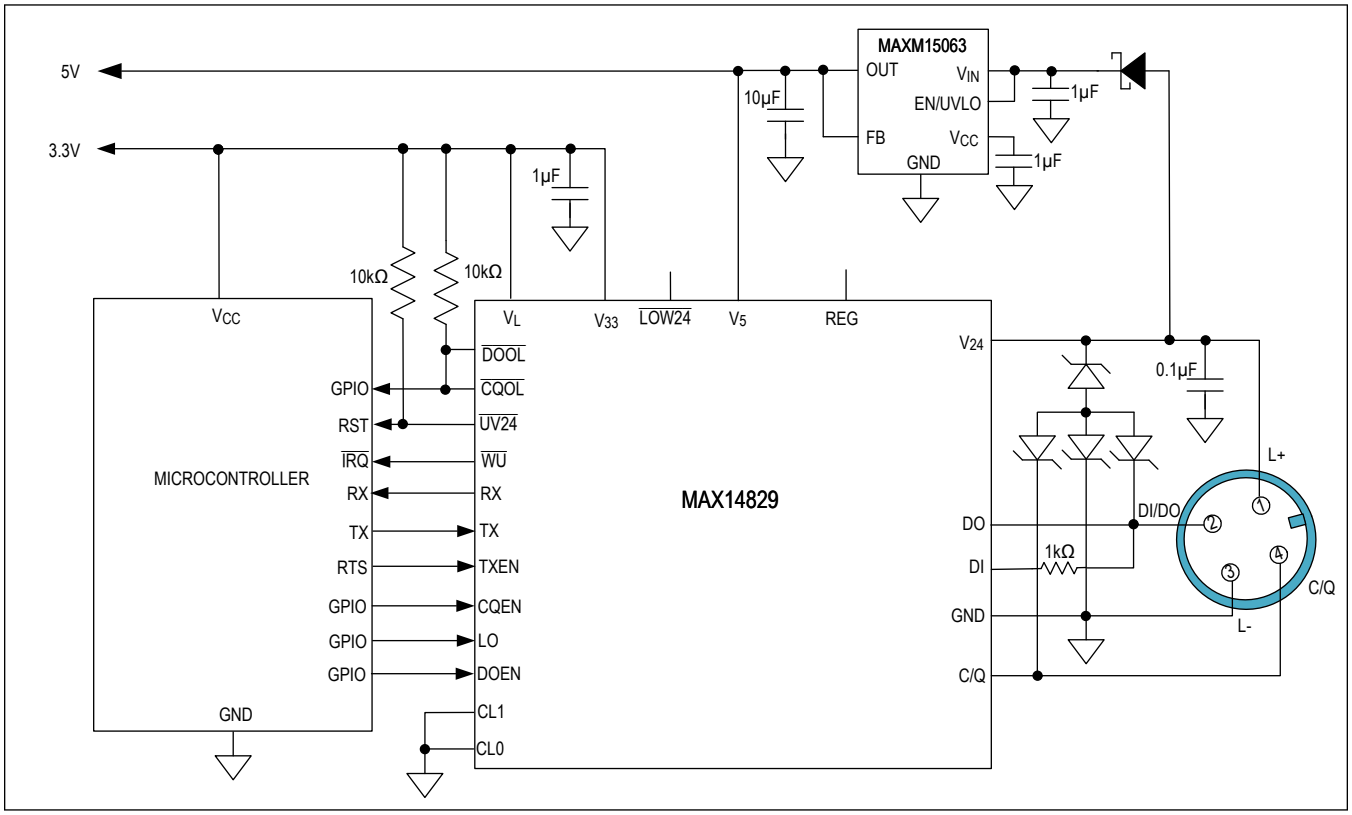


Figure 8. Using an External Step-Down with the 5V Regulator

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14829ATG+	-40°C to +125°C	24 TQFN-EP*
MAX14829ATG+T	-40°C to +125°C	24 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

T = Tape & Reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/18	Initial release	—
1	7/20	Updated the Benefits and Features, Functional Diagram, Pin Description, and Transient Protection sections; updated TOC03	1–2, 10, 15, 19
2	4/21	Added TOC23 and updated the *Low Voltage and Undervoltage Detection* section	12, 18
3	10/21	Updated *Functional Diagram*	15