2.5V/3.3/5V 2.5GHz 1:4 PECL/ECL CLOCK DRIVER WITH 2:1 DIFFERENTIAL INPUT MUX

Precision Edge®
SY89830U

Features

- **Guaranteed AC parameters over temp/voltage:**
  - **> 2.5GHz f_{MAX}**
  - **< 25ps within-device skew**
  - **< 225ps t_r/t_f time**
  - **< 450ps prop delay**
- **Low jitter design:**
  - **< 1ps$_{RMS}$ cycle-to-cycle jitter**
  - **< 15ps$_{PP}$ total jitter**
- **2:1 Differential MUX input**
- **Flexible supply voltage: 2.5V/3.3V/5V**
- **Wide operating temperature range: –40°C to +85°C**
- **100K ECL compatible outputs**
- **Inputs accept PECL/LVPECL/ECL/HSTL logic levels**
- **Available in a 16-pin TSSOP package**

Precision Edge®

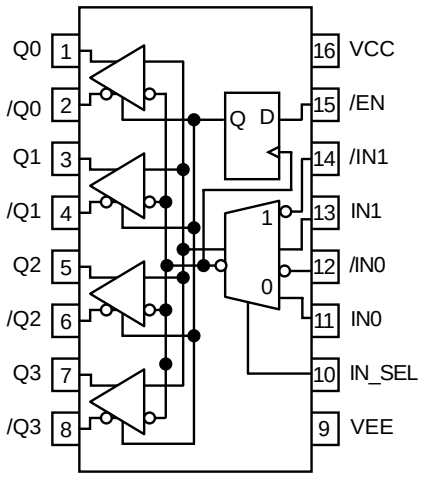
General Description

The SY89830U is a high-speed, 2.5GHz differential PECL 1:4 fanout buffer optimized for ultra-low skew applications. Within device skew is guaranteed to be less than 25ps over temperature and supply voltage. The wide supply voltage operation allows this fanout buffer to operate in 2.5V, 3.3V, and 5V systems.

The SY89830U features a 2:1 input MUX, making it an ideal solution for redundant clock switchover applications. If only one input pair is used, the other pair may be left floating. In addition, this device includes a synchronous enable pin that forces the outputs into a fixed logic state. Enable or disable state is initiated only after the outputs are in a LOW state, thus eliminating the possibility of a “runt” clock pulse.

The SY89830U I/O are fully differential and 100K ECL compatible. Differential 10K ECL logic can interface directly into the SY89830U inputs.

The SY89830U is part of Micrel’s high-speed precision edge timing and distribution family. For applications that require a different I/O combination, consult the Micrel website at www.micrel.com, and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators, and clock generators.



16-Pin TSSOP (T32-1)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89830UK4I	K4-16-1	Industrial	89830U	Sn-Pb
SY89830UK4ITR[2]	K4-16-1	Industrial	89830U	Sn-Pb
SY89830UK4G[3]	K4-16-1	Industrial	89830U with Pb-Free bar line indicator	NiPdAu Pb-Free
SY89830UK4GTR[2, 3]	K4-16-1	Industrial	89830U with Pb-Free bar line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

Pin Number	Pin Name	Pin Function
1, 2, 3, 4, 5, 6, 7, 8	Q0 to Q3 /Q0 to /Q3	(LV)PECL, (LV)ECL differential outputs: Terminate with 50Ω to V_{CC}–2V. For single-ended applications, terminate the unused output with 50Ω to V_{CC}–2V.
9	V_{EE}	Negative Power Supply: For LVPECL, PECL applications, connect to GND.
10	IN_SEL	(LV)PECL, (LV)ECL compatible 2:1 mux input signal select: When IN_SEL is LOW, the IN0 input pair is selected. When IN_SEL is HIGH, the IN1 input pair is selected. Includes a 75kΩ pull-down. Default state is LOW and IN0 is selected.
11, 12, 13, 14	IN0, /IN0 IN1, /IN1	(LV)PECL, (LV)ECL, HSTL clock or data inputs. Internal 75kΩ pull-down resistors on IN0, IN1. Internal 75kΩ pull-up and 75kΩ pull-down resistors on /IN0, /IN1. /IN0, /IN1 default condition is V_{CC}/2 when left floating. IN0, IN1 default condition is LOW when left floating.
15	/EN	(LV)PECL, (LV)ECL compatible synchronous enable: When /EN goes HIGH, Q_{OUT} will go LOW and /Q_{OUT} will go HIGH on the next LOW input clock transition. Includes a 75kΩ pull-down. Default state is LOW when left floating. The internal latch is clocked on the falling edge of the input (IN0, IN1)
16	V_{CC}	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors.

IN0	IN1	IN_SEL	/EN	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
↓	X	L	H	L
X	↓	H	H	L

Note:

1. ↓ = negative edge

Symbol	Rating	Value	Unit
$V_{CC} - V_{EE}$	Power Supply Voltage	6.0	V
V_{IN}	Input Voltage (V_{CC} = 0V, V_{IN} not more negative than V_{EE}) Input Voltage (V_{EE} = 0V, V_{IN} not more positive than V_{CC})	–6.0 to 0 +6.0 to 0	V
I_{OUT}	Output Current –Continuous –Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{LEAD}	Lead Temperature (soldering, 20sec.)	260	°C
T_{store}	Storage Temperature Range	–65 to +150	°C
θ_{JA}	Package Thermal Resistance (Junction-to-Ambient) –Still-Air (single-layer PCB) –Still-Air (multi-layer PCB) –500lfpm (multi-layer PCB)	115 75 65	°C/W
θ_{JC}	Package Thermal Resistance (Junction-to-Case)	21	°C/W

Note:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{CC}	Power Supply Voltage										V	
	(PECL)	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5		
	(LVPECL)	2.375	3.3	3.63	2.375	3.3	3.63	2.375	3.3	3.63		
	(ECL)	–5.5	–5.0	–4.5	–5.5	–5.0	–4.5	–5.5	–5.0	–4.5		
	(LVECL)	–3.63	–3.3	–2.375	–3.63	–3.3	–2.375	–3.63	–3.3	–2.375		
I_{CC}	Power Supply Current	—	—	70	—	50	72	—	—	75	mA	
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	$V_{IN} = V_{IH}$
I_{IL}	Input LOW Current IN	0.5	—	—	0.5	—	—	0.5	—	—	µA	$V_{IN} = V_{IL}$
	/IN	–150	—	—	–150	—	—	–150	—	—	µA	$V_{IN} = V_{IL}$
C_{IN}	Input Capacitance (TSSOP)	—	—	—	—	1.0	—	—	—	—	pF	

Note:

1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

2.5V PECL DC Electrical Characteristics

V_{CC} = 2.5V ±5%, V_{EE} = 0V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage (Single-ended)	555	—	875	555	—	875	555	—	875	mV	V_{CC} = 2.5V
V_{IH}	Input HIGH Voltage (Single-ended)	1275	—	1620	1275	—	1620	1275	—	1620	mV	V_{CC} = 2.5V
V_{OL}	Output LOW Voltage	555	680	805	555	680	805	555	680	805	mV	V_{CC} = 2.5V
V_{OH}	Output HIGH Voltage	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV	V_{CC} = 2.5V
V_{IHCMR}	Input HIGH Voltage Common Mode Range[2]	1.2	—	V_{CC}	1.2	—	V_{CC}	1.2	—	V_{CC}	V	

Notes:

1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters vary 1:1 with V_{CC}. Output load is 50Ω to V_{CC} –2V.
2. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

3.3V PECL DC Electrical Characteristics

V_{CC} = 3.3V ±10%, V_{EE} = 0V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage (Single-Ended)	1355	—	1675	1355	—	1675	1355	—	1675	mV	V_{CC} = 3.3V
V_{IH}	Input HIGH Voltage (Single-Ended)	2075	—	2420	2075	—	2420	2075	—	2420	mV	V_{CC} = 3.3V
V_{OL}	Output LOW Voltage	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV	V_{CC} = 3.3V
V_{OH}	Output HIGH Voltage	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV	V_{CC} = 3.3V
V_{IHCMR}	Input HIGH Voltage Common Mode Range[2]	1.2	—	V_{CC}	1.2	—	V_{CC}	1.2	—	V_{CC}	V	

Notes:

1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters vary 1:1 with V_{CC}. Output load is 50Ω to V_{CC} –2V.
2. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

5.0V PECL DC Electrical Characteristics

V_{CC} = 5.0V ±10%, V_{EE} = 0V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage (Single-Ended)	3055	—	3375	3055	—	3375	3055	—	3375	mV	V_{CC} = 5.0V
V_{IH}	Input HIGH Voltage (Single-Ended)	3775	—	4120	3775	—	4120	3775	—	4120	mV	V_{CC} = 5.0V
V_{OL}	Output LOW Voltage	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV	V_{CC} = 5.0V
V_{OH}	Output HIGH Voltage	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV	V_{CC} = 5.0V
V_{IHCMR}	Input HIGH Voltage[2] Common Mode Range	1.2	—	V_{CC}	1.2	—	V_{CC}	1.2	—	V_{CC}	V	

Notes:

1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters vary 1:1 with V_{CC}. Output load is 50Ω to V_{CC} –2V.
2. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

100KEP DC Electrical Characteristics

V_{CC} = 0V, V_{EE} = –2.375V to –3.63V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage (Single-ended)	–1945	—	–1625	–1945	—	–1625	–1945	—	–1625	mV	
V_{IH}	Input HIGH Voltage (Single-ended)	–1225	—	–880	–1225	—	–880	–1225	—	–880	mV	
V_{OL}	Output LOW Voltage	–1945	–1820	–1695	–1945	–1820	–1695	–1945	–1820	–1695	mV	50Ω to V_{CC}–2V
V_{OH}	Output HIGH Voltage	–1145	–1020	–895	–1145	–1020	–895	–1145	–1020	–895	mV	50Ω to V_{CC}–2V
V_{IHCMR}	Input HIGH Voltage Common Mode Range[2]	V_{EE} +1.2	—	0.0	V_{EE} +1.2	—	0.0	V_{EE} +1.2	—	0.0	V	

Notes:

1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.
2. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

100KEP DC Electrical Characteristics

V_{CC} = 0V, V_{EE} = –4.5V to –5.5V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage (Single-ended)	–1945	—	–1625	–1945	—	–1625	–1945	—	–1625	mV	
V_{IH}	Input HIGH Voltage (Single-ended)	–1225	—	–880	–1225	—	–880	–1225	—	–880	mV	
V_{OL}	Output LOW Voltage	–1945	–1820	–1695	–1945	–1820	–1695	–1945	–1820	–1695	mV	50Ω to V_{CC}–2V
V_{OH}	Output HIGH Voltage	–1145	–1020	–895	–1145	–1020	–895	–1145	–1020	–895	mV	50Ω to V_{CC}–2V
V_{IHCMR}	Input HIGH Voltage Common Mode Range[2]	V_{EE} +1.2	—	0.0	V_{EE} +1.2	—	0.0	V_{EE} +1.2	—	0.0	V	

Notes:

1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.
2. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

100KEP DC Electrical Characteristics

V_{CC} = 2.375V to 3.63V, V_{EE} = 0V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IH}	Input HIGH Voltage	1200	—	—	1200	—	—	1200	—	—	mV
V_{IL}	Input LOW Voltage	—	—	400	—	—	400	—	—	400	mV

LVPECL: V_{CC} = 2.375V to 3.63V, V_{EE} = 0V; PECL: V_{CC} = 4.50V to 5.50V, V_{EE} = 0V
LVECL: V_{CC} = 0V, V_{EE} = –2.375V to –3.63V; ECL: V_{CC} = 0V, V_{EE} = –4.50V to –5.5V

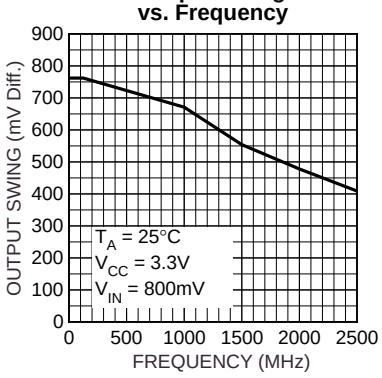
Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}[1]	Maximum Frequency	2.5	—	—	2.5	—	—	2.5	—	—	GHz
t_{PD}	Propagation Delay to Output LVPECL/LVECL										
	Diff. IN (150mV)	—	—	—	—	375	—	—	—	—	ps
	Diff. IN (800mV)	300	350	450	300	350	450	300	350	450	ps
	Single-Ended IN	—	—	—	—	375	—	—	—	—	ps
	PECL/ECL										
	Diff. IN (150mV)	—	—	—	—	375	—	—	—	—	ps
	Diff. IN (800mV)	275	350	425	275	350	425	275	350	425	ps
	Single-Ended IN	—	—	—	—	355	—	—	—	—	ps
	HSTL	325	—	500	300	—	450	300	—	450	ps
t_{SKEW}[2]	Within-Device Skew (Diff.)	—	15	25	—	15	25	—	15	25	ps
	Part-to-Part Skew (Diff.)	—	100	150	—	100	150	—	100	150	ps
t_{SW}	Select to Valid Output Switchover Time	—	—	450	—	400	450	—	—	450	ps
t_S[3]	Set-Up Time /EN to CLK	100	0	—	100	0	—	100	0	—	ps
t_H[3]	Hold Time /EN to CLK	200	50	—	200	50	—	200	50	—	ps
t_{JITTER}	Cycle-to-Cycle[4]	—	0.2	1	—	0.2	1	—	0.2	1	ps_{RMS}
	Total Jitter (622MHz clock)[5]	—	<15	—	—	<15	—	—	<15	—	ps_{PP}
V_{ID}	Input Voltage Swing	150	800	1200	150	800	1200	150	800	1200	mV
t_r, t_f	Output Rise/Fall Times (20% to 80%)	75	—	225	75	130	225	85	—	225	ps

Notes:

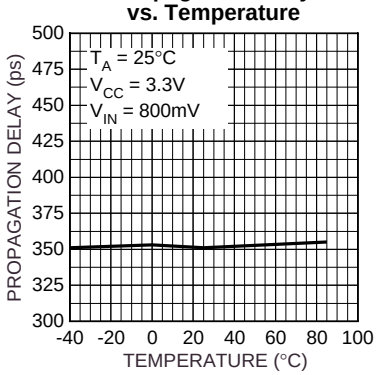
1. f_{MAX} is defined as the maximum toggle frequency. Measured with 750mV input signal, 50% duty cycle, output swing ≥ 400mV (diff), all loading with 50Ω to V_{CC}–2V.
2. Skew is measured between outputs under identical transitions.
3. Set-up and hold times apply to synchronous applications that intend to enable/disable before the next cycle. For asynchronous applications, set-up and hold time does not apply.
4. Cycle-to-cycle jitter definition: The variation in period between adjacent cycles over a random sample of adjacent cycle pairs. $T_{JITTER\_CC} = T_n – T_{n+1}$ where T is the time between rising edges of the output signal.
5. Total jitter definition: with an ideal clock input applied to one channel of the MUX, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

V_{CC} = 3.3V, V_{EE} = GND, T_A = 25°C, unless otherwise stated.

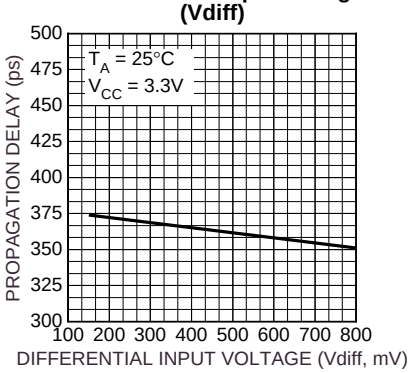
Output Swing vs. Frequency



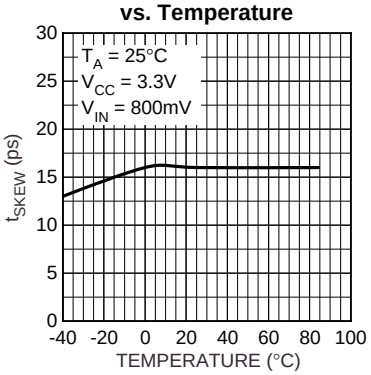
Propagation Delay vs. Temperature



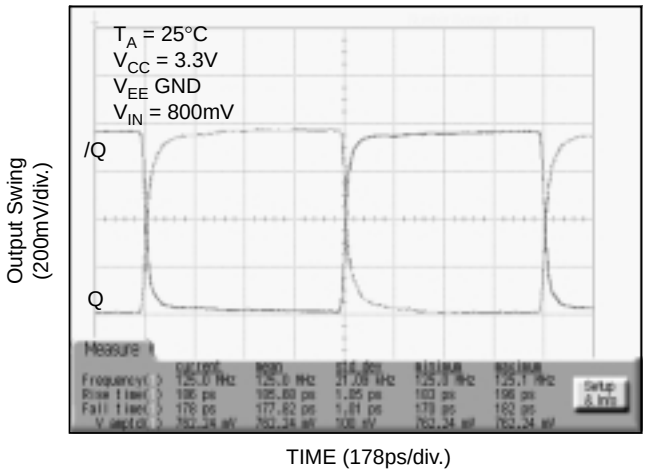
Propagation Delay vs. Differential Input Voltage (Vdiff)



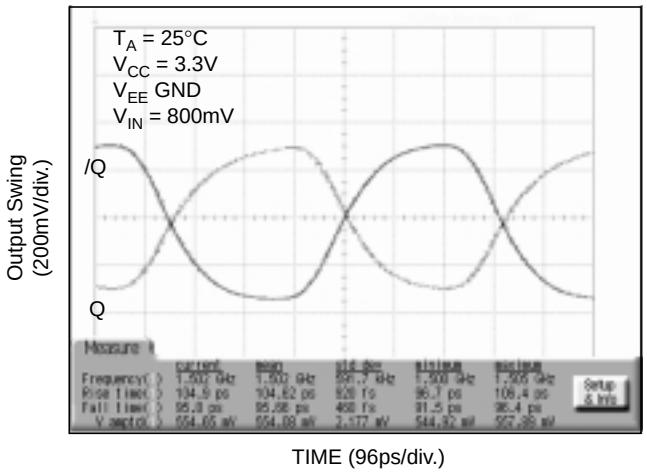
t_{SKEW} vs. Temperature



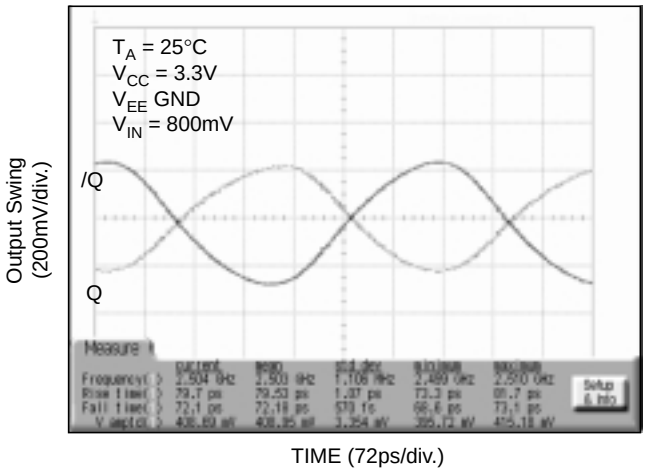
125MHz Output



1.5GHz Output



2.5GHz Output



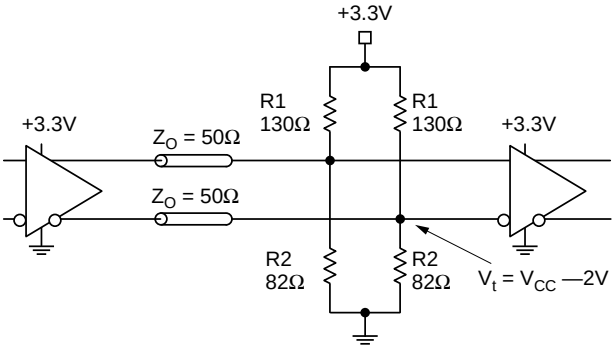


Figure 1. Parallel Termination–Thevenin Equivalent

Notes:

1. For +2.5V systems:
   R1 = 250Ω
   R2 = 62.5Ω
2. For +5.0V systems:
   R1 = 82Ω
   R2 = 130Ω

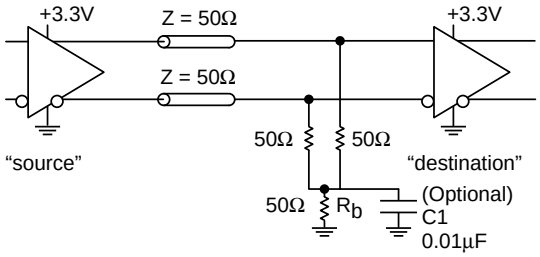


Figure 2. Three-Resistor "Y–Termination"

Notes:

1. Power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. R_b resistor sets the DC bias voltage, equal to V_t. For +3.3V systems R_b = 46Ω to 50Ω. For +5V systems, R_b = 110Ω.
4. C1 is an optional bypass capacitor intended to compensate for any tr/tf mismatches.

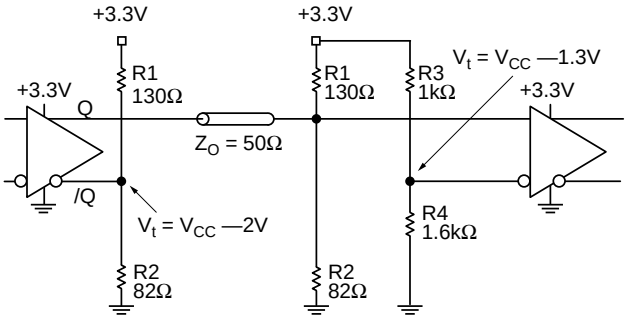
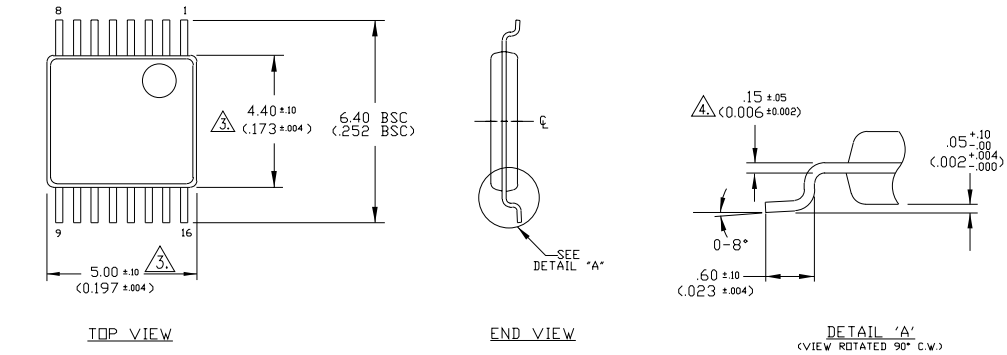


Figure 3. Terminating Unused I/O

Notes:

1. Unused output (/Q) must be terminated to balance the output.
2. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω, R3 = 1.25kΩ, R4 = 1.2kΩ.



TOP VIEW

END VIEW

DETAIL 'A'
(VIEW ROTATED 90° C.W.)

SIDE VIEW

NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
4. THIS DIMENSION INCLUDES LEAD FINISH.

Rev. 01

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB http://www.micrel.com